A PROPORTIONAL WIRE CHAMBER ELECTRONICS SYSTEM UTILIZING CAMAC*

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Summary

This report describes a system of electronics to be used with a proportional wire chamber hodoscope. The system, which uses CAMAC packaging and data handling philosophy, consists of octo (8 channel) wire signal amplifiers, octo 4-bit per wire latch modules, gate fanout modules, crate controllers, and two types of data processor-interface units to the SDS 9300 computer. System operation is explained, and each component is described.

Introduction

This report describes a system of electronics to be used with proportional wire chambers which will be installed in the SLAC 20-BeV spectrometer for an experiment in December 1970. In this application the chambers are used as position defining hodoscopes with an externally generated fast gate ($\approx$ 15-30 nsec) for the electronics. Considerable attention has been given to the timing characteristics of the electronics. Preliminary reports on chamber performance are available.[1,2]

Physical considerations and previous spectrometer operating policies require minimum electronics at the chambers, so the wire amplifiers have been physically separated from the data processing electronics. Amplified wire signals will be transmitted about 400 feet over existing high quality 50 Ω coax.

CAMAC[3] packaging and system concepts are used as a convenient method for achieving modularity, flexibility, and ease of expansion, although the more sophisticated aspects of CAMAC are not applicable.

Experimental considerations and processing speed limitations require storing of up to 4 independent events per beam pulse, which has a 1.6 μsec maximum width, and a maximum 360 pps rate. Each channel therefore contains 4 latch flip-flops.

The system includes a data processor as an interface to the SDS 9300 computer which generates wire addresses, in order to reduce data flow and produce data in a more convenient, preprocessed form. Although a processor with internal memory was originally proposed for optimum data flow, a simpler "scan-stop-read" scanner was built as an interim unit due to schedule considerations. Both units have been built and tested and will be described.

System test facilities are built into the chambers, so that an entire chamber can be pulsed, read out, and verified.

For the initial installation it is planned to have 5 chambers, with about 400 total active wires.

System Description and Operation

The overall block diagram of the wire chamber electronics is shown in Fig. 1. Plug-in cards located at the chamber contain amplifiers which raise the wire signals to a -700 mV level for direct transmission over existing Foam-8 cables to the Counting House where latch units, processor, computer, the fast trigger logic, etc. are located. Since the signals are already on coax cables, the additional delays which are normally needed for proportional wire chamber signals are externally inserted with coax cables, thereby eliminating the need for any delays in the electronic circuits.

Digital storage (latching) of the chamber signals takes place in the octo-4-bit latch module. Each latch unit accepts 4 NIM fast logic gates each of which is fanned out from a 16-fold fanout unit. The readout system accepts up to 16 latch modules in a crate; a design decision based upon crate power considerations, readout word format, and chamber size. The data is read out onto the CAMAC Read lines in 8-bit words, 4 per module, in order to minimize readout circuits in the module. CAMAC standards (EUR 4100e) are followed quite closely inside the crate.

Up to 8 crates are tied together via simplified crate controllers and a much simplified branch highway which contains only 8 data lines, 3 crate address lines, 4 module address lines, 2 event lines (subaddress), a clear line and the S2 strobe line. In general, the crate controller and branch highway are not in accordance with the proposed branch highway specification EUR 4600e, although many of the concepts are similar. The readout philosophy is quite simple: the address is placed on the branch highway, and the returning data is read (strobed) at the last moment, i.e., just before the address is changed again. This allows maximum settling time of the lines. In our system we have scanned successfully at a 2 MHz rate.

The scanner interfaces the branch highway to the computer I/O and contains sequential addressing and processing logic to generate 2 wire addresses in a 24-bit computer word (see Fig. 2). After reading the word the computer acknowledges, and the scanner resumes until the next 2 addresses are found. During scanning, the computer is held by a "not ready" signal. The scanner scans the 8-bit words at a 2 MHz rate, so that the maximum scanning time for 4 events, 8 crates, with 128 modules, is 256 μsec, in addition to the computer input time.

The memory processor, which is an alternate to the scanner described above, generates two wire addresses per 24-bit word just as in the scanner, but scanning is done off-line and addresses are stored in a 63 word memory. At the end of scanning, the computer is interrupted and the data is read in at a rate limited only by the computer I/O capability. An identification word preceding the data (see Fig. 2) gives the number of wires hit (half-word count) to set up a software read-in table. Since the scanning is off-line, the scan rate is not critical: the selected scan rate of 500 kHz results in a maximum scan time of 1 millisec, well under the SLAC beam spacing of 2.78 millisec.

The basic operating sequence is described as follows. During the beam pulse the trigger logic sends gate signals which strobe data into the latches; after the beam pulse the scanner (processor) is started and subsequently sends wire addresses to the computer. After the data has been sent the scanner (processor) is reset, the latches are reset, and the system is ready to take data from the next beam pulse.

High Speed Electronics

Amplifier

The amplifiers are of conventional design using MC1035 IC's, and are packaged 8 channels on a card which plugs into connectors mounted on the chamber. The overall gain is nominally 600 and the output limits at about -700 mV into 50 Ω.

The output, specifically at the request of the experimenters, contains no shapers or standardizing circuitry.

The schematic of the amplifier is shown in Fig. 3 and a photograph in Fig. 4. Special efforts in board layout were made to minimize input wire lengths and channel coupling.

Fanouts

The fanout units are constructed in a single width CAMAC module using conventional circuits and MECL II IC's. A partial schematic for 4 outputs is shown in Fig. 5. Each fanout handles 1 event gate and can drive up to 16 latch module gate inputs in the crate. The unit is dc coupled and has output rise and fall times in the order of 5 nsec, which is adequate for the 15-30 nsec gate widths.

A photograph of the unit is shown in Fig. 6. Note that Sealectro Snap-on connectors have been used wherever possible, instead of the standard LEMO connector, for space and cost considerations. The module uses only -6 V power and draws about 350 mA.

Octo-4-Bit Latch

This single width module contains 8 identical channels, each with a storage capacity of four bits. Four 50 Ω gate inputs accept the NIM fast gates which sequentially strobe the 8 inputs. A block diagram of the unit is shown in Fig. 7, and a detailed schematic of a single channel in Fig. 8. Each channel consists of a MC1035 differential receiver-discriminator stage which switches at -300 mV and standardizes the signals from the wire amplifiers into an 8 nsec MECL level pulse. Thirty-two latch flip-flops consisting of cross-coupled MC1010 gates store the signals after strobing with the event gates. The flip-flop outputs are individually gated onto an 8 bit MECL emitter OR bus which is translated to TTL open collector output levels for the CAMAC read lines. Each 8 bits of readout represents storage of one event in the module. CAMAC addressing is employed: this includes the station line N, and the subaddress lines A1 and A2 for the 4 events. Although multiple function codes are not used in this system, the module includes a gate for F(0), Read, so that the module can be used in other more complex systems in the future. The address logic uses one 5 input NAND gate for the F(0), and a Signetics N8251B decoder for the address decoding, the levels of which are translated to MECL to operate the read gates. The latch reset requires an "AND" of Clear and S2, as recommended in CAMAC.

Timing performance of the channel is shown in Fig. 9 which shows gate efficiency for a 15 nsec gate as a function of relative signal and gate timing. It should be pointed out that these measurements were made with 1 nsec time resolution so that the curves are somewhat coarse and only give an indication of the noise and stability of the latch module circuits.

In addition, channel-to-channel variations in nominal gate times occur due to circuit delay differences, layout effects, and differences in circuit thresholds, and give a further indication of the performance. Measurements performed on a single latch module showed timing differences of approximately 1 nsec.

The module uses about 1.1 amps at -6 V and less than 100 mA at +6 V; both voltages are dropped to the proper IC voltages in the module.

The photograph of the module is shown in Fig. 10. Again careful consideration is given to minimum input wire lengths and uniform layout.

Data Handling Electronics

Crate Controller

A minimum nonstandard crate controller was designed especially for this application which is justified by the number of units (up to 8) to be built. However, the branch highway served by the crate controllers employs some of the principles of the proposed standard CAMAC highway.

The details of the branch highway twisted-pair line driving are shown in Fig. 11. The address, Clear and S2 lines are driven by the National DM8830N line driver selected for its ability to drive low line impedances. Dual terminations to +5 V and ground are placed in a termination unit at the far end of the line[4] for optimum termination, although initial tests of the system have shown that such a termination is not required since the branch highway is relatively short (10'-20'). Signals are received in the controllers by the Signetics SP380A Utilogic circuit, which has a high switching threshold ($\approx$ 1.9 V) and at the same time very light input loading, so that transmission approaches the simplified ideal case. The 8 data lines in the highway are driven in each controller by paralleled MC858P open-collector circuits capable of sinking 72 mA nominal at ground. Line terminators to +5 V are located in the processor and/or the line terminator. At the present time 100 Ω (50 mA) data line pull-up resistors in the 2 MHz scanner have proven adequate, whereas 220 Ω pull-up resistors have been used in the processor which scans at 500 kHz.

A block diagram of the crate controller is shown in Fig. 12. The crate number is manually set on a thumbwheel. A comparison circuit energizes the subaddress, station lines, and data outputs when the selected crate address is recognized. Gating of the data lines is not logically necessary, but guards against a faulty module in a crate affecting the rest of the system. Note that no timing or module response signals are used in the unit. Pull-up resistors are added to the CAMAC Dataway lines in accordance with the CAMAC specification.

As shown in the photograph (Fig. 13) two branch highway connectors are included which are directly bussed to each other. Mechanical construction is straightforward with the smaller second board in the Normal CAMAC station floating to facilitate alignment. The crate controller contains 13 IC's and draws about 300 mA at +6 V.

Scanner

The scanner drives the branch highway, receives the data, and processes it into 24-bit words for the SDS 9300 computer. The unit, shown in Fig. 14, is constructed in conventional chassis form with about 70 TTL IC's connected by wire-wrap.

The heart of the unit is the 9-bit address counter shown in the block diagram, Fig. 15. This synchronous counter sequentially scans the modules at a 2 MHz rate while the scanner tests for 1's in the 8-bit data stream with a strobed OR gate. When a "1" is detected, the address scanning stops and the 8 data bits are then scanned at 4 MHz by an 8 to 1 line multiplexer. For each "1" found, the complete 12-bit address is stored in one-half of a 24-bit register and the half-word counter is incremented by 1. When the 24-bit word is full, the wire scan stops and the computer reads the data word, after which the wire scan resumes. If there are no more "ones" in the 8-bit data set then the system reverts to the 2 MHz module scan. This continues until the scan is complete (End of wires), or until the half-word counter reaches 128 (Overflow), after which the half-word count is sent. Then the computer is signalled on the skip bus that the readout is complete. Resetting of the scanner and/or latches may be automatic or external as desired.

The scanner contains two thumbwheels to limit the extent of the scan and thereby reduce overall scan time. These permit setting of the last crate (0-7) and the last event (0-3).

Memory Processor

The memory processor is constructed on wire-wrap cards which plug into a commercial wire-wrap chassis (see Fig. 16), and is based upon the use of Intel Corp. 3101 4-bit × 16-word semiconductor memory chips organized into a 64-word, 24-bit high speed read-write memory. The memory is split into two 12-bit halves for purposes of writing half words, but is read out in 24-bit words.

The block diagram is shown in Fig. 17. Operation is quite straightforward, and is somewhat similar to the scanner described above. An address generator produces sequential 9-bit addresses for the branch highway, and as the 8 bits of data return they are strobed and stored in a register which is continuously scanned by a multiplexer at a 4 MHz rate. The full 12-bit word addresses are continuously applied to the memory data input lines. When a "1" is found a write enable is sent to the next half of the memory bank to store the wire address at successive memory locations. Note that the wire address comes from a delayed address register which is required since the data in the data register is out of phase with the branch highway address counter by one full module data word. A separate memory address counter and control system keeps track of the current memory location, memory overflow, and terminates writing after memory overflow. The same memory address counter is used in the readout cycle.

During readout, the identification word, which precedes the data set (see Fig. 2), is read from a separate register through multiplexer gates into the output. Then the memory is sequentially read out. After the last data word a full word of zeroes is read out as a further check on computer-processor synchronization.

As in the scanner, the memory processor contains thumbwheels to limit the scan to the desired number of crates and events.

The memory processor will not reach its full potential until the computer read-in rate is considerably increased, since the rate is now computer I/O limited to about 30 μsec per word.

Crates and Power Supplies

Standard CAMAC crates, 24 position, manufactured by Nuclear Enterprises, Inc., are being used for this system; each is presently powered by custom packaged Lambda half-rack supplies, -6 V at 30 A, and +6 V at 10 A. A full crate of latch modules, fanouts, and controller draws approximately 18 A at -6 V and approximately 1.4 A at +6 V. Although forced circulation is planned, the modules show minimal temperature rise without it, due to the front entry convention cooling provided by the Nuclear Enterprises crate. Figure 18 shows a photograph of the crate and power supply.

Because of the low power drain on the +6 V supply, it now appears that a more optimum arrangement would be dual 6 V, 30 A supplies, with one supply devoted to all the +6 V power for the system. In this way 5 crates, for example, can be powered with 3 power supply chassis instead of 5. It is expected to make this packaging change in the near future in order to save valuable space and to standardize on supplies.

Conclusion

We have described a proportional wire chamber electronics system built around CAMAC for convenience and flexibility.

It should be pointed out that the system is not limited to the processing technique described in this report. For example, direct read-in with data packaged as 3-8 bit data words per 24-bit computer word may be accomplished by substituting another interface between the branch highway and the computer port.

To a large extent the system approach described here is a direct result of the SLAC accelerator characteristics of low rate and low duty cycle, which allows considerable time for data processing between beam pulses.

References

1. E. Bloom et al., "Multiwire proportional chambers," Report No. SLAC-TN-70-5, Stanford Linear Accelerator Center (March 1970).

2. E. Bloom et al., "Multiwire proportional chambers," Internal Memorandum, Stanford Linear Accelerator Center (October 27, 1970).

3. CAMAC, A Modular Instrumentation System for Data Handling, Report No. EUR 4100e, EURATOM (March 1969).

4. Abdel-Latif, Strutt, A New Integrated Gate Eliminating Line Reflections in High-Speed Digital Systems, Proceedings of IEEE, June 1970, pp. 936-938.
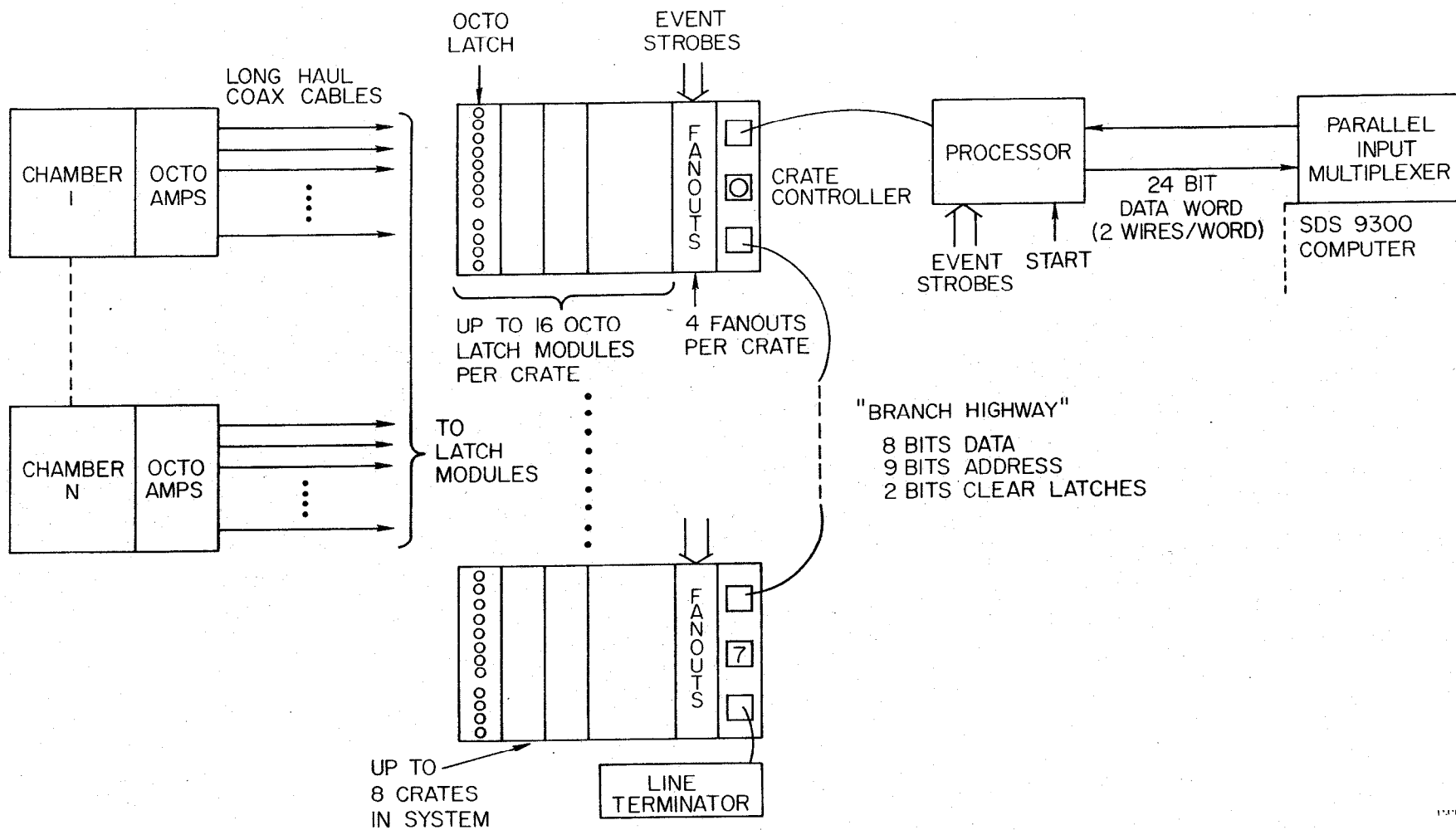
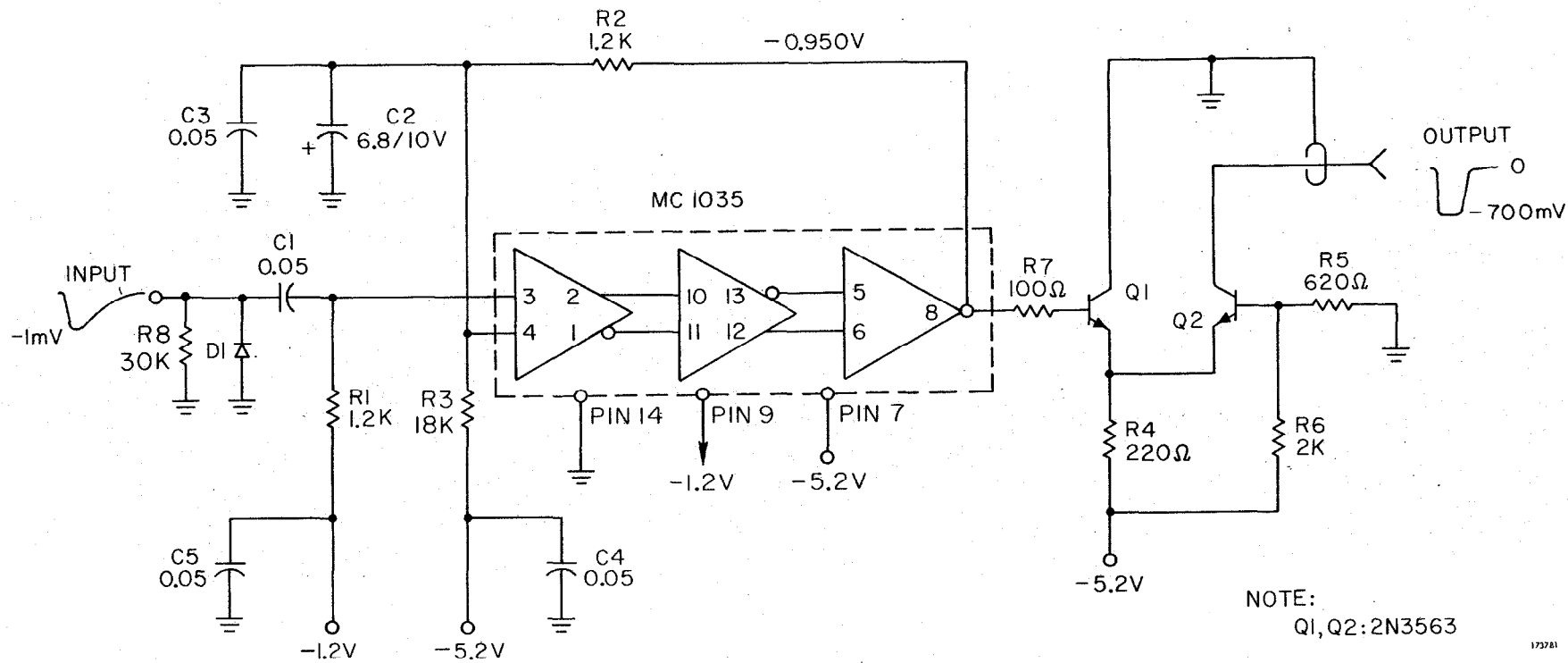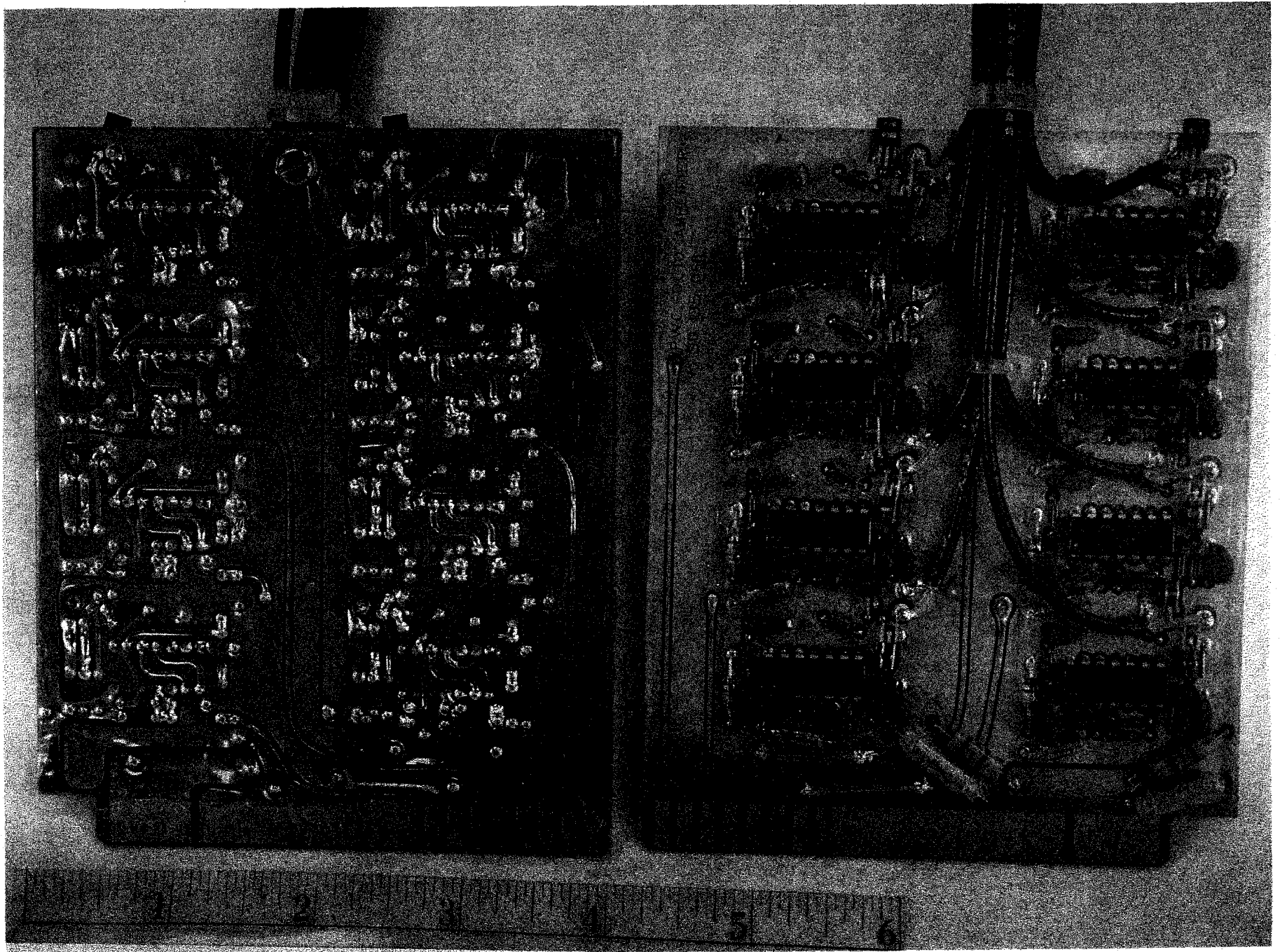FIG. 1--Proportional wire chamber electronics — overall block diagram.

BIT NUMBER 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23

| MEMORY OVERFLOW | 0 0 0 0 0 0 0 | | EVENT 3 | EVENT 2 | EVENT 1 | EVENT 0 | M.S.B. 2^{11} | 12 BIT HALF-WORD COUNTER (MEMORY PROCESSOR) 7 BIT HALF-WORD COUNTER (SCANNER) | L.S.B. 2^0 |

IDENTIFICATION WORD

BIT NUMBER 0   12   23

| SAME FORMAT NEXT HIGHER ADDRESS | EVENT 2^1 2^0 | CRATE 2^2 2^1 2^0 | MODULE 2^3 2^2 2^1 2^0 | WIRE 2^2 2^1 2^0 |

DATA WORD

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FIG. 2--Word format.

FIG. 3--Amplifier circuit diagram.

FIG. 4--Photograph of the octo-amplifier.

FIG. 5--Fanout circuit diagram.
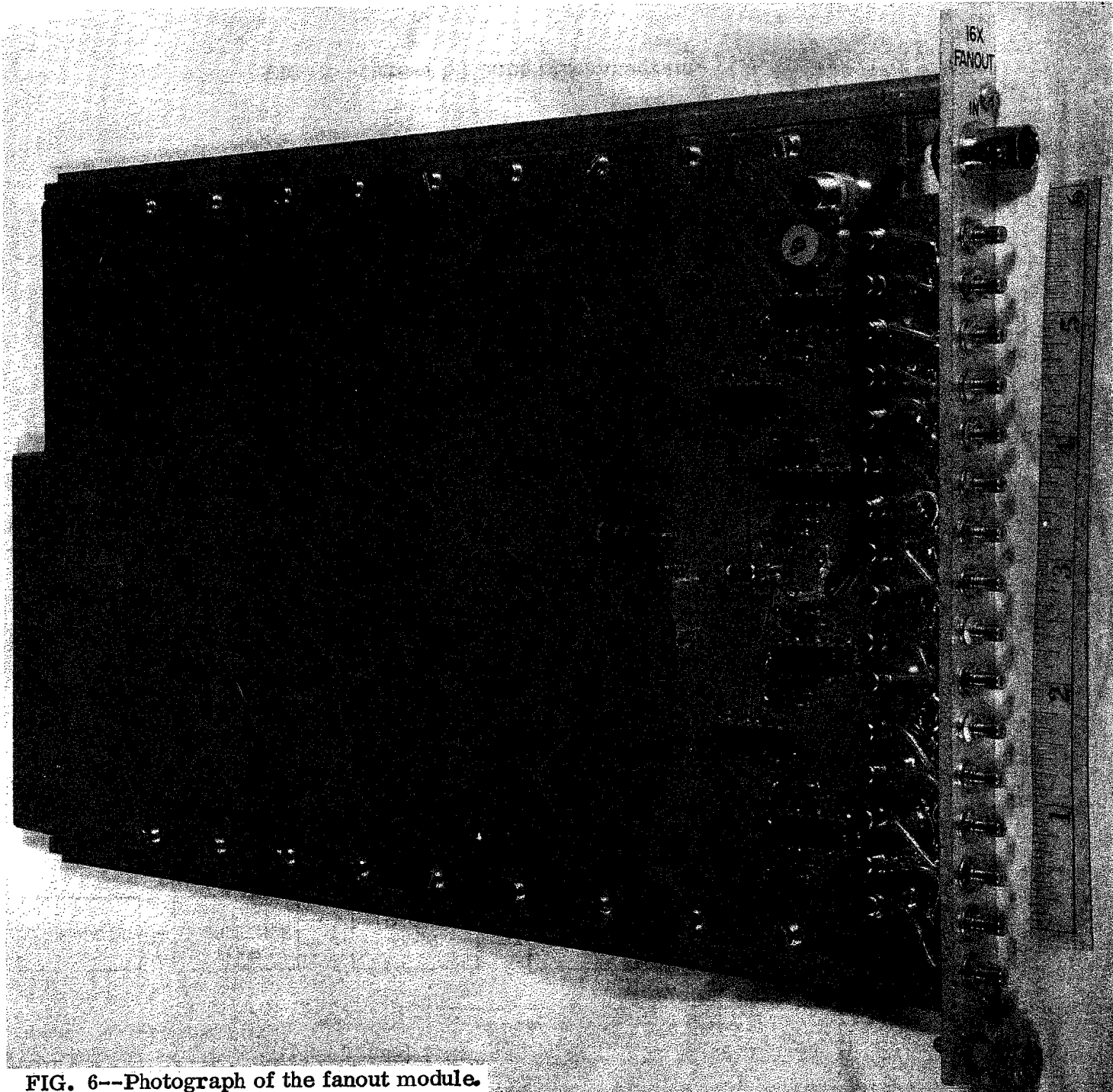
FIG. 6--Photograph of the fanout module.

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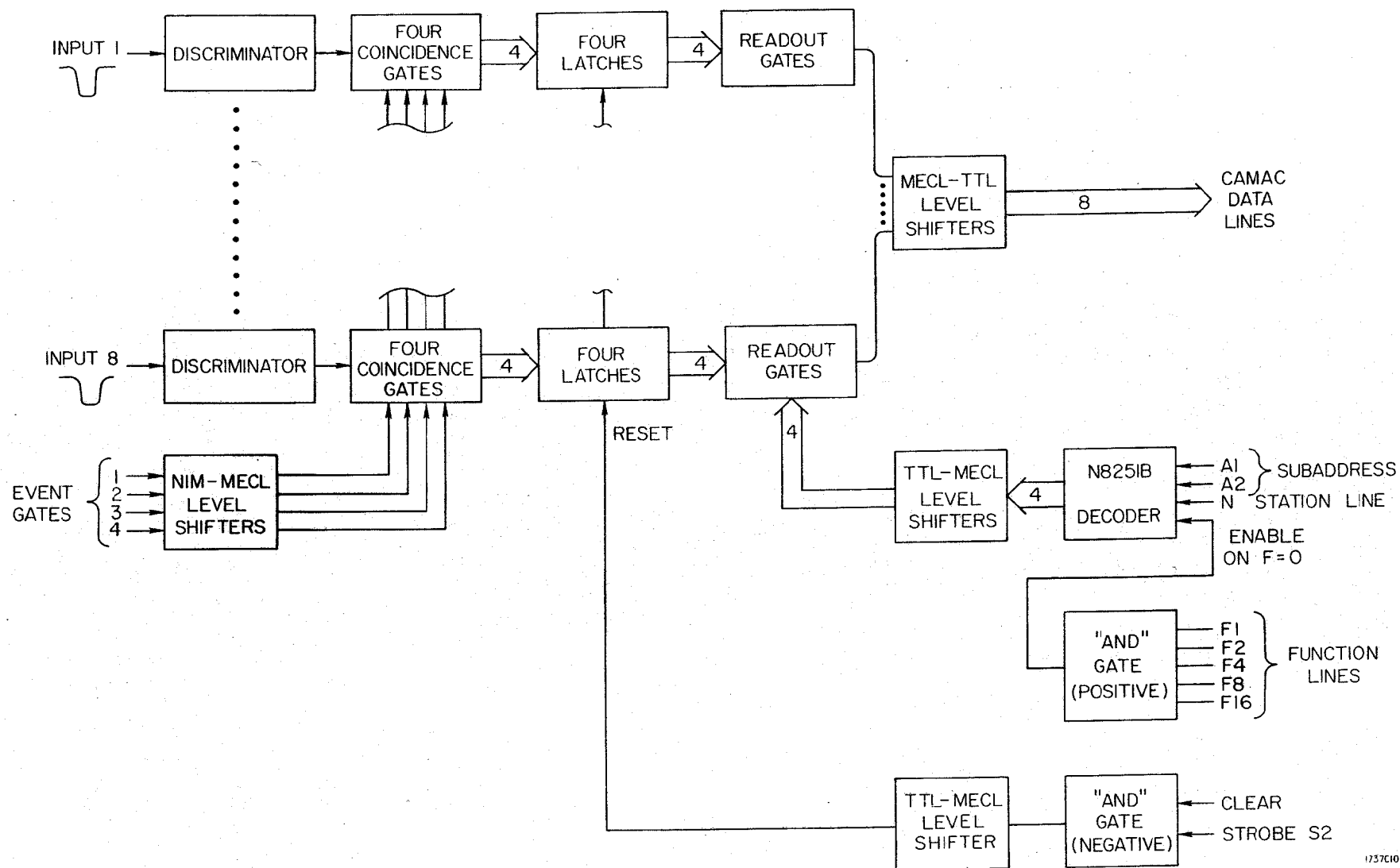
FIG. 7--Octo-4 bit latch block diagram.
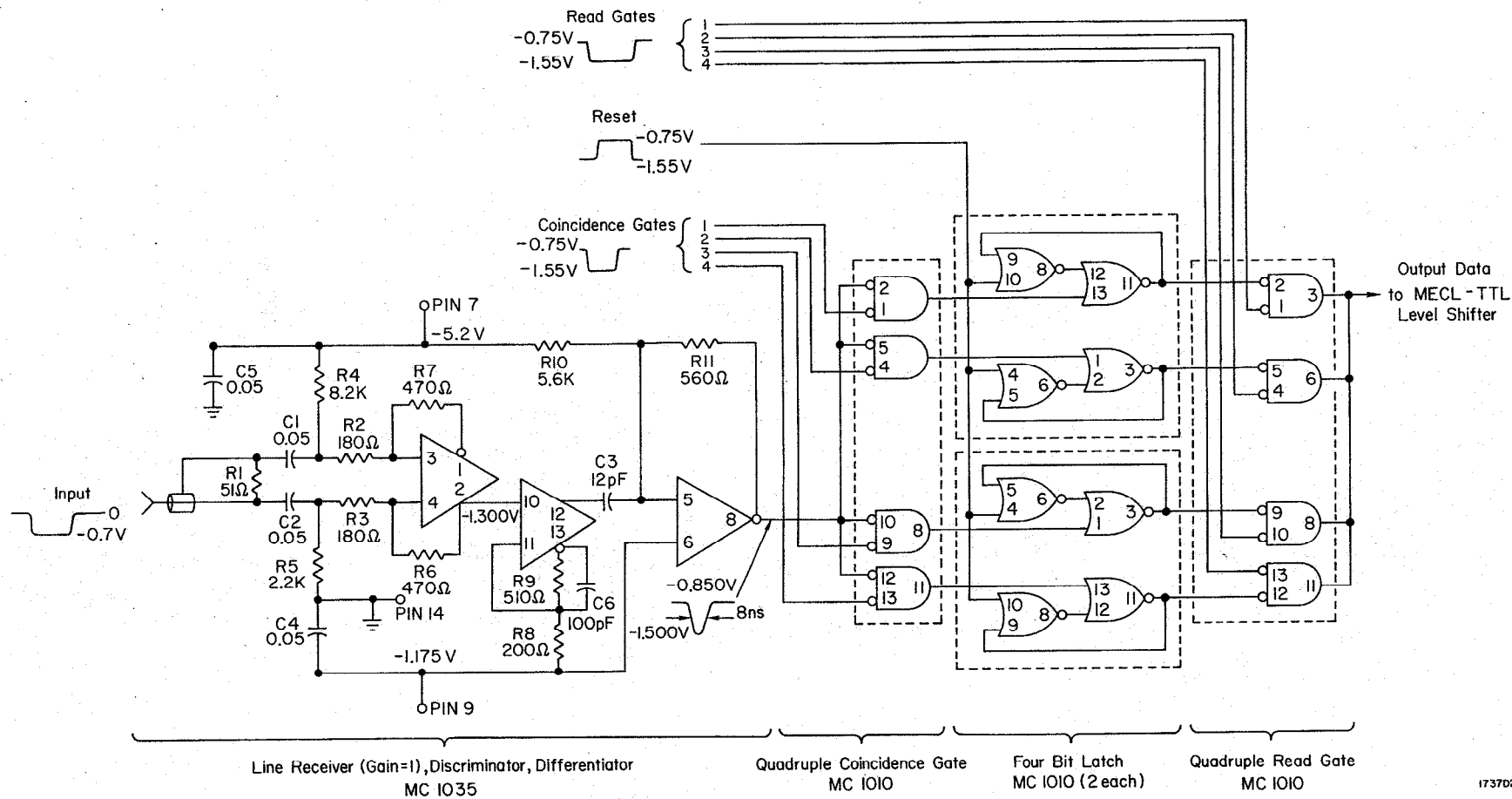
FIG. 8--Circuit diagram of single channel of octo-4 bit latch.
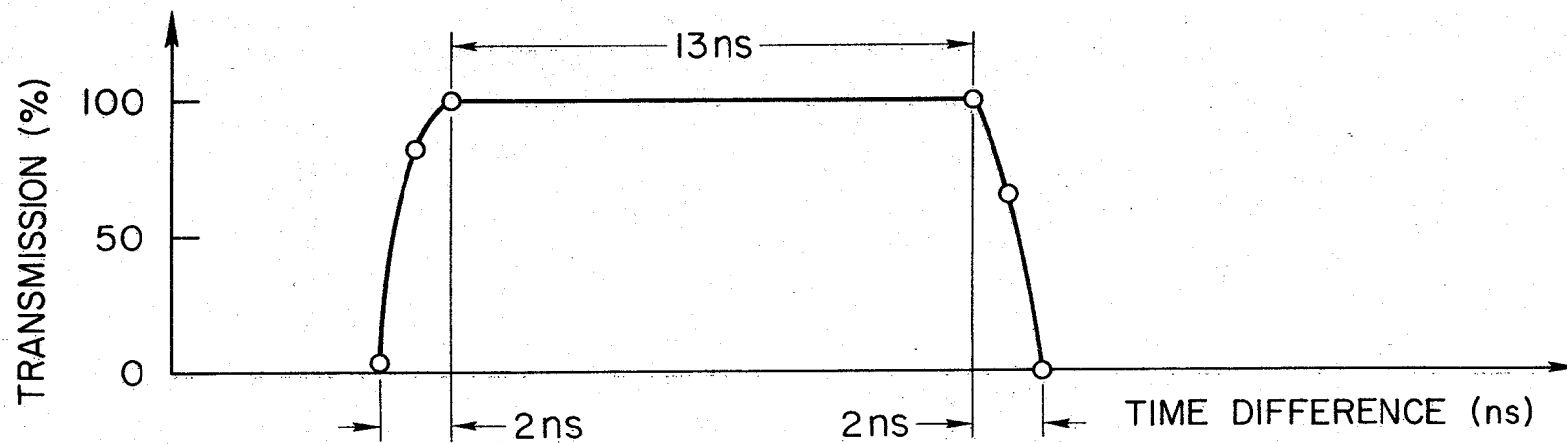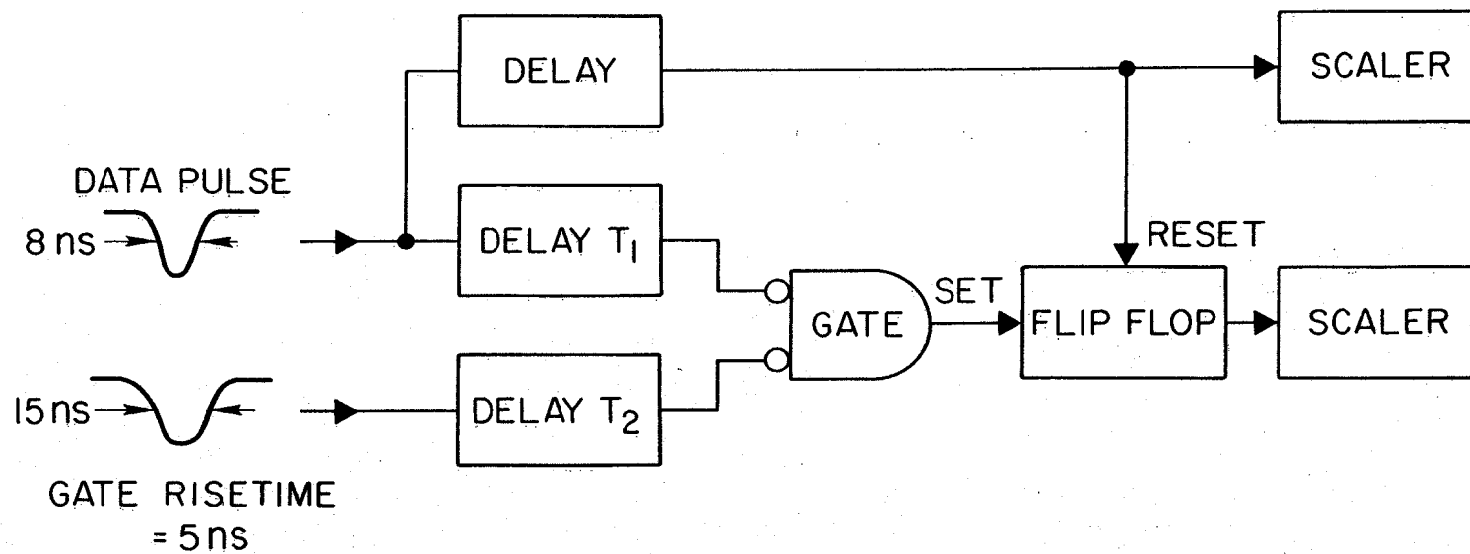
FIG. 9--Coincidence gate efficiency — T1 and T2 vary in 1 nsec increments.
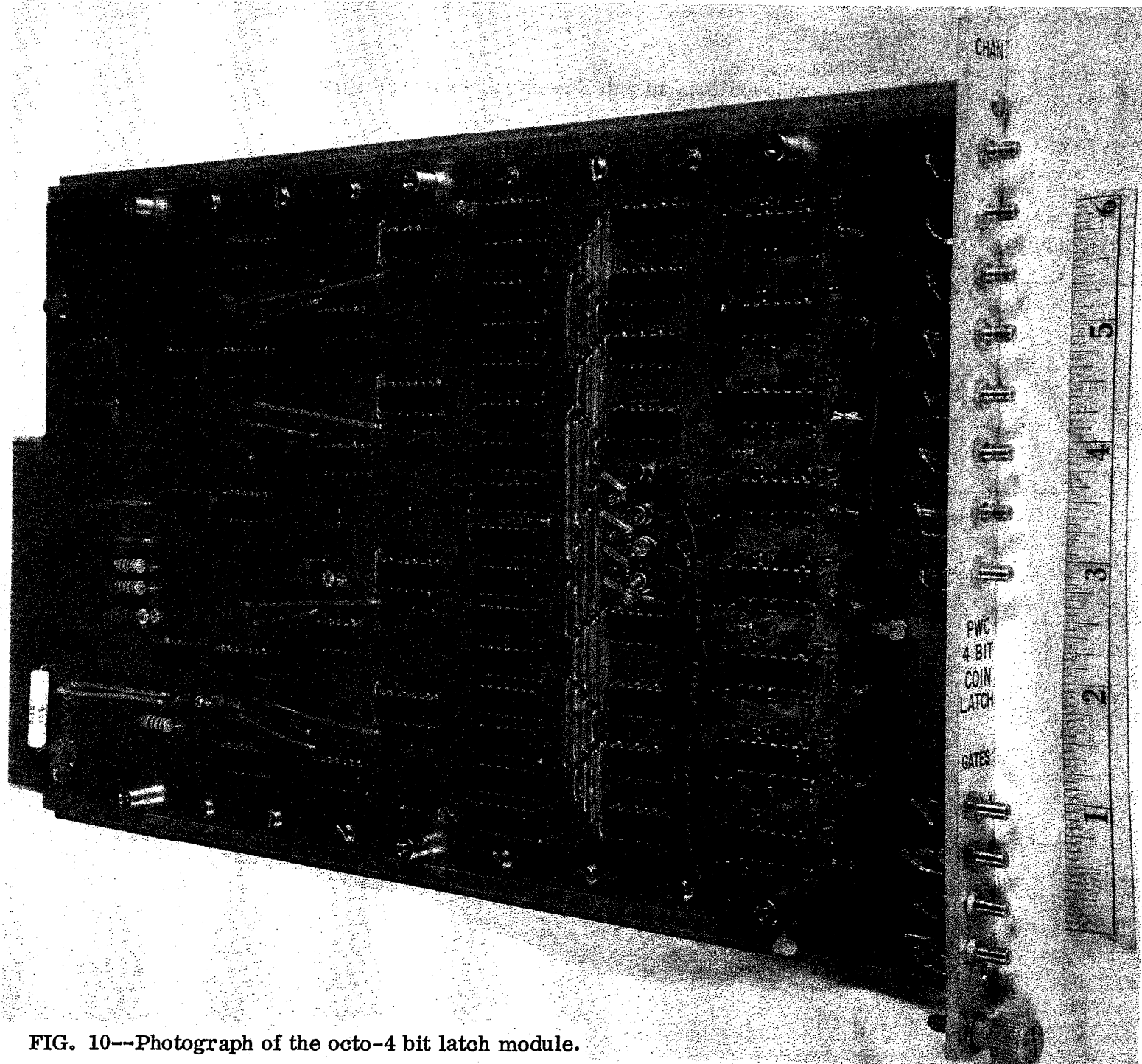
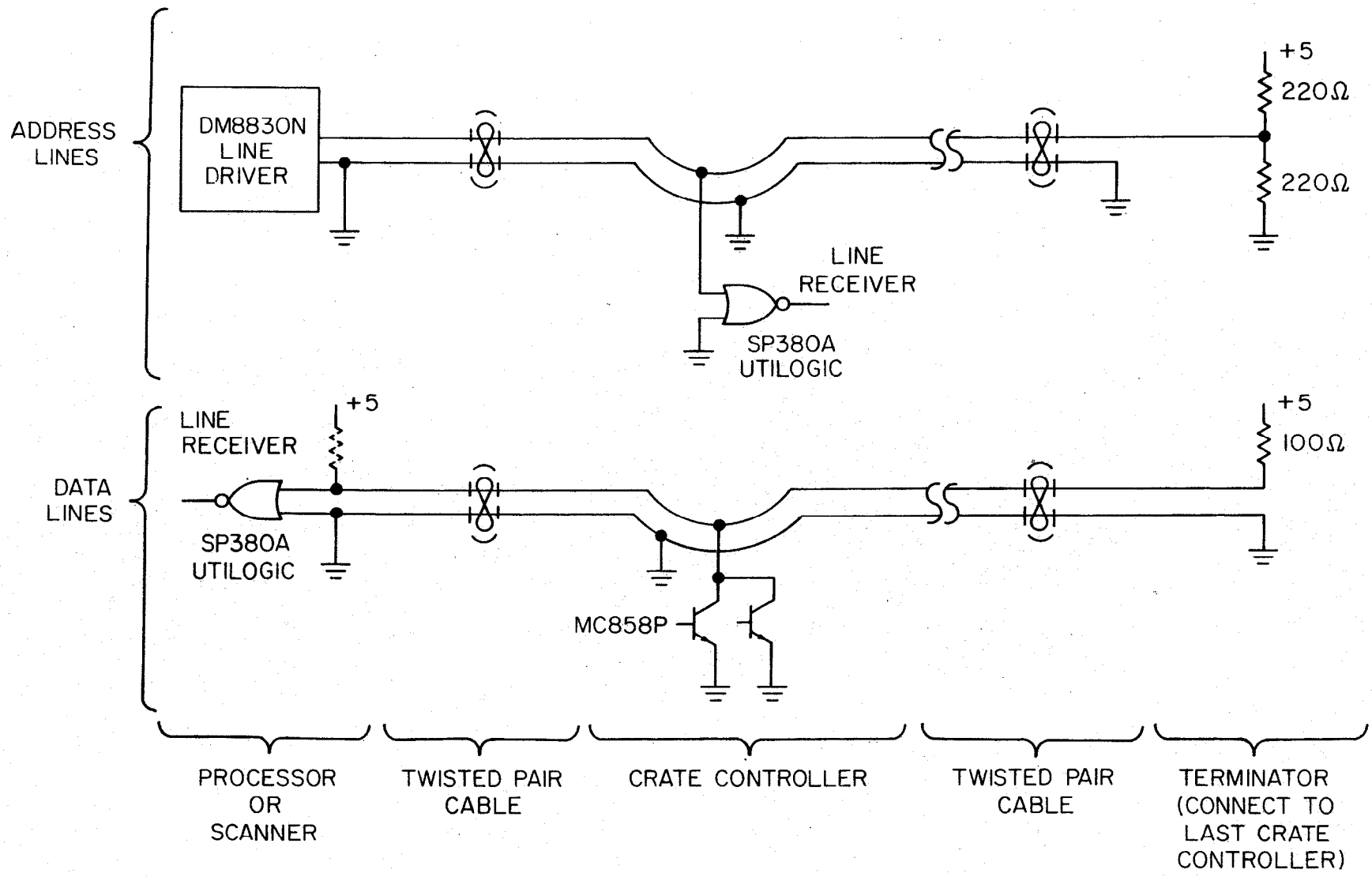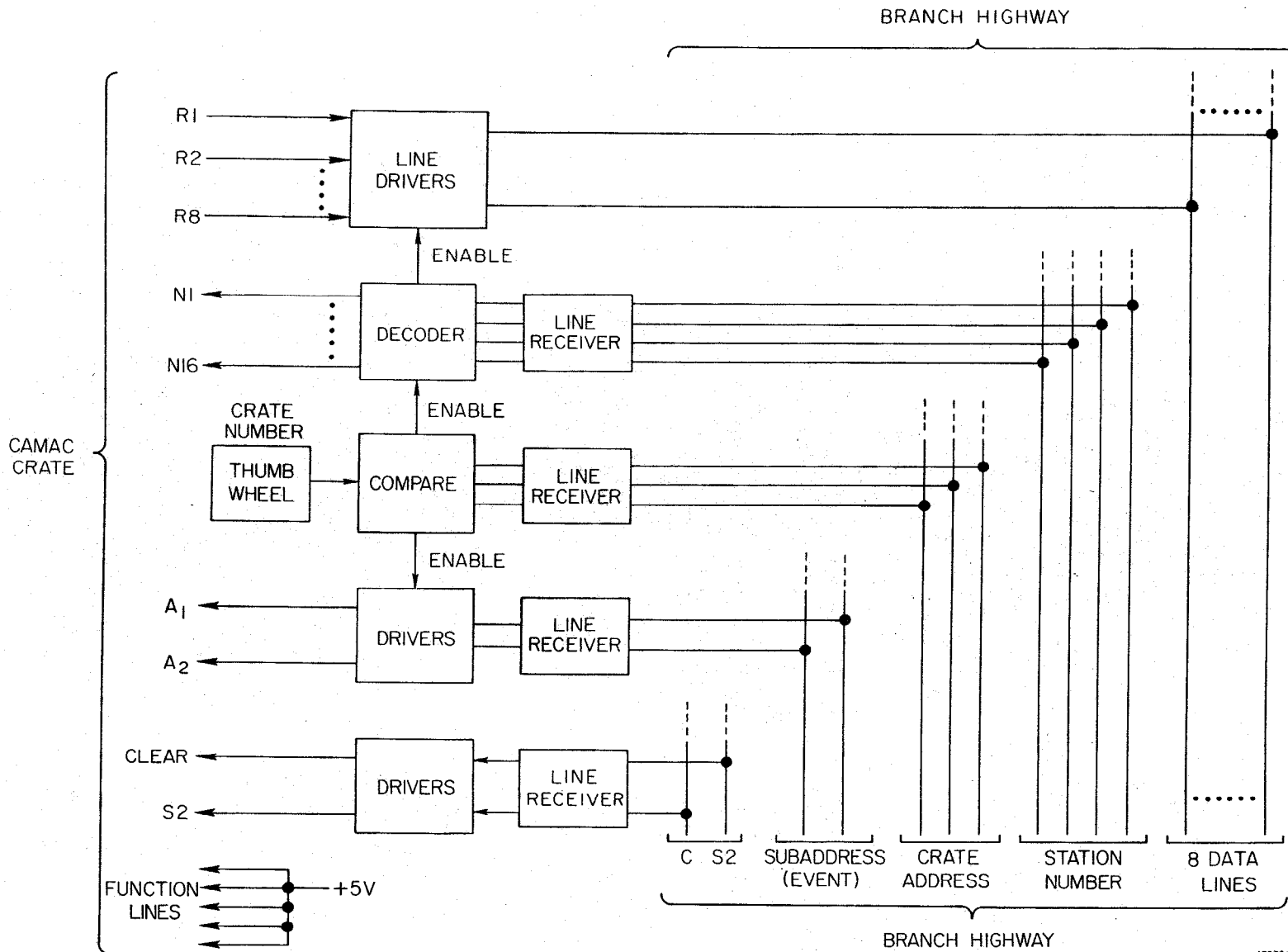FIG. 10--Photograph of the octo-4 bit latch module.

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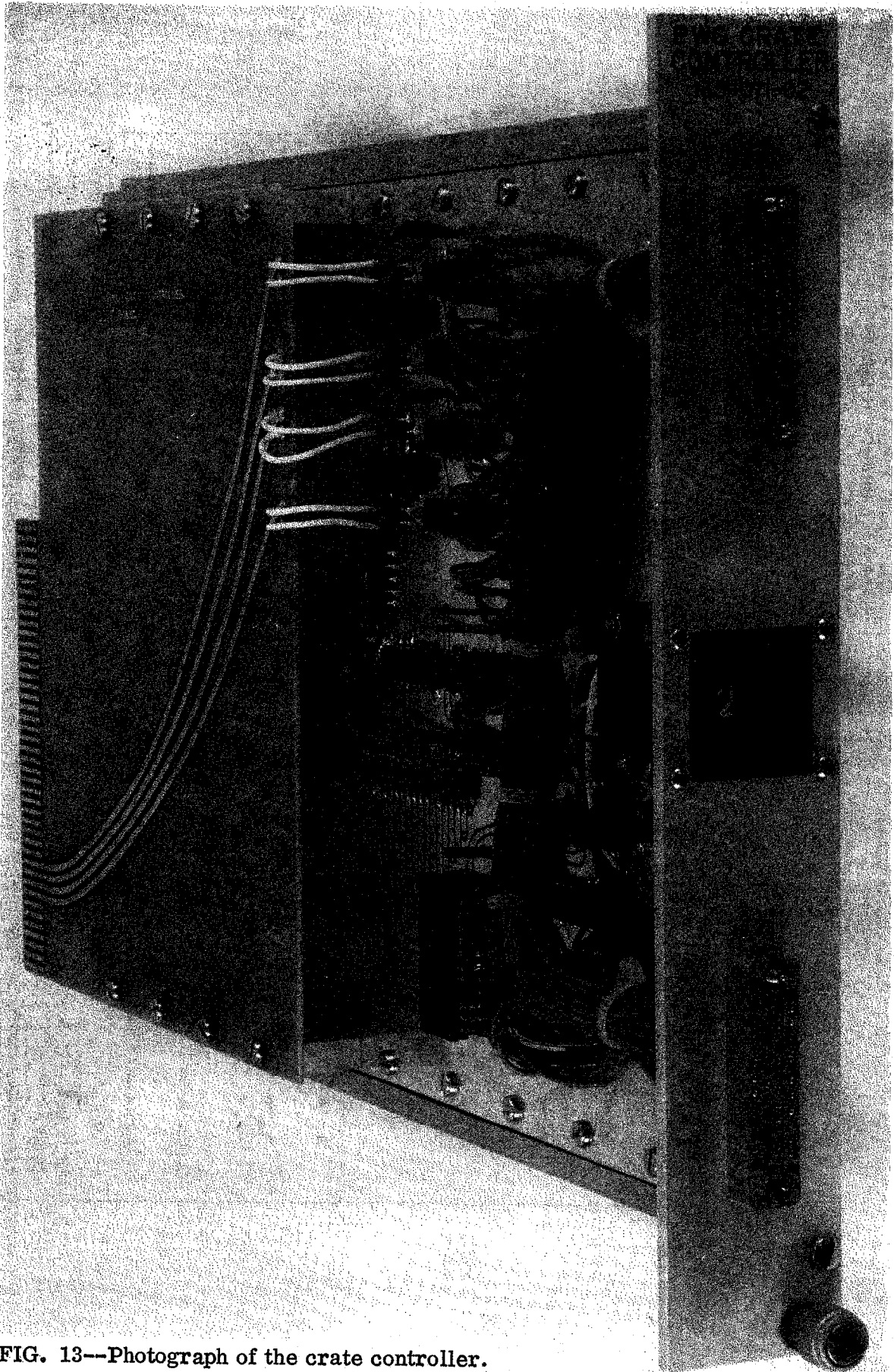FIG. 11--Branch highway line driving concept.

FIG. 12--Crate controller block diagram.

FIG. 13--Photograph of the crate controller.

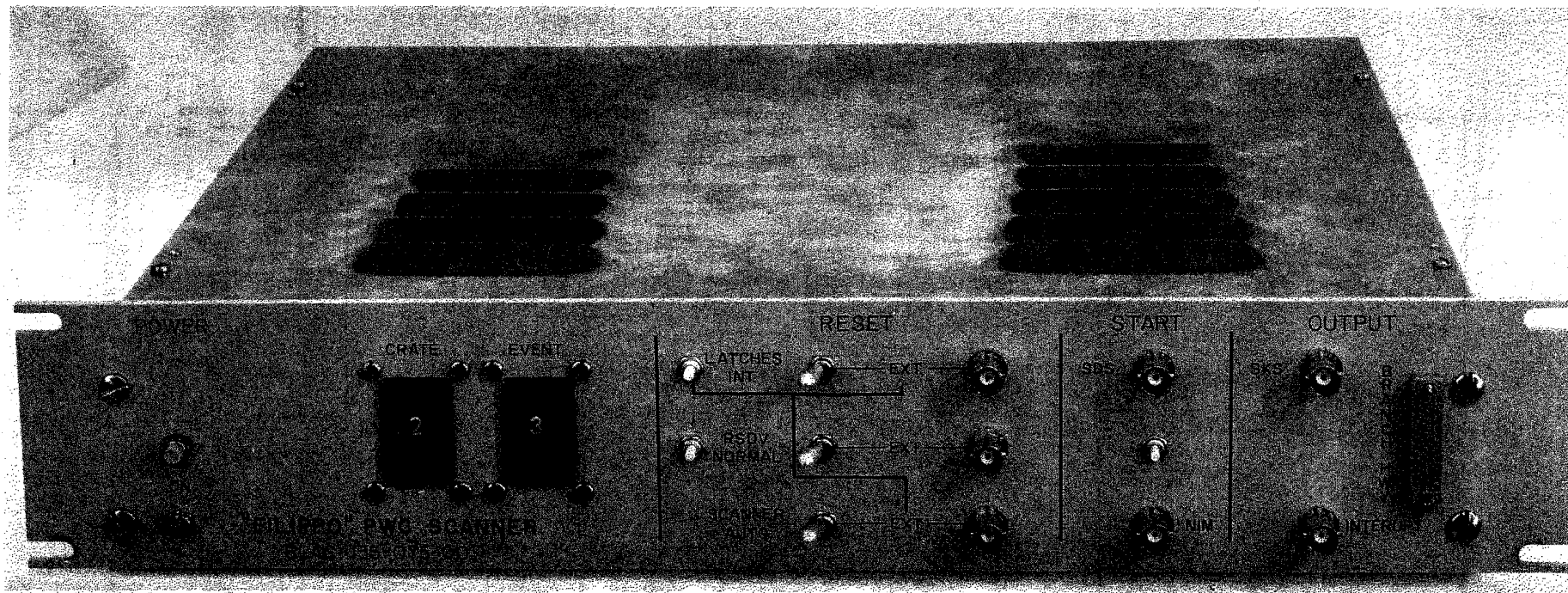1737A16
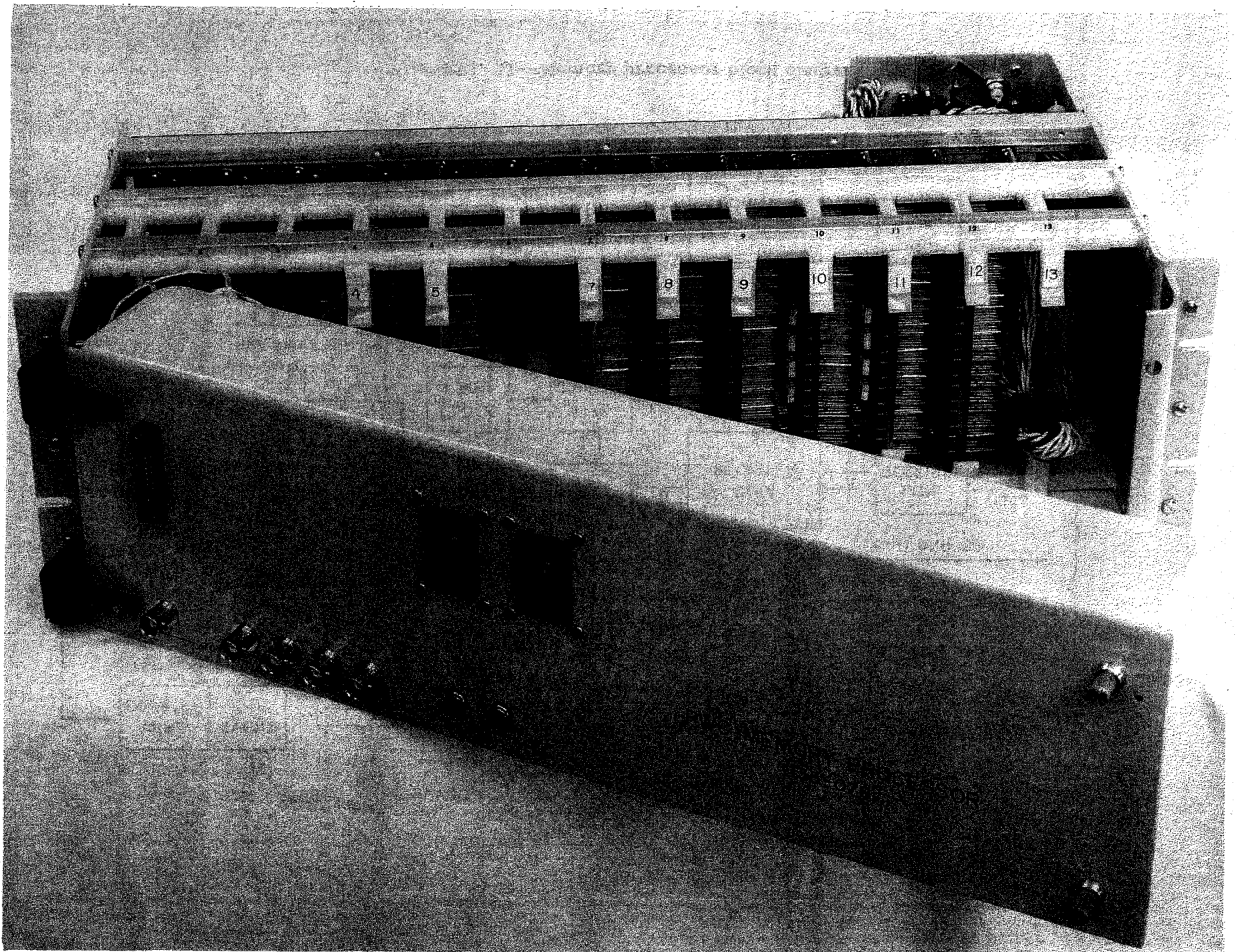
FIG. 14--Photograph of the scanner.

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FIG. 15--Scanner block diagram.

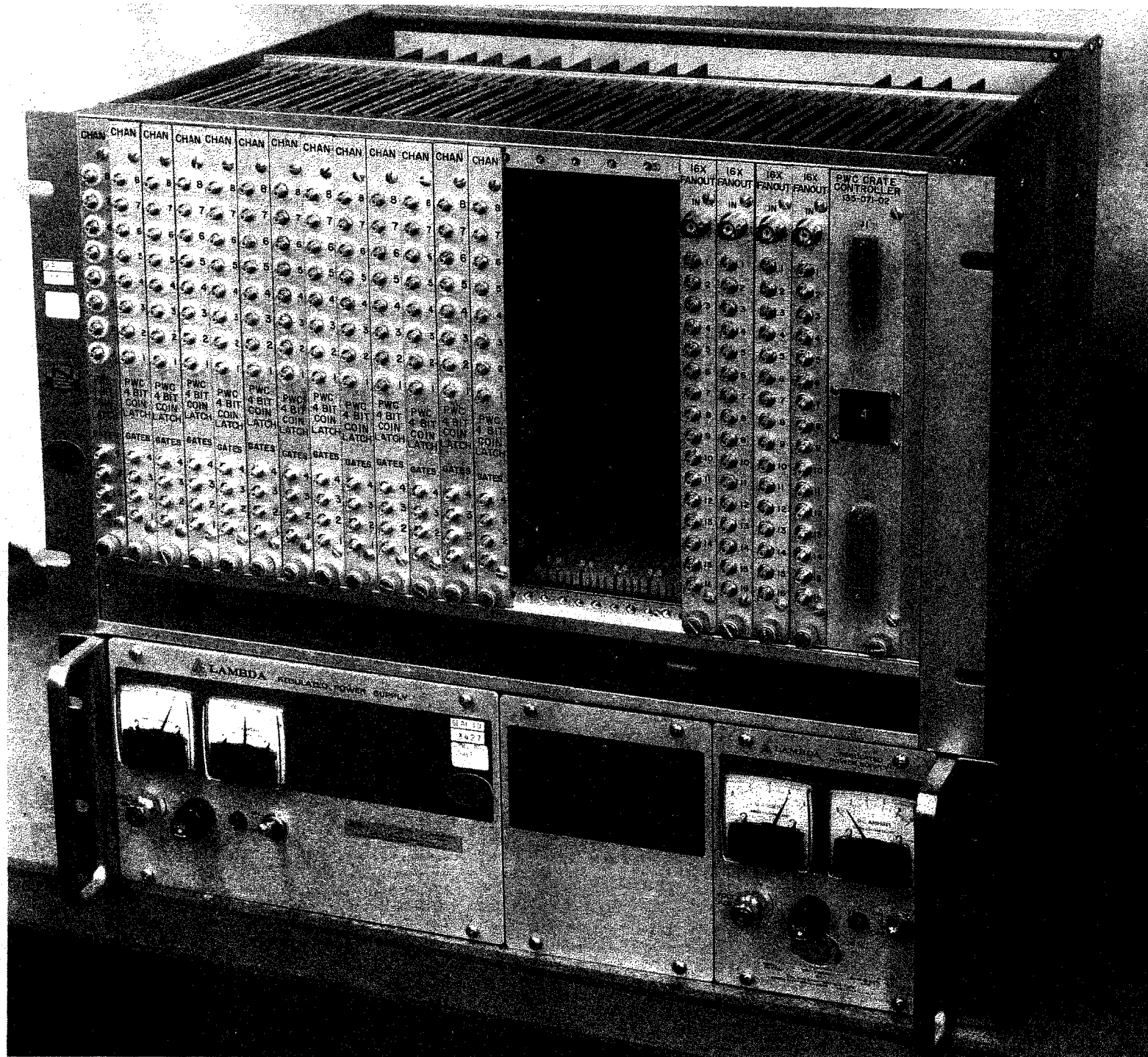FIG. 16--Photograph of memory processor.

FIG. 17--Memory processor block diagram.

FIG. 18--Photograph of crate and power supply.