SLAC-PUB-792
(EXPI)
August 1970

AN ON LINE VIDICON SCANNING SYSTEM FOR RAPID CYCLE BUBBLE CHAMBERS*

R. G. Friday, D. W. G. S. Leith, D. G. McShurley
Stanford Linear Accelerator Center
Stanford University, Stanford, California 94305

(Submitted to High Energy Physics Instrumentation Conference, September 8-12, 1970, Dubna, USSR.)

---

*Work supported by the U. S. Atomic Energy Commission.

AN ON LINE VIDICON SCANNING SYSTEM FOR RAPID CYCLE BUBBLE CHAMBERS

A prototype vidicon scanning system was built to determine the feasibility of using the latest integrated circuits in conjunction with video and computer equipment* to scan and digitize bubble chamber pictures in real time.

The prototype vidicon system divides the picture into a 400 × 437 x-y grid. The x limit is determined by the fact that one vidicon scan line takes 40 μ seconds and the 9 bit scaler is driven at 10 MHz. The y limit is determined by the fact that the vidicon picture consists of two interlaced scans of 437 lines each and the 9 bit y scaler counts only the first scan after the xenon light flash. The x and y scalers then form an 18 bit computer word representing one point of a bubble chamber track. The PDP-9 computer and display scope controller have the same 18 bit data format which allows us to test the system without using the computer by driving the display system directly from the vidicon system.

A buffer is required to measure the vertex of two tracks and to maintain high track densities. The I/0 operation of our PDP-9 takes approximately 3 μsec requiring a buffer holding register for each point within any 3 μsec period. One vidicon scan line takes 40 μsec allowing the computer to read 13 points per scan and maintain the frame rate of 16.7 msec. Most of the image on the face of the vidicon has decayed in 33.3 msec.

A brief calculation of probable data rates indicates the need for a mass storage device and preprocessing. One view of 13 hits/line requires a core of 5681 words, clearly requiring a mass storage device. Even a fast 75-inch per second, 800 bytes per inch, magnetic tape unit will record only 20,000 words per second or one frame in 280 msec.

---

[*] A Digital Equipment Corporation PDP-9 computer and a high resolution General Electric Co. 875-line per frame video camera were used.

Therefore, it appears reasonable that the system be required to do preprocessing to determine if a particular event should be recorded.

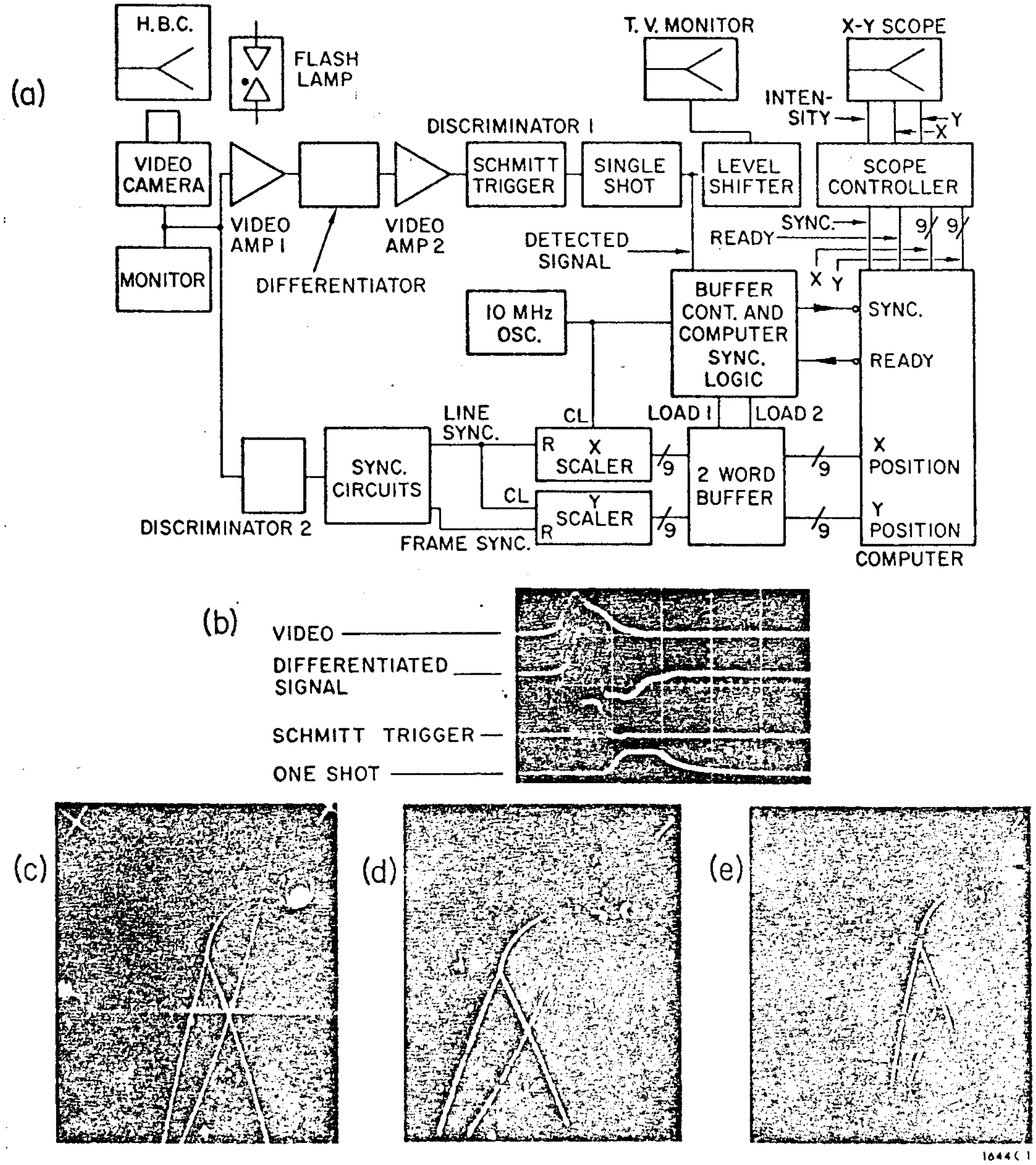
The two video amplifiers, differentiator, Schmitt trigger, and single shot in the block diagram (Fig. 1a) provide the discriminated video signal and the detected bubble signal to the control logic. The center of the pulse is determined by a zero crossing technique. The signals are shown in Fig. 1b. Since the video input voltage is about +0.5 volts and the video amplifiers have a gain of about 50, the input signals are divided down to keep the signal levels at approximately ±0.5 volts maximum at the output of video amplifier 2. Video amplifier 1 is a buffer amplifier which drives the differentiation network. Video amplifier 2 buffers the differentiated pulse and drives the Schmitt trigger, which is set to turn on at +0.1 volts and off at 0 volts. This trigger turns the single-shot on as the differentiated signal crosses zero which corresponds to the center of the video pulse. The 100 nanosecond single-shot pulse drives the buffer control logic and the level shifter which provides the discriminated video signal to the monitor.

Discriminator 2 and the sync circuits determine the line and frame sync pulses. The line sync pulse resets the x scaler and advances the y scaler. The frame sync signal resets the y counter. The first clock pulse after the detected signal, loads the x and y position into the input word of a two word buffer. The next clock pulse shifts this new x and y position to the output word and gives the computer a sync pulse provided that the computer has read the previous output word. If the computer has not read the previous word then the new word is transferred to the buffer output on the clock pulse after the computer is free. At the end of the frame, the computer is given an interrupt which causes the computer to output the data to the scope controller. The scope controller is two nine-bit digital to analog converters which position the point on the x-y scope and several single-shots which control the data channel operation. For testing without the computer a fast 20 in./μsec Hewlett Packard Scope is used which can keep up with the vidicon.

A test wire of 18 micron diameter has been mounted, simulating a straight track in a 15" HBC, and the resulting signal has been easily detected. The present x-y grid limits the position accuracy to approximately 850 microns for a 15" HBC allowing the length of a 1 cm muon track to be measured to about 10%.

A bubble chamber picture, Fig. 1c, was projected life-size on a screen and scanned with the video system. Figure 1d shows the TV monitor display of the reconstructed zero crossing signal. Figure 1e shows the completely reconstructed picture on the x-y scope.

In addition we have made preliminary tests using a solid state vidicon* having a target array of 750,000 photoconductive silicon diodes. These tests indicate that the high sensitivity and reduced blooming provide increased definition. To take advantage of the increased definition a faster clock and additional buffer words will be required.



---

*RCA developmental type C23136A.