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(ACC)

ACCELERATOR COMPUTER SECTOR MEMORY*

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Introduction

The accelerator control system (RCS) has been implemented using telephone relays. A control signal is encoded in CCR and transmitted to a selected sector by means of looped cable pairs. The sector is selected (seized) by a long haul pair routed directly from CCR to each sector. Each sector can be controlled from one of three switched sector panels (SSP) or by the computer, a DEC PDP9. Computer commands are sent to a sector utilizing the Switched Sector Panel No. 3 wire pairs. A control signal must be held for 100 to 200 msec to insure operation of the controlled circuit. The access time is limited now by the present relay system. The computer-sector access time could be reduced to approximately 50 μsec if a solid state system were available between the computer and the sector equipment. The sector memory is the first step in this direction.

Sector Memory Requirements

A prototype unit has been designed to be inserted between the wire pairs entering a sector and the sector remote control decoder. This equipment has the following features:

1. 48 volt/24 volt compatibility. CCR signals are sent at a 48 volt level. The sector receiver requires between 24 to 48 volts input for operation. A differential discriminator (modified XOR) assures that each pair is transmitting a signal. A summing circuit assures that all pairs are coded.
2. A fast storage memory register for 7 control pairs and 3 sub-device pairs is loaded if the equipment is not busy. (The sub-device pairs make "stretch" commands or extra device selection available.)

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3. An acknowledgement signal is sent to CCR when the command signal has been loaded into the fast storage register.
4. Control signals from SSP Nos. 1 and 2 are disconnected while executing a command signal. (SSP No. 3 is disconnected by the computer.)
5. A time delay allows the RCS decoder relays to relax before a new command is executed.
6. A pulse generator produces an execute signal for 0.1 seconds minimum or for 0.1 seconds after the command signal is turned off.
7. If the same command signal is sent again before the execute signal ends, the decoder relays are held for an additional 0.1 second.
8. If a different command signal is sent before the execute signal ends, it is ignored until completion of the present command.

The requirements of this system can be expressed more precisely by the following definitions and logical equations:

C_P is the control pair signal

C1 - C6 denotes looped pair signals

$SD_{0,1,2}$ is the subdevice pair signals

SS denotes the sector seize signal

S is defined as the command signal exists.

$$S = C_p \cdot C_1 \cdot C_2 \cdot C_3 \cdot C_4 \cdot C_5 \cdot C_6 \cdot (SD_0 \cdot SD_1 \cdot SD_2) \cdot SS \qquad (1)$$

P_0 is the loading pulse for the fast storage register

F is the free state of the free/busy FF

$$P_0 = S \cdot F \qquad (2)$$

A is an acknowledgement signal sent to CCR indicating that the storage register is loaded.

Same is a signal which indicates agreement between the storage register and the command signal.

$$A = \text{Same} \tag{3}$$

T_1 is a time delay to allow the decoding relays to relax.

D is the execute or drive signal

K_3A is a signal which disconnects control by SSP1 and SSP2

$$K_3A = S + D + T_1 \tag{4}$$

Δ denotes a change of state

K_1, K_2 are seizing relays for SSP1 and SSP2

$$T_1 = \Delta\overline{K}_1 \cdot \bar{K}_2 + \bar{D} + T_1 \text{ delay} \tag{5}$$

B is the busy state of the busy/free FF

$$D = B \cdot \bar{T}_1 \cdot \bar{K}_1 \cdot \bar{K}_2 + \text{Same} \cdot D + D \cdot \text{Delay} + D(SD_0 + SD_1 + SD_2) \tag{6}$$

$\overline{XOR}$'s is the complemented product of each comparison circuit

$$\text{Same} = S \cdot \overline{XOR}\text{'s}$$

K_3 is a relay signal that connects the execute signal to the decoder relays

$$K_3 = D \tag{8}$$

$$(\text{Set B}) = \text{Same} \tag{9}$$

$$(\text{Set F}) = \bar{T}_1 \cdot \bar{D} \cdot \overline{\text{Same}} \tag{10}$$

Sector Memory Circuitry (Ref. Fig. 1 and 2)

The seven loop pairs are filtered as they enter the sector memory. The filter attenuates any high frequency transients and reduces the -48 volt input signals to -5 volts for application to the W500 Emitter follower level shifters. The output of these circuits is either 0 or -3 volts which are standard DEC levels.

The signals are next applied to exclusive OR (XOR) circuits. These circuits assure that each input pair has the proper coding (one wire must be at OV and the other must be greater than -30 V. Both at OV or both at -48 V is not allowed.) If each pair passes this check, the signal is applied to the input gate of a flip flop (Fast Storage register). The loading pulse is generated if all signals pass the coding check and all are present to form signal S and the equipment is not busy executing a previous command. S is generated if and only if the 7 control pairs, the three subdevice pairs, and the sector select pair appear at the input of the S Gate.

The signal polarity on each of the 7 looped pairs is compared with the polarity of each fast storage register (FF). If these signals are the same, Same and Diff. signals are generated. Same also requires an S signal.

If an S signal is present and the free/busy FF is F (free), a load pulse P_0 is generated which stores the command from the 7 looped pairs and the three subdevice pairs in the appropriate Fast Storage registers. An "acknowledgement" signal is sent back to CCR when Same appears.

When the RCS Receiver control relays (K_1 and K_2) are relaxed, time delay T_1 is started. This delay is adjustable over a range of .1 to .5 seconds to allow the decoder relays to relax.

As soon as T_1 has timed out, and the busy/free FF is busy (set by Same), the decoder drive pulse D is started. This pulse is adjustable from .1 to .5 seconds. This signal enables the output relay drivers and the receiver relay K_3 which connects the command stored in the storage registers to the decoder relays. The D circuit contains a rechargable "one shot" so that the period can be extended if the same command is sent again.

When D has finished, T_1 is again enabled to allow time for the decoder relays to relax. This is necessary if a SSP had previously been connected to the computer controlled sector and a command is still enabled on that SSP.

The sector memory will accept another command when the busy/free FF is reset. This occurs when T_1 has timed out and the D pulse has finished and the input command has been removed. It should be noted that as long as a command is applied to the input, the execute pulse D will be held. This operation is required because of held manual commands via the SSP. (Subdevice pulses SD_0, SD_1 and SD_2 may also be used to stretch the D pulse.)

SSP Nos. 1 and 2 are inhibited from applying a command if T_1 or D or S are present.

A special XOR was required on the control pair input because of the time coding sequence due to relay contact bounce in CCR. The details of this XOR are discussed in the "Mallory XOR" appendix of this note. Typical timing signals and DEC symbols are also included for reference in the appendix.

Conclusions

A prototype utilizing DEC discrete circuitry has been installed in Sector 16. The operation is essentially transparent to the CCR operator. Acknowledgement circuitry does not exist in CCR yet nor does a computer program exist to utilize this signal. An effective system really requires that a sector memory be installed in every sector. An integrated circuit version is now being constructed which will result in approximately a 50% reduction in price.

Acknowledgement

Dr. K. B. Mallory, head of the Instrumentation and Control group is responsible for defining the initial concepts and suggesting the solution to the contact bounce problem which resulted in the Mallory XOR.

References

1. R. B. Neal, Editor, The Stanford Two-Mile Accelerator (W. A. Benjamin, New York, 1968); pp. 533-534.
2. W. C. Struven, "Control and monitoring of the SLAC accelerator utilizing a PDP9 system," Report No. SLAC-PUB-592, Stanford Linear Accelerator Center (April 1969).

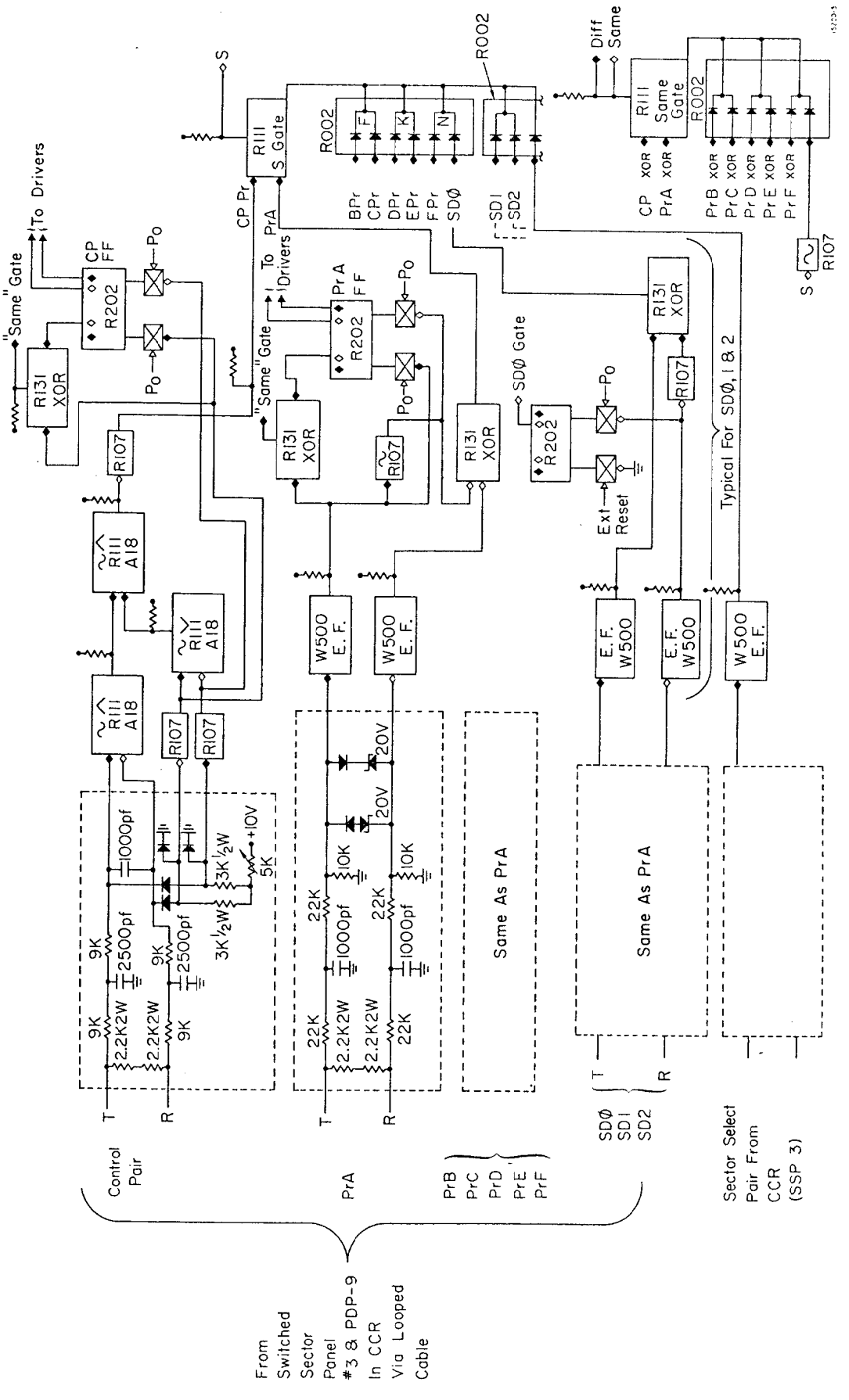

From Switched Sector Panel #3 & PDP-9 In CCR Via Looped Cable
Control Pair
PrA
PrB PrC PrD PrE PrF
SDØ SD1 SD2
Sector Select Pair From CCR (SSP 3)
Same As PrA
Typical For SDØ, 1 & 2
"Same" Gate
To Drivers
CP FF
R202
R131 XOR
R111 A18
R107
W500 E.F.
R111 S Gate
R111 Same Gate
R002
SDØ Gate
Ext Reset
CP Pr
To PrA Drivers
PrA FF
BPr CPr DPr EPr FPr SDØ
SD1 SD2
CP XOR PrA XOR
PrB XOR PrC XOR PrD XOR PrE XOR PrF XOR
Diff Same
9K
2.2K2W
2500pf
1000pf
3K ½W
+10V
5K
22K
10K
20V
R107

Fig. 1

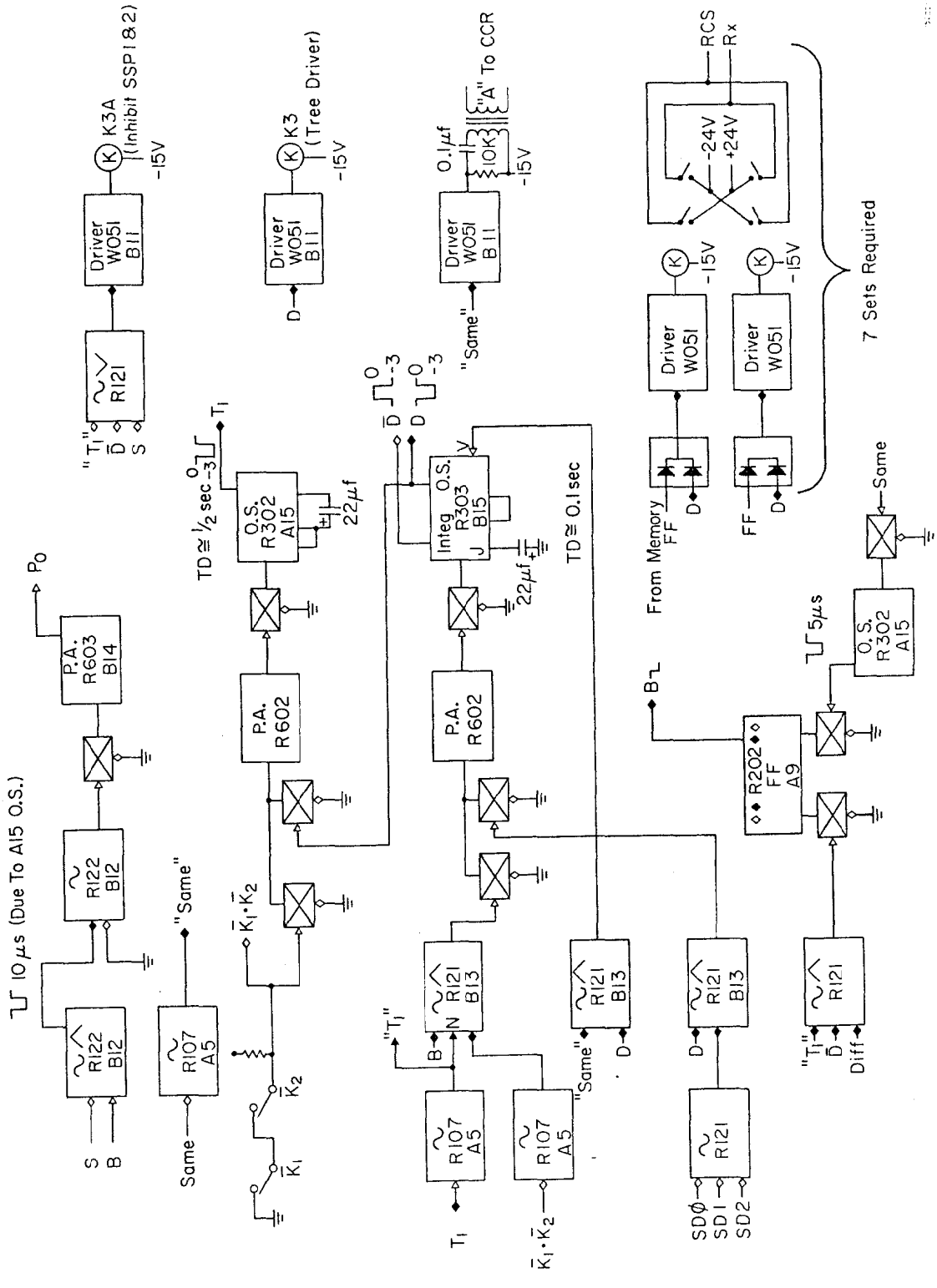

P.A. R603 B14
R122 B12
R122 B12
S
B
10 μs (Due To A15 O.S.)
P0
R107 A5
Same
"Same"
K1 · K2
K2
K1
P.A. R602
O.S. R302 A15
TD ≅ ½ sec
T1
22μf
R121 B13
T1
R107 A5
K1 · K2
"Same"
R121 B13
D
R121 B13
SDØ
SD1
SD2
R121
"T1"
D
S
R121
K3A (Inhibit SSP1&2)
-15V
Driver W051 B11
K3 (Tree Driver)
-15V
Driver W051 B11
D
D
-3
D
-3
"Same"
Integ. O.S. R303 B15
22μf
TD ≅ 0.1 sec
P.A. R602
0.1μf
10K
"A" To CCR
-15V
Driver W051 B11
B
From Memory FF
Driver W051
-15V
FF
Driver W051
-15V
RCS
Rx
-24V
+24V
7 Sets Required
R202 FF A9
5μs
O.S. R302 A15
Same
"T1"
D
Diff
R121

Fig. 2

APPENDIX A

Conventional XOR

Typical exclusive OR circuits can be expressed by the following equations:

$$f = \bar{A}B + A\bar{B} \qquad \text{(expressed as Simplest Sum of Products)}$$

or

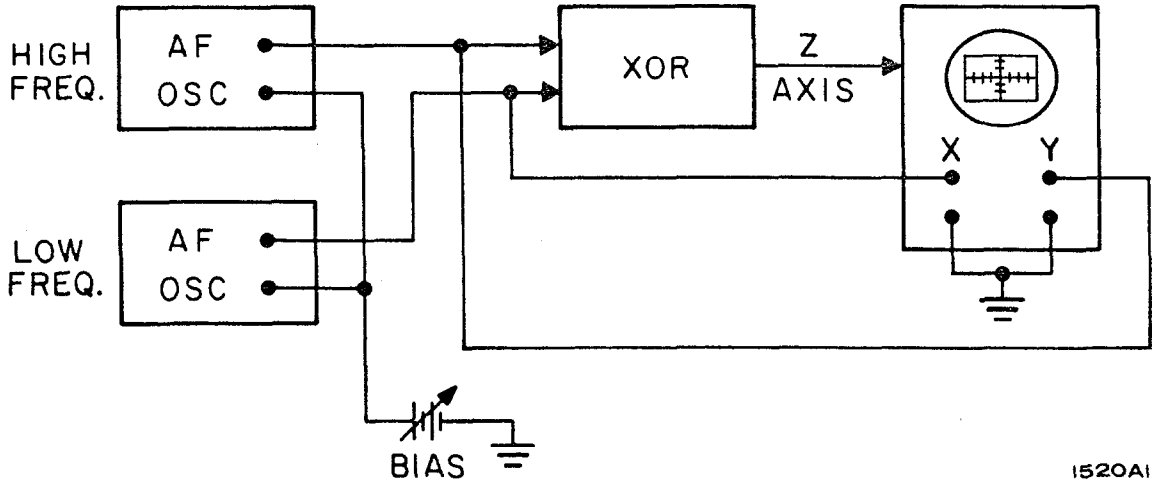
$$f = (\bar{A} + B) \cdot (A + \bar{B}) \qquad \text{(expressed as Simplest Product of Sums)}$$

These circuits produce a logic "1" output if the inputs are the same and a logic "0" output if the inputs are different.

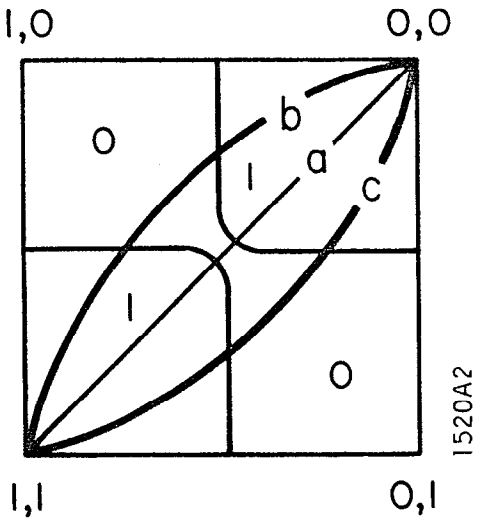
For the DEC R131 XOR; like inputs produce a -3 V output, different inputs produce a 0 V output.

In the R131, transitions between unequal inputs have a relatively short settling time, but transitions between equal inputs may produce transients to ground lasting 250 nsec or more.

This can be shown graphically by implementing the following circuit.



The circuit allows a visible Venn diagram to be displayed. The R131 DEC XOR produces a picture as follows:

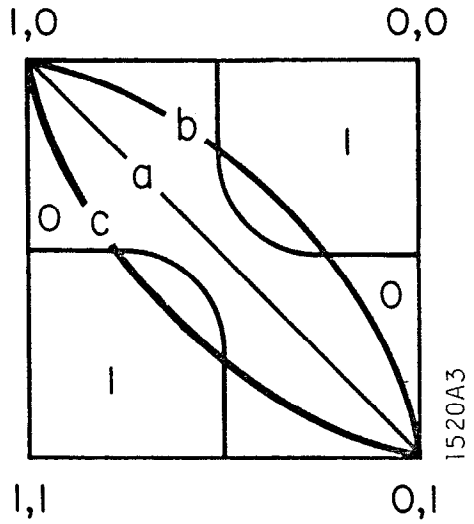


The 0,0; 0,1; 1,0; and 1,1 areas at the edges represent inputs. The regions labelled 0, 1 inside the square represent output levels.

Transitions between equal inputs

The path a would be followed if the risetime of both input signals were exactly the same. Lines b and c portray two paths of a family of curves when risetimes are unequal and are switched from 0, 0 to 1, 1 or vice versa.

If the inputs are unequal and are switched to their complements, the following picture is observed:



Transitions between unequal inputs

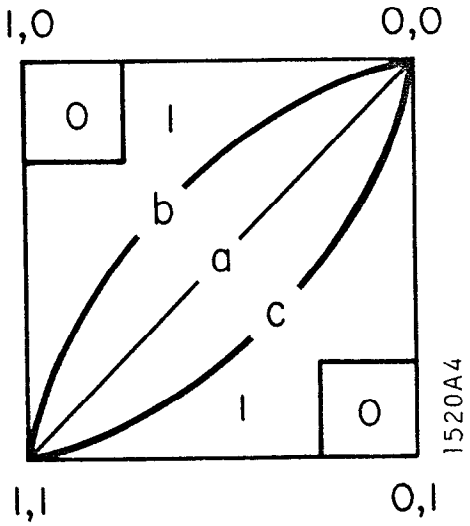
Path a shows the route of the transition with equal rise times or circuit delays on the two input pulses. Paths b and c show the effect when rise times or circuit delays are unequal resulting in multiple outputs as the curve crosses from a "0" output area to a "1" output area and back to "0" output area.

In the case of an R131 XOR, the "hole" between the two "1" regions is approximately 40 mV wide, therefore, the chance of following path a is rather small.

Mallory XOR

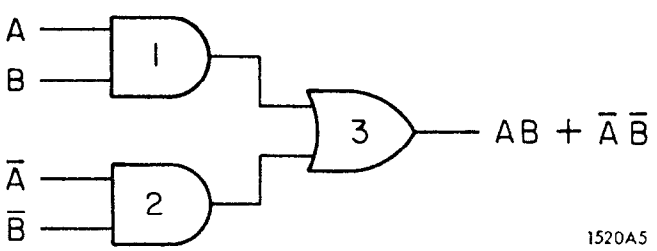
The unique feature of this XOR is the lack of transients in its output during a transition between equal inputs.

If a circuit can be constructed which has the following Venn diagram, transitions between equal inputs can be almost completely eliminated.



It is noted here that paths a, b, and c will not cause output transients to occur, however, transitions between unequal inputs are guaranteed. This latter effect is of no importance in the sector memory application, as shown by the following example.

If we start with the general form of a coincidence circuit as follows:



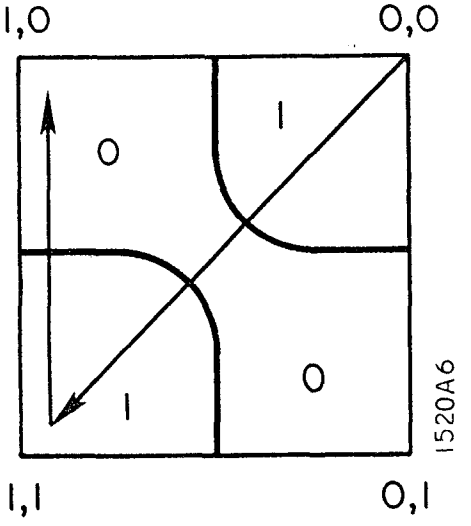
A	B	$\overline{XOR}$
0	0	1
0	1	0
1	0	0
1	1	1

and modify the inputs $\overline{A}$ and $\overline{B}$ so that they are attenuated with respect to the signals applied to A and B, a three-state circuit is obtained rather than a normal two-state circuit. The effect is to cause gate 1 to AND and produce a stable output to the OR Gate before gate 2 operates.

The control pair to a sector from CCR typically has the following time-sequence coding:

time (msec)	0	10	20
Conductor A	0	1	1
Conductor B	0	1	0

If this sequence is applied to an R131 XOR the path is as follows:

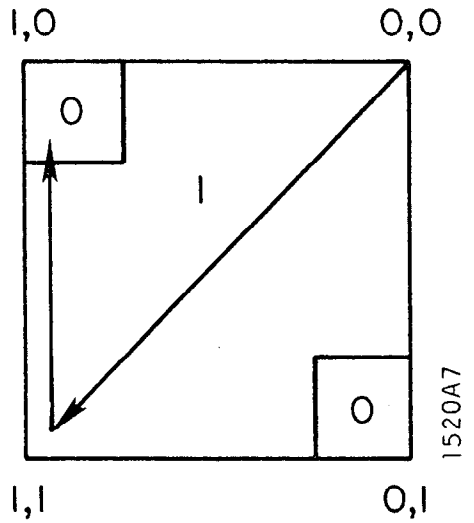


The resulting time truth table is as follows:

Input	0	1	1	→
	0	1	0	→
Output	1	0	1	0 →

time →

If this sequence is plotted for a Mallory XOR the following plot and time truth table is observed:



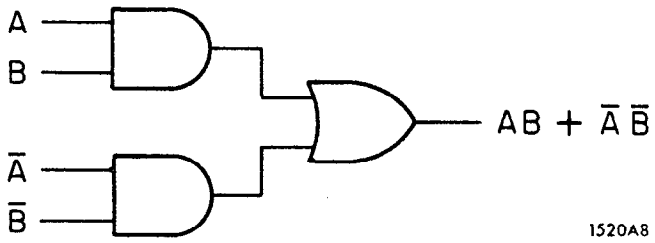
Input	0	1	1	→
	0	1	0	→
Output	1	1	0	→

time →

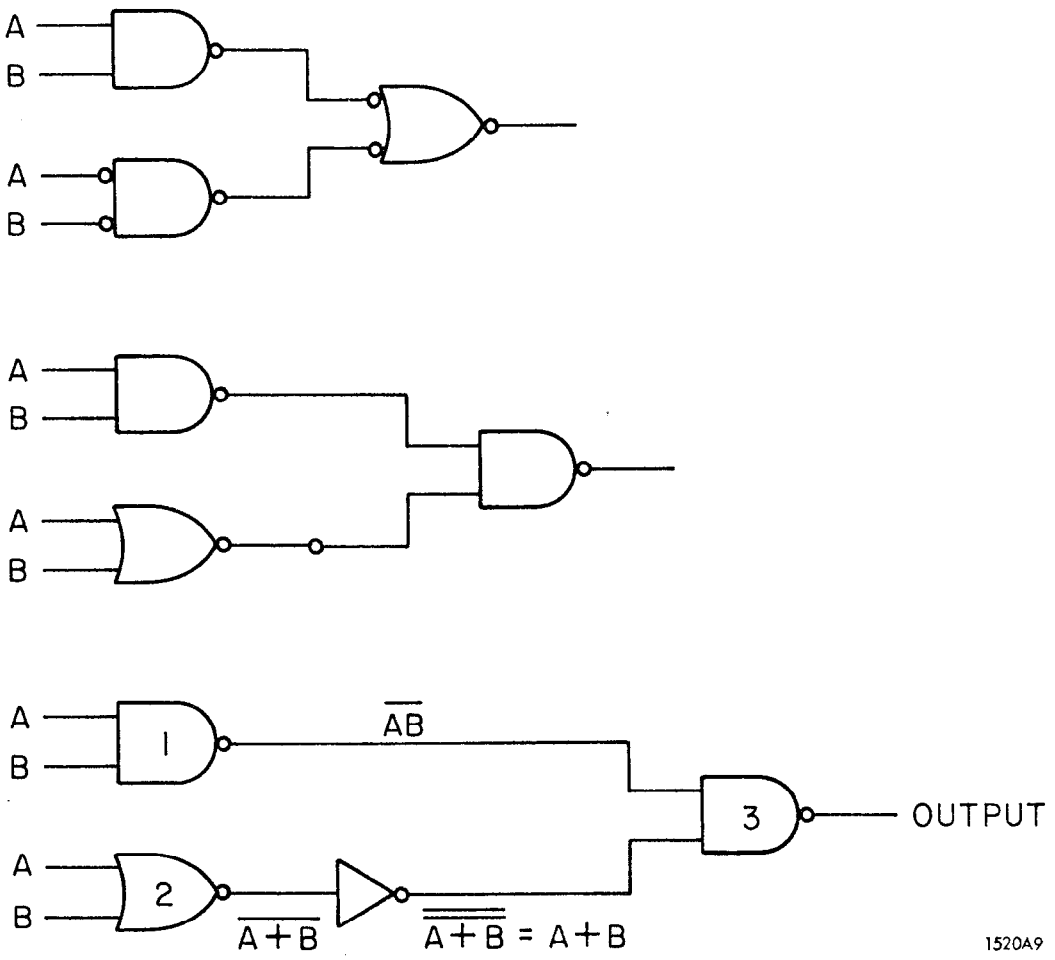
In the first case a 1, 0, 1, 0 transition is observed, whereas in the second case a clean 1, 1, 0 transition is obtained.

Implementation of the Mallory XOR

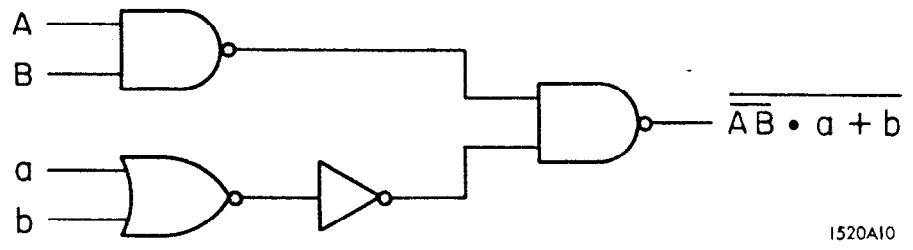
The basic coincidence circuit for reference can be shown as follows:



To implement this circuit in DEC logic requires a conversion to NAND/NOR logic and provides three of the following steps:



If we attenuate the input to the NOR Gate (No. 2) we obtain the Mallory XOR used in the Sector Memory. The circuit is then as follows:



The output can then be expressed as follows:

$$\overline{\overline{A\bar{B}} \cdot a+b}$$

$$= \overline{\overline{A\bar{B}}}+\overline{(a+b)} \qquad \text{using DeMorgan's Theorem}$$

$$= AB+\bar{a} \cdot \bar{b} \qquad \text{which is the coincidence form.}$$

If the output is followed by a single inversion we obtain:

$$\overline{AB+\bar{a} \cdot \bar{b}}$$

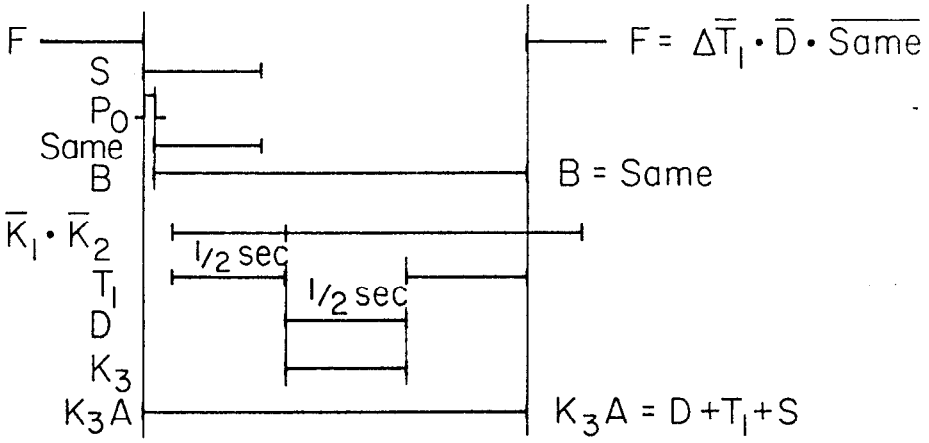
$$= \overline{AB} \cdot \bar{\bar{a}}\bar{\bar{b}}$$

$$= \bar{A}+\bar{B} \cdot a+b$$

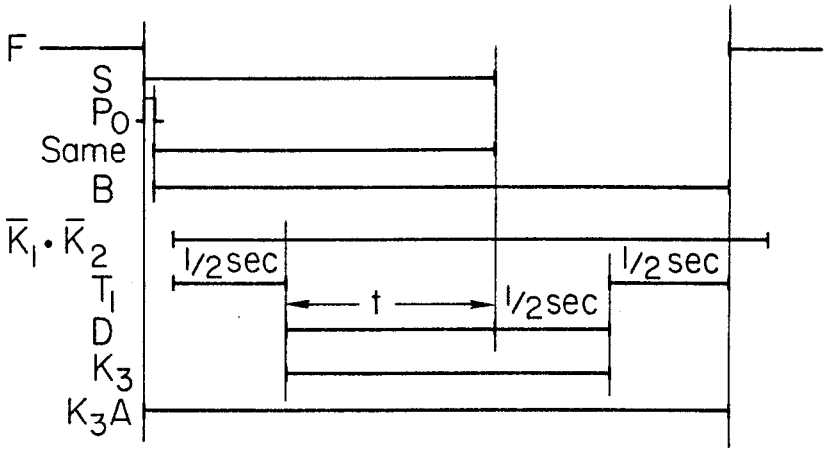
$$= \bar{A}(a+b)+\bar{B}(a+b)$$

$$= \bar{A}a+\bar{A}b+\bar{B}a+\bar{B}b$$

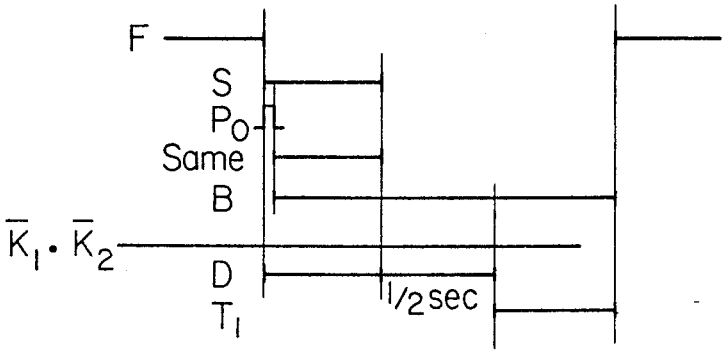
$$= \bar{A}b+\bar{B}a \qquad \text{which is the Simplest Sum of Products for an XOR.}$$



Timing Diagram If SSP 1 or 2 Has Previously Selected This Sector And Command Is Momentary.



Timing Diagram If SSP 1 or 2 Has Previously Selected This Sector And Command Is Held For Time t.



Timing Diagram If Computer Can Select Sector And Initiate A Command Immediately.

SECTOR MEMORY TIMING

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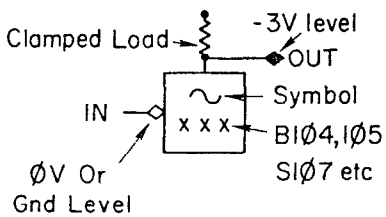
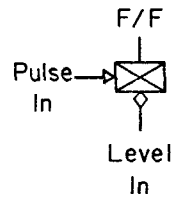
APPENDIX C

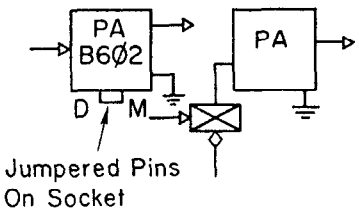
INVERTER



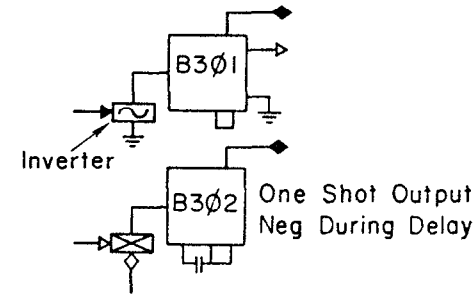
DCD GATE



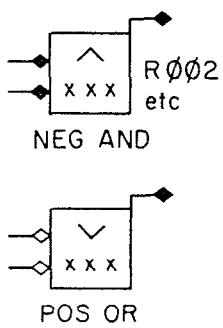
PULSE AMPLIFIERS



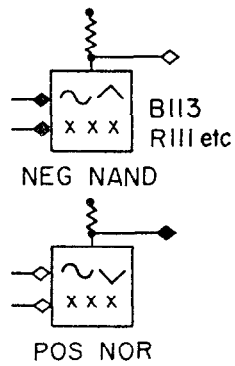
DELAYS



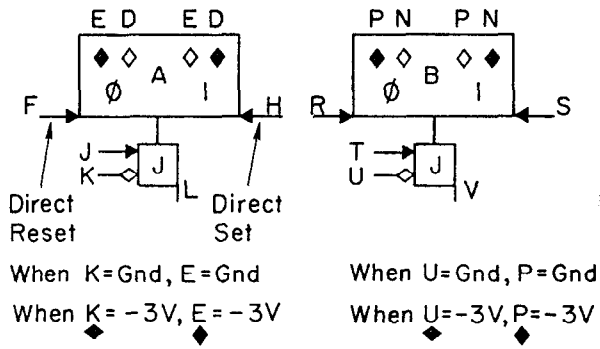
DIODE GATE



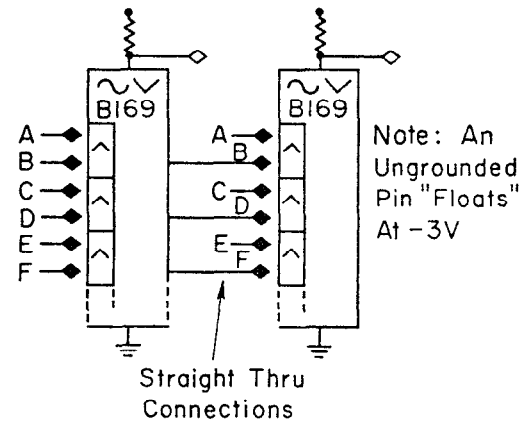
NAND/NOR



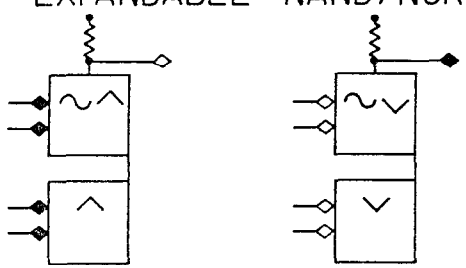
FLIP FLOP B 213



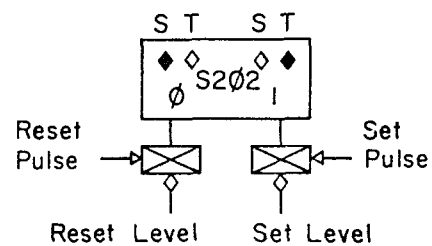
MIXERS



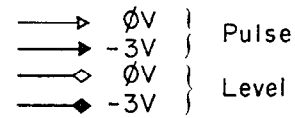
EXPANDABLE NAND/NOR



FLIP FLOP



Note: When A -3V Signal Is Paralleled With A ØV Signal, The ØV Signal Survives



152C012