(Presented at the 12th Scintillation and
Semiconductor Counter Symposium,
Washington D.C., March 11-13, 1970)

SLAC-PUB-726
(EXPI) and (EXP)
August 1970

A WIRE SPARK CHAMBER SPECTROMETER WITH A CAPACITOR MEMORY AND FET READOUT*

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Summary

A 20-plane wire chamber spectrometer utilizing capacitors as memory elements and suitable for operation in a magnetic field is described. The (parallel) wire planes are separated by ~1 cm. The active areas of the chambers range in size from 120×120 cm^2 to 200×240 cm^2. The wire separation is 1 mm. Each readout wire is connected to a separate capacitor resulting in a 30 K-bit memory for the total system. Using FET's as gates, the capacitors are read out in 32 bit words. These words are formatted into data sets of 18 bits/spark and transferred to a PDP-9 computer. Digital processing of data is briefly described, including the computer interface and test procedures. Advantages of this system are discussed together with some performance characteristics.

Introduction

We report here on the design and construction of a wire chamber spectrometer with large acceptance (Fig. 1) to be employed at SLAC to study neutral K decays and interactions.

Two primary constraints were imposed on the spectrometer design: one by the magnet, and the other by the poor duty cycle of the linac.

In order to obtain the maximum possible spectrometer acceptance, it is necessary to use a large magnet, 2.5 m × 1 m × 1m gap in this case, and to place the chambers in its fringing field. Conventional magnetostrictive and core readout chambers can be made to operate in a magnetic field, but their multitrack efficiency can be termed as marginal under these circumstances. Furthermore, any influence of the magnetic field on the readout could introduce serious systematic errors in the data. To overcome this problem we decided to adopt a novel readout method which is unaffected by any achievable magnetic field.

The basic idea, conceived by Neumann and Nunamaker,[1] is to connect each readout wire to ground through a capacitor. A charge flows into it if its wire is hit by a spark. The capacitors are then read out through FET gates. Since the FET's have low leakage currents, there is enough time (several ms) to read out the 30 K spectrometer wires serially.

The second major requirement is for a high multitrack efficiency. The reason for this is that SLAC has a poor duty cycle δ. The beam comes in 360 pulses/s, each pulse being 1.6 μs in duration, so $\delta \simeq 6 \times 10^{-4}$. Since the time between the actual event in the spectrometer and application of high voltage to the chambers is a significant fraction of the beam pulse width (~ 350 ns), clearing fields cannot be used effectively during a pulse. Consequently, an average trigger may contain several extraneous tracks in addition to the desired event tracks. The upper limit on event rate is set by the ability to sort out the events of interest from all of the tracks taken with the event. Sparks missing from either the tracks of interest or the spurious tracks make this separation more difficult.

To achieve a high multi-track efficiency great care was taken in the design of the high voltage pulsing system. The major points are listed below:

1. The high voltage is applied to the chambers by discharging delay lines through a hydrogen thyratron.[2]
2. Resistors are placed in series with each high voltage wire to limit the current in any spark.
3. Each readout plane has a separate high voltage plane, with wires running parallel to those in the readout plane.

Mechanical Construction

The spectrometer consists of two groups of spark chambers and a horizontally deflecting dc magnet. The first group of chambers, situated upbeam of the magnet has ten readout planes, four x, four y, and two slanted planes for ambiguity resolution. The coordinates of the slanted planes are denoted by u and v. The upbeam aperture is limited by that of the x-y plane which is 1.2×1.2 m^2. The second group, downbeam of the magnet has a similar arrangement except that the horizontal aperture is larger (2.4 m).

Each of the 20 chambers consists of two planes of parallel stretched wires with separated functions, either high voltage or readout. The gap between planes is about 1 cm, and the wire spacing in a plane is about 1 mm. By making parallel wire chambers we eliminate the pulse propagation problems inherent in crossed wire chambers. Hence we expect a high and uniform efficiency. This consideration is particularly relevant to our large 1.2×2.4 m^2 chambers.

Three methods of mounting the wires were considered: woven screening, mylar backed wire, and stretched wire. Woven screening was rejected because of the close control needed to obtain the necessary wire positioning accuracy and the difficulty of obtaining wide screening with easily solderable wires. Glueing the

* Work supported by the U.S. Atomic Energy Commission and the Air Force Office of Scientific Research.

This paper has been published in IEEE Transactions on Nuclear Science, NS-17, 50-54, June 1970.

wires to a mylar backing was considered unsatisfactory because of problems arising from the sensitivity of the gap width to fluctuations in gas pressure, and some spurious sparking problems encountered during some early tests. We chose to use the stretched wire technique and have developed a system which provides the rigid frame structure necessary to maintain wire tension, yet enables the gaps to be assembled close together. The requirement for a large winding machine was already solved by the availability at SLAC of a machine capable of handling 4 frames of up to 3×3 m^2 in size.

We have also simplified the manufacture of the relatively large number of chambers by using a modular form of construction (see Fig. 2). Consider, for example, the square 1.2×1.2 m^2 chambers (see Fig. 3). There are two groups of these, each group giving x, y, x, y readout, 8 gaps in all. Each group of 4 gaps is made of 5 modules clamped together with 1 cm thick lucite window frames as gas seals between them. Each module consists of 2.5×10 cm^2 Al bars welded together with fiberglass epoxy boards (G-10) glued to both sides. After glueing, the outside surfaces of the G-10 were ground flat. The 0.1 mm (dia.) Be-Cu wires were wound on the winding machine at about 230 g tension; the modules were then mounted on the machine where the wires were glued (after alignment) to the G-10 surfaces. In order to maintain wire tension after glueing, the modules were pre-stressed by applying a single load (about 70% of the total force exerted by the wires) at the midpoint of the module. After the wires were glued, this load was removed.

In the case of the 1.2×1.2 m^2 chambers, ten identical modules were constructed. After the wires were glued in place, they were optically measured. The measurements are referred to tooling balls which are mounted on the extreme corners of the module mounting lugs where they may be sighted after assembly. The modules were then selected, those having the best wire positioning accuracy being used for readout, the others for high voltage. It is only after this operation that there was any difference in the construction of the individual modules. The wire planes on each side of a module are perpendicular to each other, one plane being half of an x readout gap, the other plane half of the adjacent y readout gap.[3] However, they both serve the same function, i.e., HV and readout planes are not "mixed" on the same module.

The HV wires are soldered in pairs to a printed circuit strip board; each pair of wires is connected through a 500 Ω resistor to a HV bus. The 20 wires at each edge of the plane are connected through a resistor chain to ground to taper the HV field at the edges combating breakdown along the edges parallel to the wires. Breakdown along the edges perpendicular to the wires is prevented by a mylar strip extending about 2 cm into the chamber. To minimize optically induced spurious sparking, sheets of black paper have been installed in the center of each module.

The readout wires are soldered individually to the traces of "fanout" PC boards. Soldering was chosen because of its reliability. These fanout boards are mounted on the backs of the two rows of connectors into which the FET boards are inserted (see Fig. 4). The use of connectors enables easy and quick interchange of readout electronic cards. A sheet metal enclosure provides electromagnetic shielding for the FET boards and their associated cabling.

When the fast logic indicates the occurrence of an event, the chambers are energized by 100 ns, 5 kV pulses generated by discharging parallel 50 Ω transmission lines through thyratrons. The number of paralleled cables is proportional to the width of the chamber and is approximately three cables/meter of chamber width. The lines are terminated at the HV bus of each chamber. Capacitors are in series with each termination to accommodate a clearing field when desirable.

Data Processing, Hardware

The basic circuit of the C-FET memory is shown in Fig. 5. In the quiescent state, C is charged to 15 volts. Because of the possibility of small leakage currents (the FET gates are biased to -8 V) C is recharged periodically between events by applying a 100 μs pulse to the gate of the FET. As long as there is no event the capacitor remains "charged". After an event, when a spark develops between the HV plane and the readout wire, a charge flows into the associated capacitors (reducing their voltage below the quiescent 15 V). The affected capacitors then remain "discharged" until a strobe (ADDRESS 1) pulse, applied some time later, recharges C. The resultant charging current develops a signal across the 200 Ω load resistor in the source circuit of the FET. Clamping diodes D1 and D2 are required to protect the FET's from overvoltage.

Thirty-two FET's are interrogated simultaneously by an ADDR 1 pulse producing a 32-bit word of raw spark data. Each plane, then, is divided into N/32 'words', where $1152 \leq N \leq 2304$ is the number of wires in the plane, depending on its size. Bits of like binary weights from each PC board are hardwire OR'ed and applied to a bank of 32 comparators. The value of ADDR 1 is used to denote the source of the 32-bit data word. Each board has a six bit "switch" (set of jumper wires) which enables it to recognize its "board address." By appropriate placement of the jumper wires any board can be made to respond to any value of ADDR 1. The 32-bit word is then reformatted into one or more 18-bit words (one for each spark) and fed into a PDP-9 computer via the direct memory access (DMA) channel.

Figure 6 is a flow chart for the data processing logic comprised of the following elements:

1. A 5-bit plane counter for identification of the wire-chamber plane from which data are to be taken next.
2. An ADDRESS 1 counter identifying the group of 32 'bits' within a given plane. The largest plane is divided into 72 words of 32 bits each; this requires that the ADDR 1 counter be 7 bits. Six bits are decoded on the FET PC board. The last, seventh bit is transmitted over one of two wires and selects the first or second group of 32 FETs on the card.
3. An ADDR 2 counter that encodes the location of the 32-bit word into 5 bits. The state of this counter corresponds to the last bit of the encoded spark position.

4. A 5-bit WIDTH counter, showing the number of wires 'hit' by the spark. The sum of ADDR 1, ADDR 2 and WIDTH total 17 bits, which along with a data format flag bit make up the 18-bit spark chamber word transmitted to the PDP-9.
5. Formatting logic consisting of a 32-bit shift-register, a 5 MHz gated clock, logic gates, and counters (2), (3) and (4).
6. A 9-bit counter generating sequential strobe pulses for acquisition of data from blind scalers, coincidence latches, ADC's for pulse height, ADC's for time-of-flight and identifier words for the experiment.

Acquisition and processing of data proceeds as follows (see Fig. 6): When the fast logic identifies an event, it pulses the chamber and starts the asynchronous operation of the data acquisition and processing logic. The DMA address and word-count registers are preset to state 00...01; the DMA address 0...0 is reserved for the total number of words in the event. First, the plane ID word is stored followed by wire chamber data words. The circuit tests each data word and increments ADDR 1 counter if it has no spark information. Otherwise the formatting logic is actuated. A 5 MHz clock is gated on to encode the 32-bit word into 5 ADDR 2 bits and 5 WIDTH bits. The spark location in any given plane is then equal to the wire spacing times the quantity[4]

$$\text{ADDR 1} + \text{ADDR 2} - \frac{\text{WIDTH}-1}{2} \ .$$

The hardware also recognizes the presence of 2 or more sparks within a group of 32 bits and proceeds with the encoding process generating one 18-bit word/spark until a test shows that all non-zero data have been processed. Note that if a spark should fall accross the boundary of two 32-bit words, two 18-bit data words will be sent to the PDP-9 computer; they will be reformed into a single spark by software programming. After the examination of the last group of 32 bits in a plane, an 'END-OF-PLANE' signal is generated to increment the plane counter. The new plane ID is stored in memory; examination and formatting of data words then proceeds as before. The last word in the spark chamber system produces an END-OF-CHAMBER identification word and initiates acquisition of counter data consisting of some 200 registers. A hardware test allows only non-zero data to be fed into the DMA-allocated memory locations. After completion of counter data acquisition, the DMA address register is set to 0...0, and the contents of the DMA word-count register are stored in that location. Thus the first word in the DMA memory block informs the program of the number of words transferred in the block.

To test the chamber system one selects one plane at a time, manually or under program control, and goes through the same processing sequence utilizing the same circuitry as for a real event. For this test, one applies a 6-volt pulse to the drain electrodes of all FET's in a plane. This is done by remotely pulsing the clamp voltage from +15 V to +21 V. When the FET's are subsequently strobed in the test readout, this additional voltage simulates the "discharged" state associated with a spark. Hence all wires should indicate a spark. Those words that fail the test are recognized by the formatting logic and stored in memory.

An event of seven sparks per plane will be processed by the hardware in less than 3 ms. The test of a plane requires 1.25 to 2.5 ms, depending on the number of wires in that plane.

Data Processing, Software

The software for the on-line computer (a PDP-9) has been designed with two factors in mind. One, since a complete analysis of every event would require a prohibitive amount of on-line computer time, the experimental data must be transferred to magnetic tape for later analysis by a full-scale off-line computer (an IBM 360/91). Two, in order to prevent massive losses of running time, system performance must be monitored on-line. To answer the second requirement, some analysis will be done on every event, and a complete analysis will be done on some fraction of the events. Thus, the computer will continuously monitor the performance of the wire chamber, and periodic diagnostic procedures will test the photomultiplier tubes, the electronic logic, the magnet current, and associated equipment. In addition, some fraction of the events will undergo complete geometric and kinematic reconstruction. It also will be possible to compare current results to a reference library of previous results (kept on DECTAPE).

The times (per event) required for each segment of the analysis are estimated to be:

Input, reformatting, and output	10-15 ms
Diagnostic checks plus histogramming	15-40 ms
Geometric reconstruction (assuming 3 tracks)	25-40 ms
Kinematic reconstruction	10-15 ms

Thus, we expect the computer to be able to accept 20-30 events/s, and to reconstruct about 10 events/s. With a large fraction of the data being analyzed on-line, we expect to have a clear idea of the quality of our data as we take it. At 15 events/s and 100 words/event, we expect to write one magnetic tape (2400 feet, 800 BPI) every 2 hours.

Performance

A $1.2 \times 1.2\ m^2$ prototype chamber has been constructed and tested. The performance of this chamber was first monitored optically and was found to be excellent from the following viewpoints:

1. The applied high voltage at which sparks became visible at various points in the chamber varied by less than 200 V. The chamber operated satisfactorily over a 4000 V range on the high voltage supply (which is operated at about 15 kV), the upper limit resulting from excessive width of sparks.
2. Although no quantitative tests were made for multi-track efficiency, extensive air showers which produced on the order of several hundred sparks were observed, and the difference in brightness of these sparks was barely discernible from the brightness of single track events. Furthermore, a monitor probe connected to the high voltage "bus bar" showed

the waveform of the multi-spark events to be identical to the single spark events.

A prototype FET PC card for 64 wires was constructed and tested.

The performance of this readout system was found, if anything, to be superior to the optical viewing since the readout system was sensitive enough to detect sparks which were invisible to the naked eye in a totally darkened room. The upper threshold for the applied HV was once again determined by the same criterion as above — excessively broad sparks.

A lifetime test was made by accepting 2×10^6 tracks into the 64-wire prototype board with the high voltage set near the upper limit. There was no observable deterioration in the system and no FET's or diodes were damaged. We concluded that the concept is entirely satisfactory and have gone into full scale production.

Acknowledgements

The authors wish to thank Professor M. Schwartz for his continuous interest in this project and his frequent consultations on matters of principle. Thanks and credits are also due to many members of SLAC, too numerous to mention, for their excellent support in mechanical and electronic design and construction. Finally we are grateful to T. A. Nunamaker and M. J. Neumann for useful discussions concerning the design and operation of this type of chamber.

References and Footnotes

1. M. Neumann and T. A. Nunamaker, "High Sensitivity Wire Spark Chamber Readout Useful in Strong Magnetic Fields," IEEE Trans. Nucl. Sci. Vol. NS-5, (June 1968); pp. 591-3.

2. The thyratron pulsers were based upon a design by M. Gan.

3. Note that the sparks jump between wire planes of different modules.

4. The quantity ADDR 1 is effectively multiplied by 2^5 through its bit position in the formatted word.

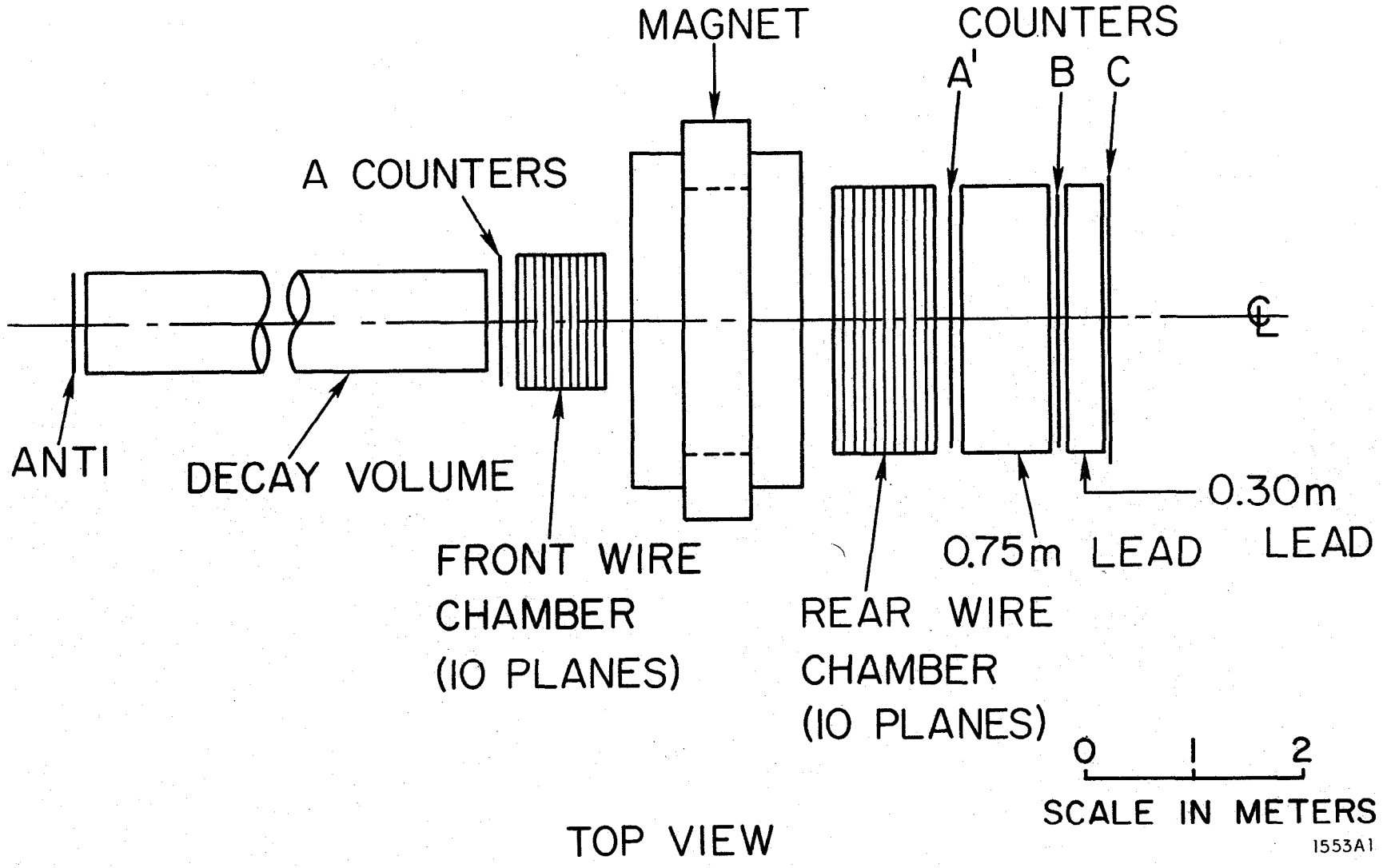

FIG. 1--Plan view of spectrometer.

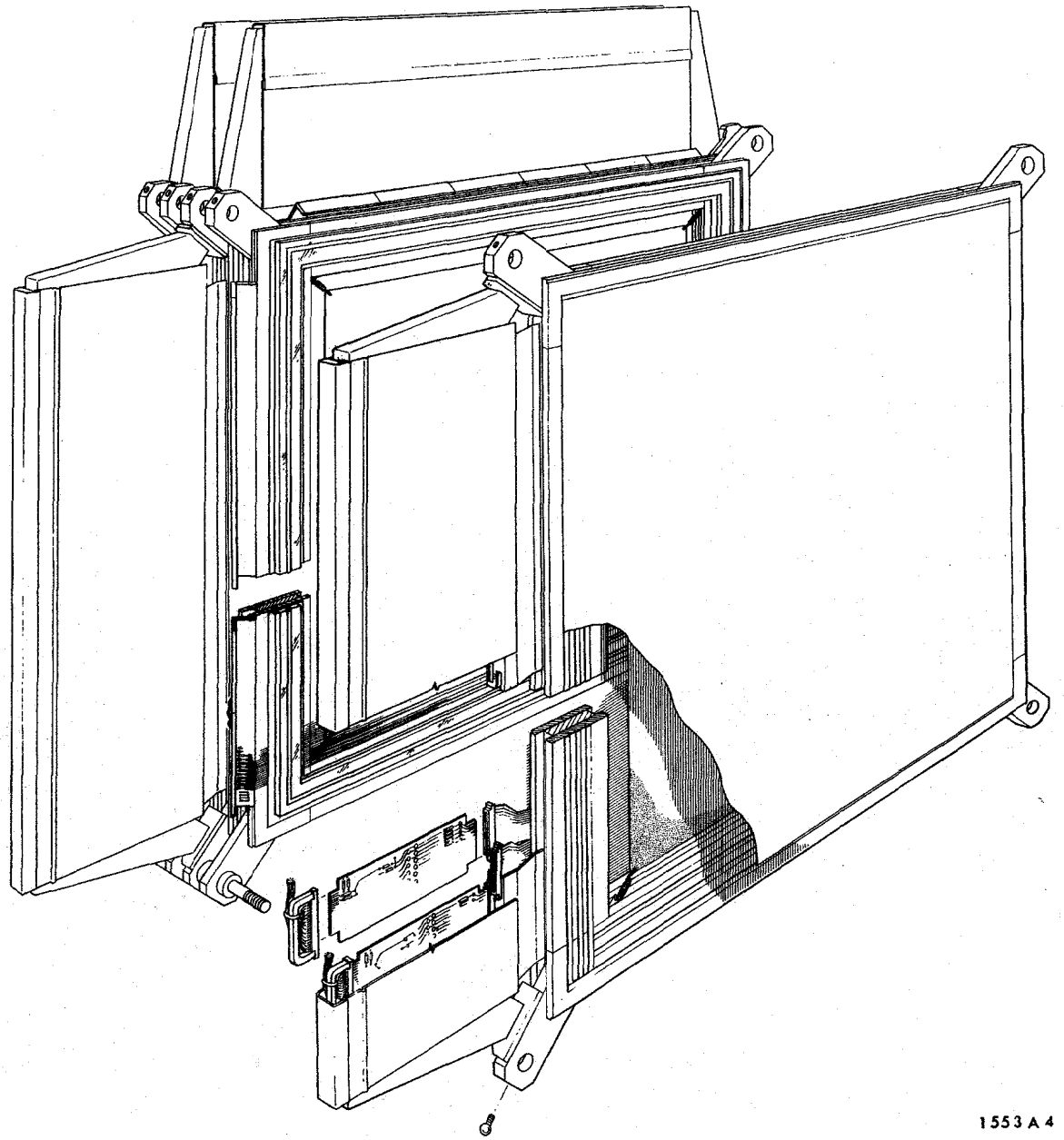

FIG. 2--Spark chamber assembly, exploded view.

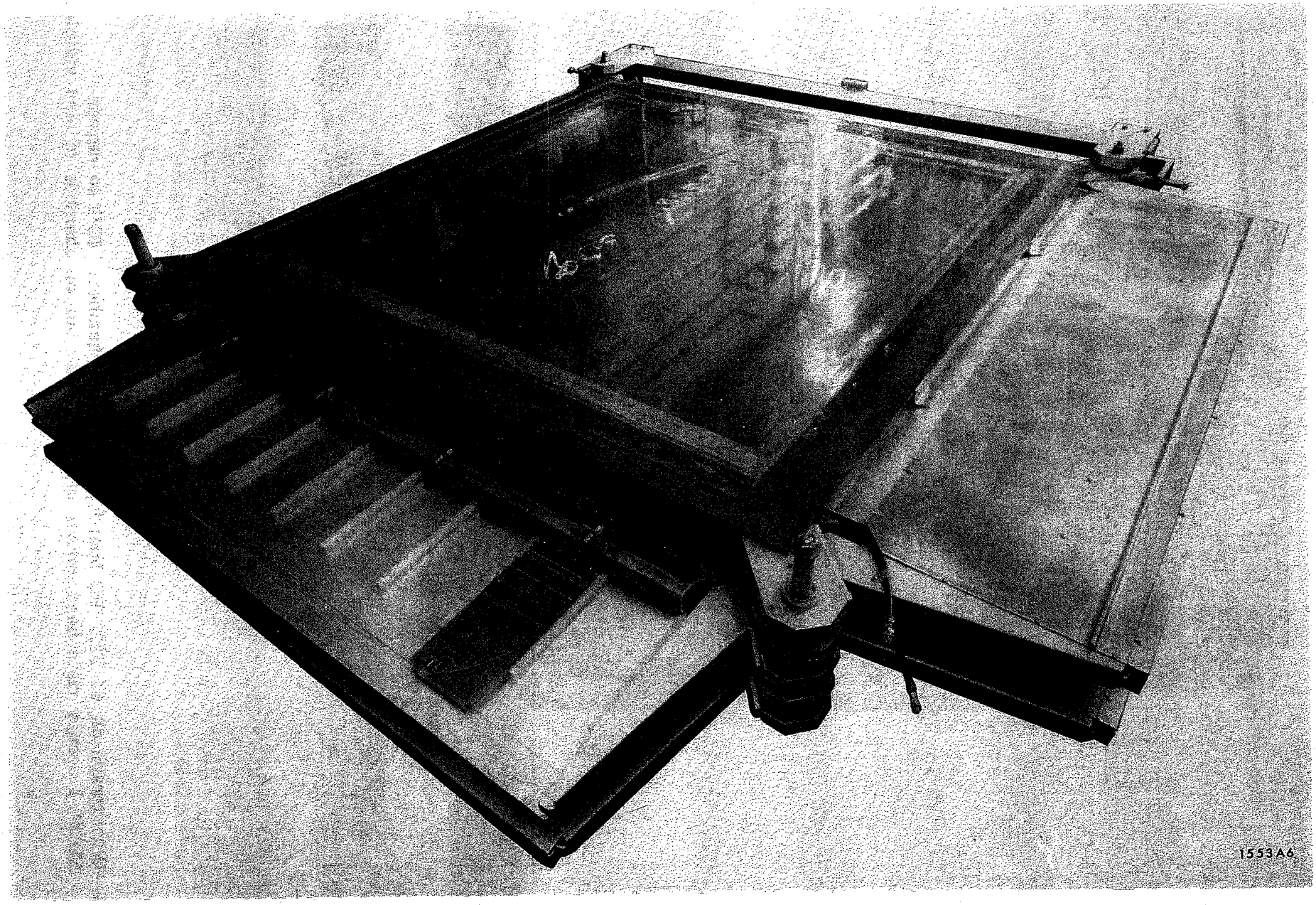

FIG. 3--(Photograph of) 1.2×1.2 m^2 module assembly.

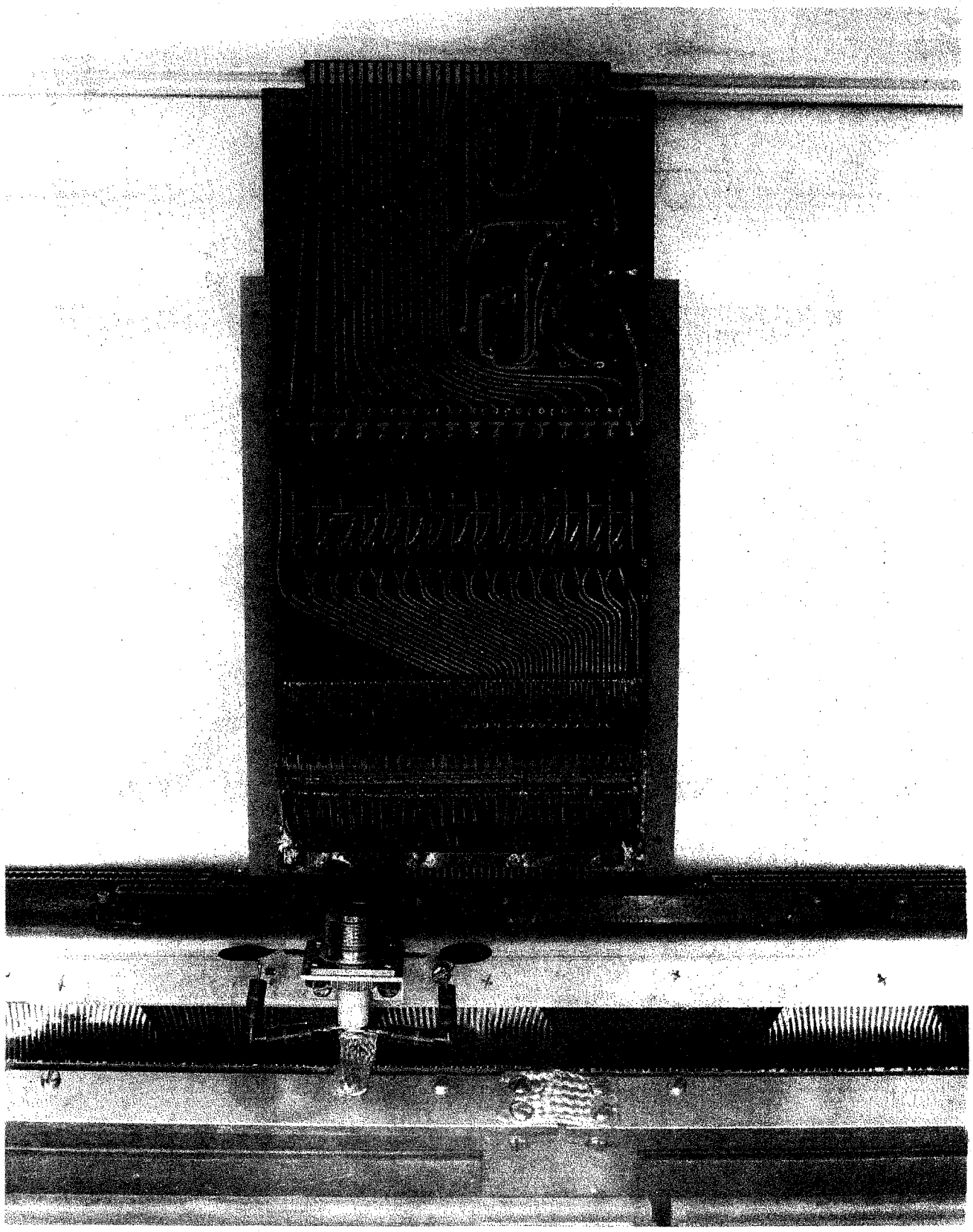

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FIG. 4--(Photograph of) 64-FET PC board plugged into chamber. IC's to decode ADDR 1 occupy right-hand corner of board. HV bus on chamber is also visible.

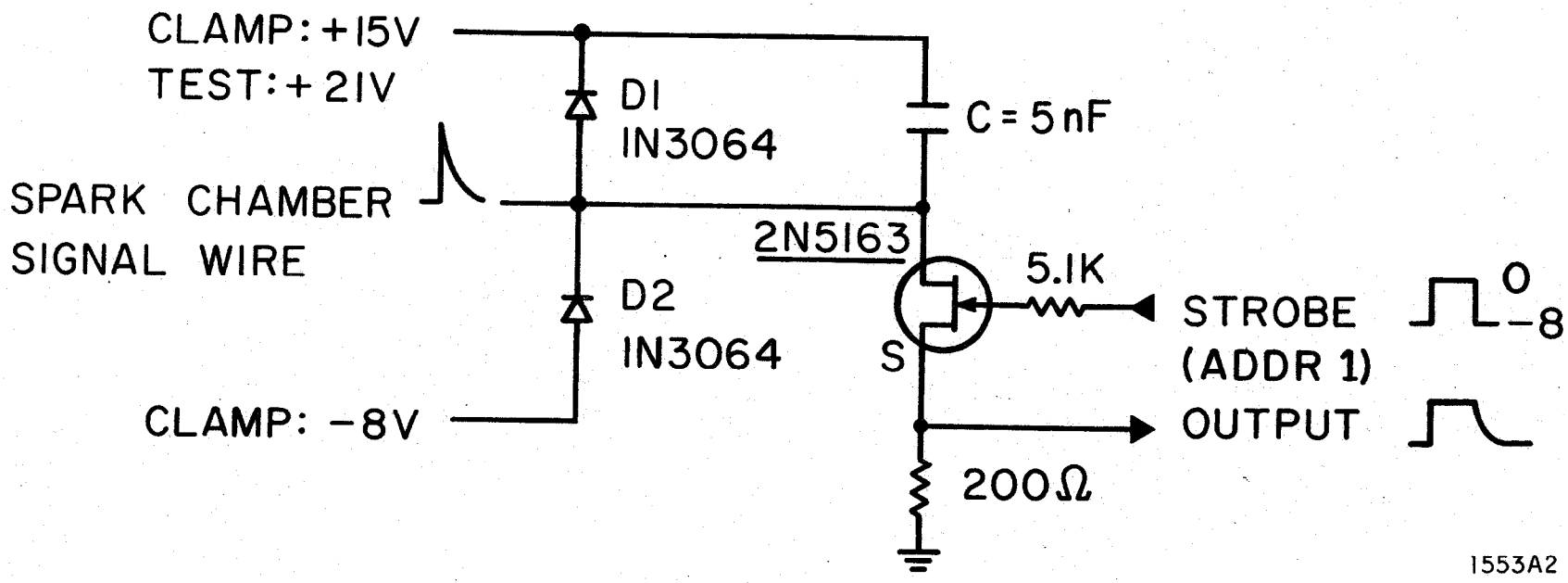

FIG. 5--Basic C-FET memory and readout circuit.

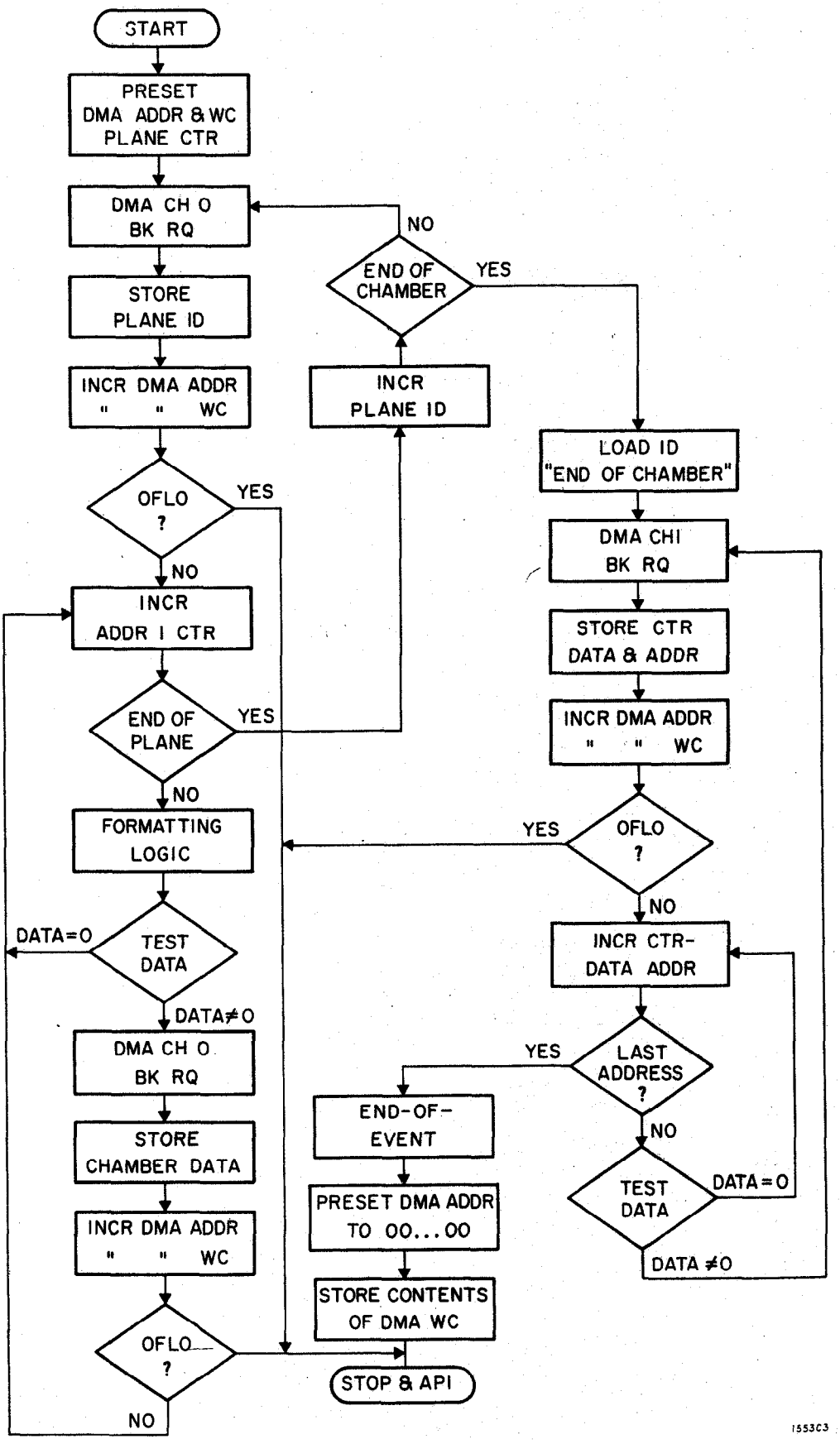

FIG. 6--Flow chart for the data processing logic.