

LINE SYNCHRONIZED PULSER*

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This note describes a line synchronized pulser that can also be used as a sweep generator, variable time delay, and frequency divider. This line synchronized pulser differs from the one given by A. G. Richardson (Electronic Design 23, Nov. 7, 1969) in that the pulse can be generated anywhere within the half period and also one or more half periods can be skipped before the pulse is generated.

The device functions as follows. Refer to the top half of Fig. 1. The ac line voltage is converted to a +20 to -0.6 across the RC circuit. The capacitor charges toward 20 volts. When the voltage across the capacitor reaches 10 V the PNPN diode breaks down, and it discharges through the base-cathode of the SCR, pulsing it on. The turning on of the SCR removes the charging voltage for the remainder of the half period.

The bottom half of the schematic of Fig. 1 performs in a similar manner except that it is active during the negative half period. Also, the SCR is replaced by a programmable unijunction transistor. This is done to allow the circuit to be anti-symmetrical with respect to ground. If an SCR were to be used as shown in Fig. 2, the pulse from the capacitor discharge is not with respect to ground. The waveforms across the SCR and PUT respectively are shown in Fig. 3.

The RC time constant can be adjusted to yield a frequency divider. The voltage waveform across the SCR of a divide by 6 pulser is shown in Fig. 4. The pulser can also be driven with inverted dc.

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The voltage waveform across C is a constant amplitude sawtooth, and therefore it can be used as a sweep generator. The beam can be blanked at all times except when the voltage across the SCR is high, which is during the sweep.

FIGURE CAPTIONS

1. Line synchronized pulser with antisymmetrical pulses with respect to ground.
2. Alternate version of bottom portion of Fig. 1.
3. Voltage waveform across SCR (top trace) and across PUT (bottom trace, inverted).
4. Voltage across SCR of a divide by 6 pulser.

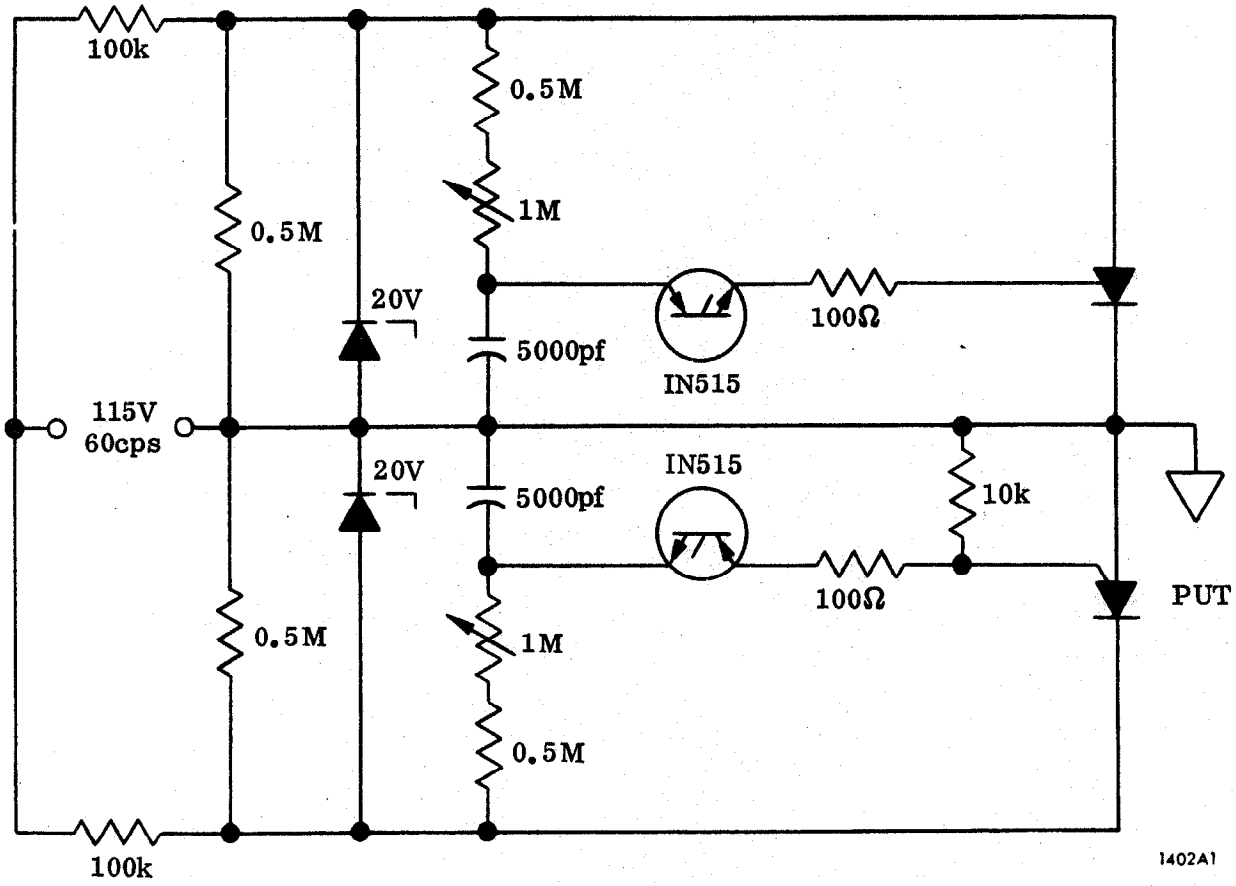


Fig. 1

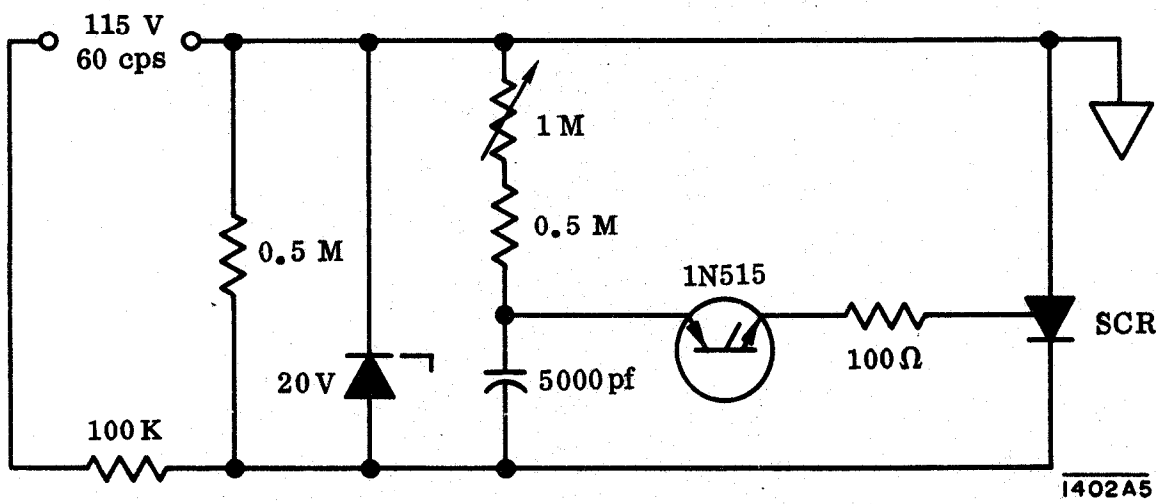


Fig. 2

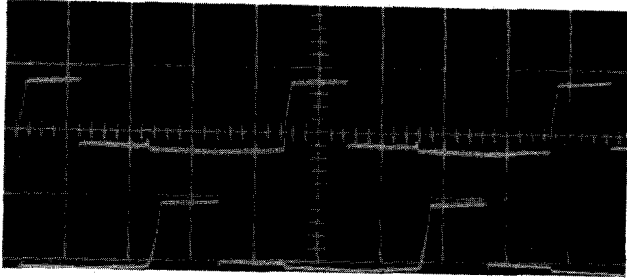


Fig. 3

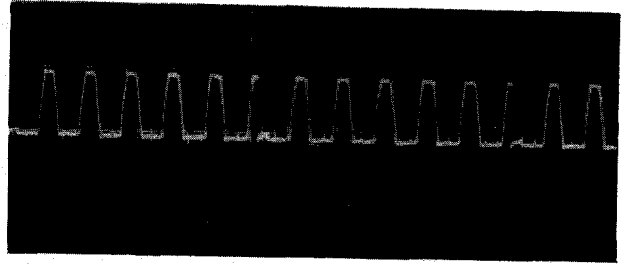


Fig. 4

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