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OPERATION OF A 100 MHz COUNT-RATE METER*

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ABSTRACT

We present the design of a digital count-rate meter operating at frequencies up to 100 MHz, and implemented with emitter coupled integrated circuits. Four channels with visual display are available, and permit simultaneous evaluation of count-rates in four locations. This instrument has been found useful in the field of high energy physics for the setup of scintillation counters, or for the steering of a secondary beam into a magnet.

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I. INTRODUCTION

The purpose of this rate meter is to provide an experimenter with the visual display of several count-rates, as it is often required in the preliminary set-up of a high energy physics experiment.

By rate measurement we mean that over a fixed interval of time, randomly spaced counts are observed, which are accumulated by a scaler and displayed such as to indicate how many counts have been received per unit of time. The unit of time here, is two microseconds, that is the accelerator pulse width, at the Stanford Linear Accelerator Center; in this case the display reads "counts per pulse."

Count-rates can be simultaneously obtained on four channels. The instrument includes a timing section permitting the selection of 10, 100, or 1000 samples, or units of time, thereby allowing higher accuracy when the number of counts per pulse, that is the rate, is low.

II. THE 100 MHz CHANNELS

The channels accept logic pulses from -300 mV to -700 mV, with a minimum width of 3 nanoseconds. The circuit is described by Fig. 1. An amplifier maintains a sufficient voltage swing at the input of a "Schmitt trigger," for the prescribed range of signal variations. The output waveform is such that the signal can trigger a Motorola MC1027 flip-flop with a positive going pulse starting at -1.5 V. The discriminator threshold can be trimmed in order to optimize the trigger pulse width at the maximum frequency. The photographs of Fig. 2 show the performance of this circuit; the effect of two discriminator threshold levels can be observed,as well as the response to a 125 MHz pulse train.

The MC1027 flip-flop and the three MC1013 flip-flops which follow it (Fig. 3) are of the $\overline{J}\,\overline{K}$ type; they incorporate a logic NOR function and thus can be easily connected as a decade counter. Gating of this counter can be achieved from standard TTL levels, by shifting negatively the trigger base line at the output of the discriminator. This procedure ensures that the gate will not introduce extra counts. Return from this first decade to TTL logic levels is then performed by four level shifters.

The output of the three decades, namely the 100 MHz MECL decade, and the two TTL decades, are buffered and finally decoded and displayed.

The gating signals applied to the channels are of different nature:

(1) A wide gate with a duration of 10, 100, or 1000 accelerator pulses, and generated by the instrument timing circuit, turns "on" the discriminators in order to accept any counts occurring during this preselected interval of time.

(2) An external gate input is also provided which allows to "frame" the incoming bursts of counts according to their time sequence. This gate must be applied to each individual channel.

(3) When the accelerator pulses are properly shaped and timed, it is possible to use them as gating signals for the channels. This function is referred to as internal gating and is simultaneously effective on all four channels, at the flip of a toggle switch.

The gating signals described under (2) and (3) are "AND-ed" with the gate of (1).

III. THE TIMING SECTION (Fig. 4)

This circuit accepts accelerator trigger pulses of $\pm$ 1 V or $\pm$ 10 V. The front end is essentially identical to that of the channels with the addition of an

inverter. The discriminator drives a preset decade counter, which provides the gating function required by the channels.

The timing section sets also the refresh cycle of the rate meter (the display is refreshed every 0.5 second) and provides a single cycle operation with manual trigger.

An illustration of the timing sequence is shown on Fig. 5.

IV. COUNT-RATE METER SPECIFICATIONS

(1) Timing section:

Input impedance	50 ohm
Sensitivity	± 500 mV at 25 nsec pulse width
Repetition rate	dc to 360 Hz

(2) Channels:

Input impedance	50 ohm
Sensitivity (negative pulse)	300 mV for 3 nsec or wider pulses
Maximum frequency	dc to 100 MHz (measured with -300 to -700 mV pulses and a pulse width of 3 nsec)

(3) Gates

(a) External gate

input impedance	larger than 1 K ohm
gate open	no connection required or not more than 1.0 volt
gate closed	not less than 1.5 volt
delay	opening not more than 10 nsec closing not more than 5 nsec

(b) Internal gate: gating of the four channels is simultaneously performed internally by the timing section input signal. For this purpose, the timing signal should constitute a window having the proper width and time sequence, and should be operative 50 nsec before the occurrence of the count bursts.

ACKNOWLEDGEMENT

The layout of the circuits and the testing procedure of this count-rate meter have been devised by C. R. Carman.

LIST OF FIGURES

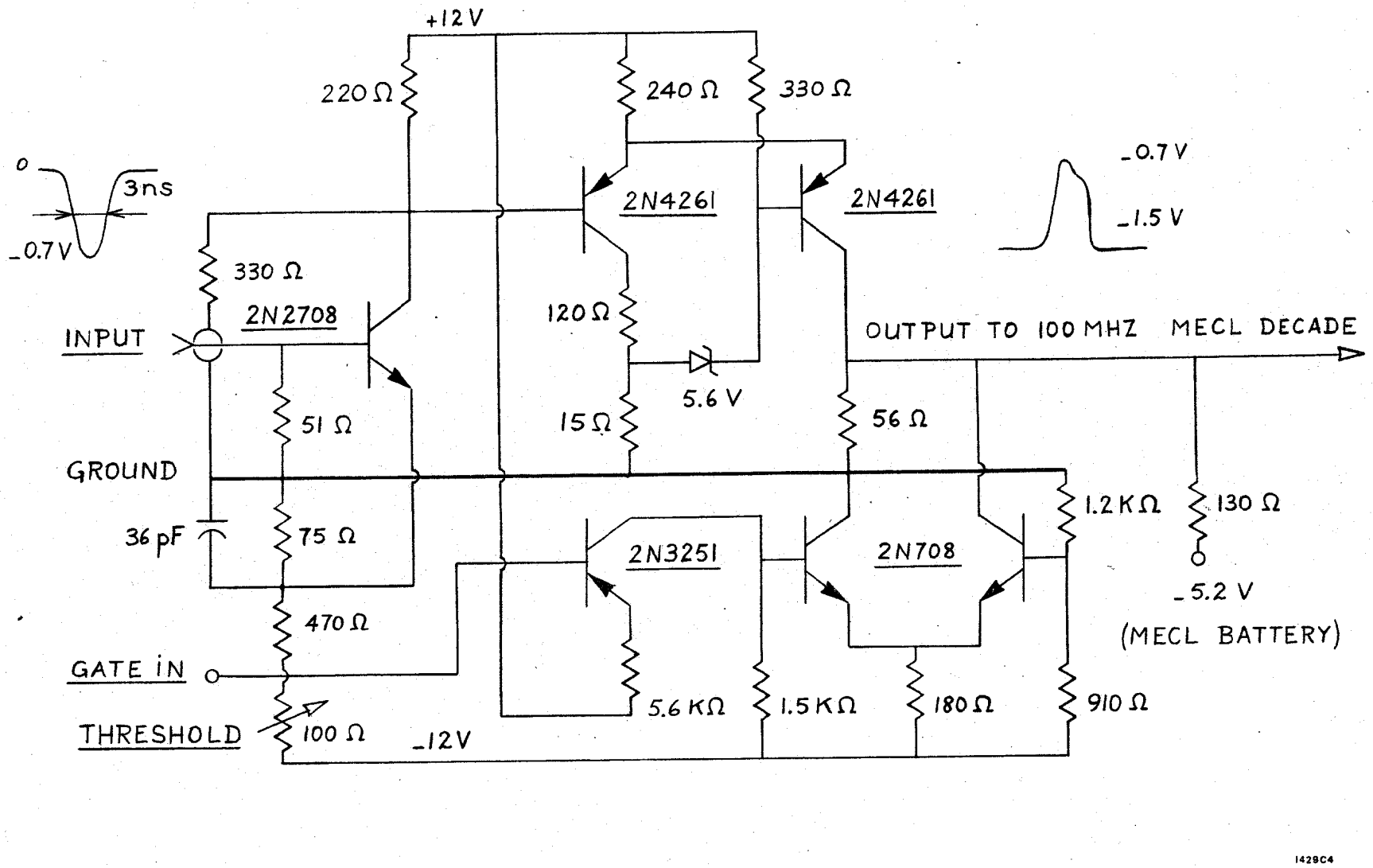
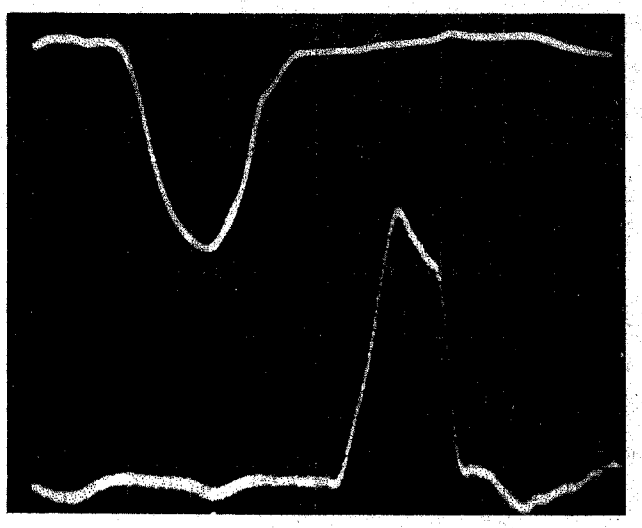

+12 V
220 Ω
240 Ω
330 Ω
0
3ns
-0.7 V
2N4261
2N4261
-0.7 V
-1.5 V
330 Ω
2N2708
120 Ω
INPUT
OUTPUT TO 100 MHZ MECL DECADE
5.6 V
51 Ω
15 Ω
56 Ω
GROUND
1.2 KΩ
130 Ω
36 pF
75 Ω
2N3251
2N708
-5.2 V
(MECL BATTERY)
470 Ω
GATE IN
5.6 KΩ
1.5 KΩ
180 Ω
910 Ω
THRESHOLD
100 Ω
-12V
1429C4

Fig. 1

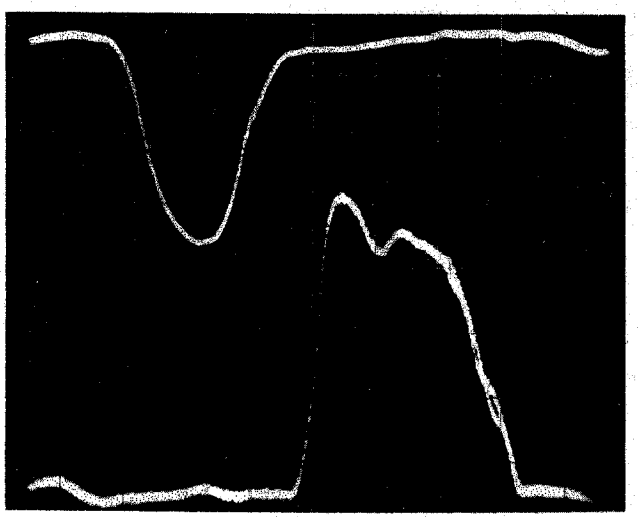


← INPUT

2 nsec/cm

200 mV/cm

MINIMUM THRESHOLD

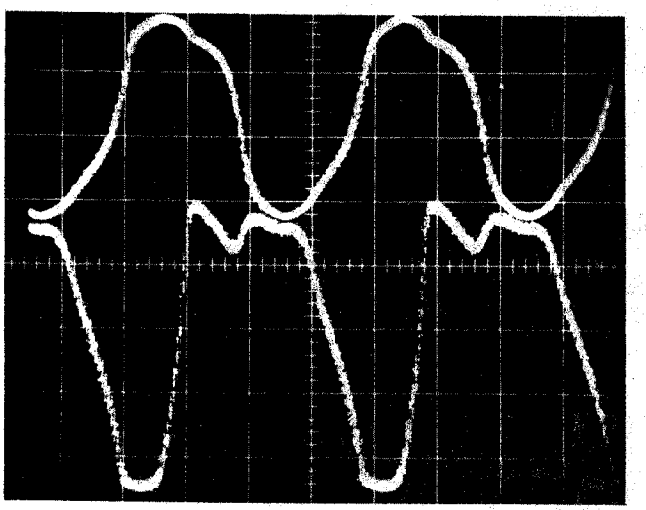


← INPUT

2 nsec/cm

200 mV/cm

MAXIMUM THRESHOLD



← INPUT

2 nsec/cm

200 mV/cm

125 MHz

1429A6

Fig. 2

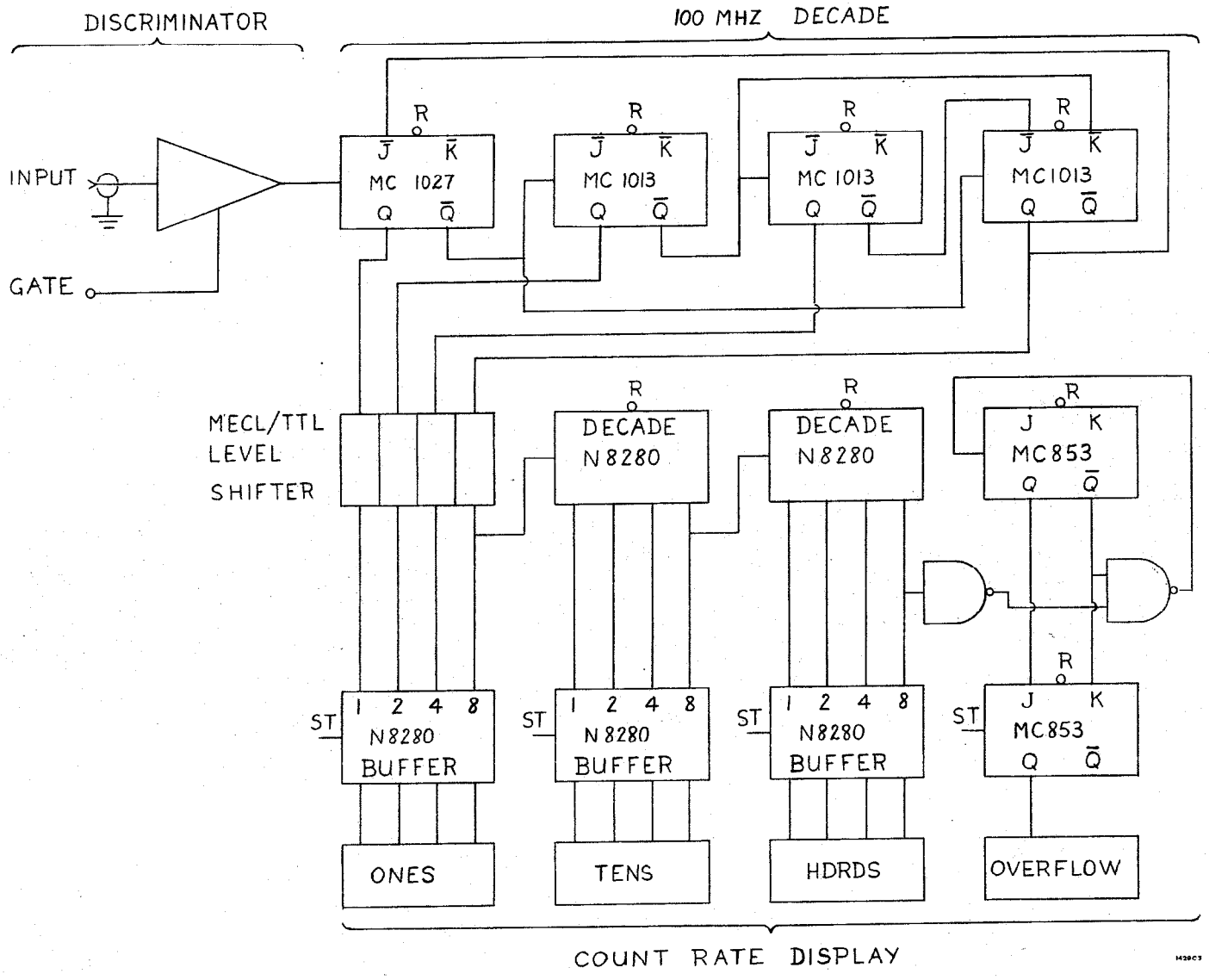

DISCRIMINATOR
100 MHZ DECADE
INPUT
GATE
R
J K
MC 1027
Q Q̄
MC 1013
MC1013
MECL/TTL
LEVEL
SHIFTER
DECADE
N8280
J K
MC853
ST
1 2 4 8
N8280
BUFFER
ONES
TENS
HDRDS
OVERFLOW
COUNT RATE DISPLAY

Fig. 3

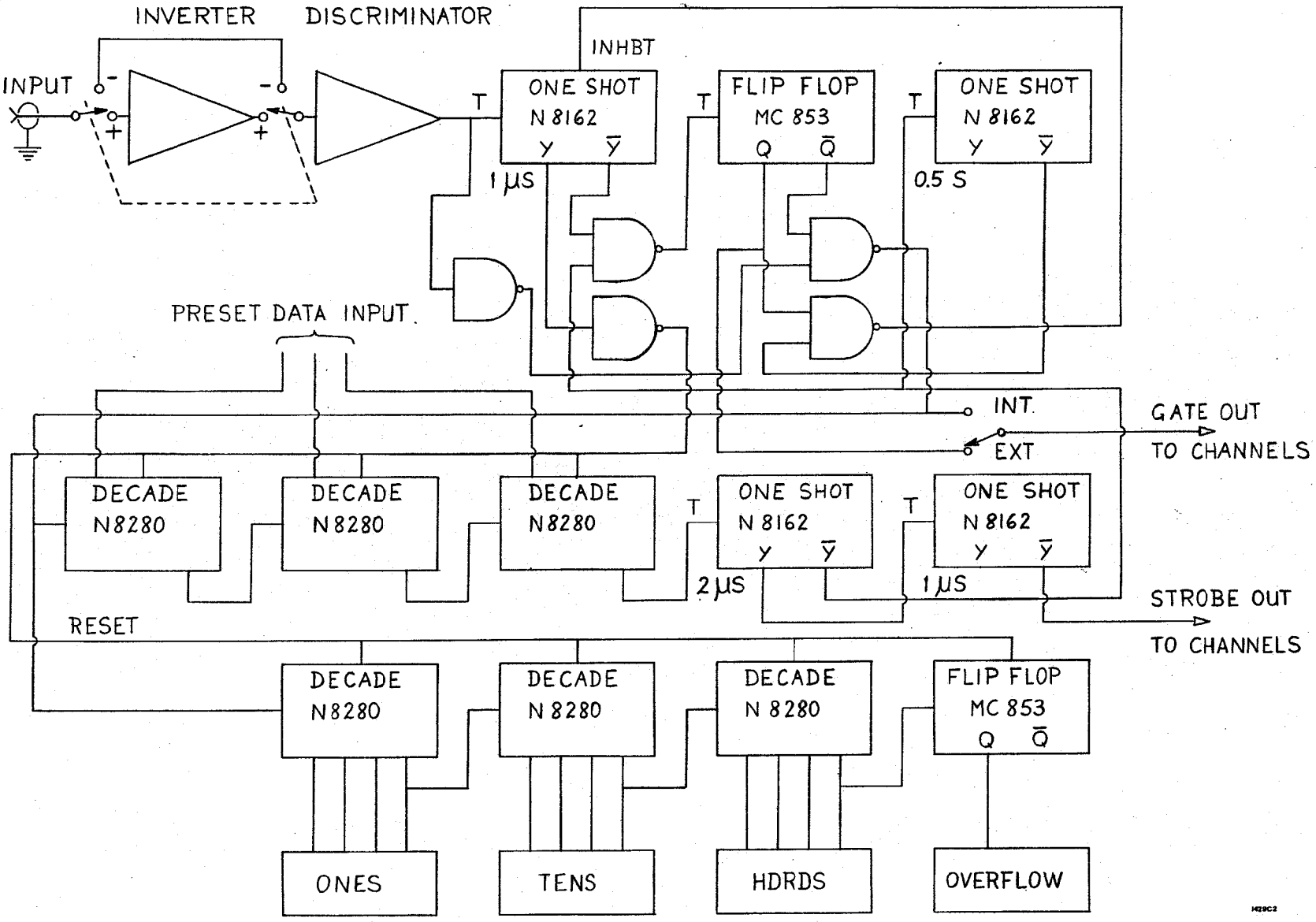

INVERTER
DISCRIMINATOR
INPUT
INHBT
ONE SHOT
N 8162
Y
$\bar{Y}$
T
1 μS
FLIP FLOP
MC 853
Q
$\bar{Q}$
ONE SHOT
N 8162
0.5 S
PRESET DATA INPUT
INT.
EXT
GATE OUT
TO CHANNELS
DECADE
N8280
DECADE
N8280
DECADE
N8280
ONE SHOT
N 8162
2 μS
ONE SHOT
N 8162
1 μS
STROBE OUT
TO CHANNELS
RESET
DECADE
N8280
DECADE
N 8280
DECADE
N 8280
FLIP FLOP
MC 853
ONES
TENS
HDRDS
OVERFLOW

Fig. 4

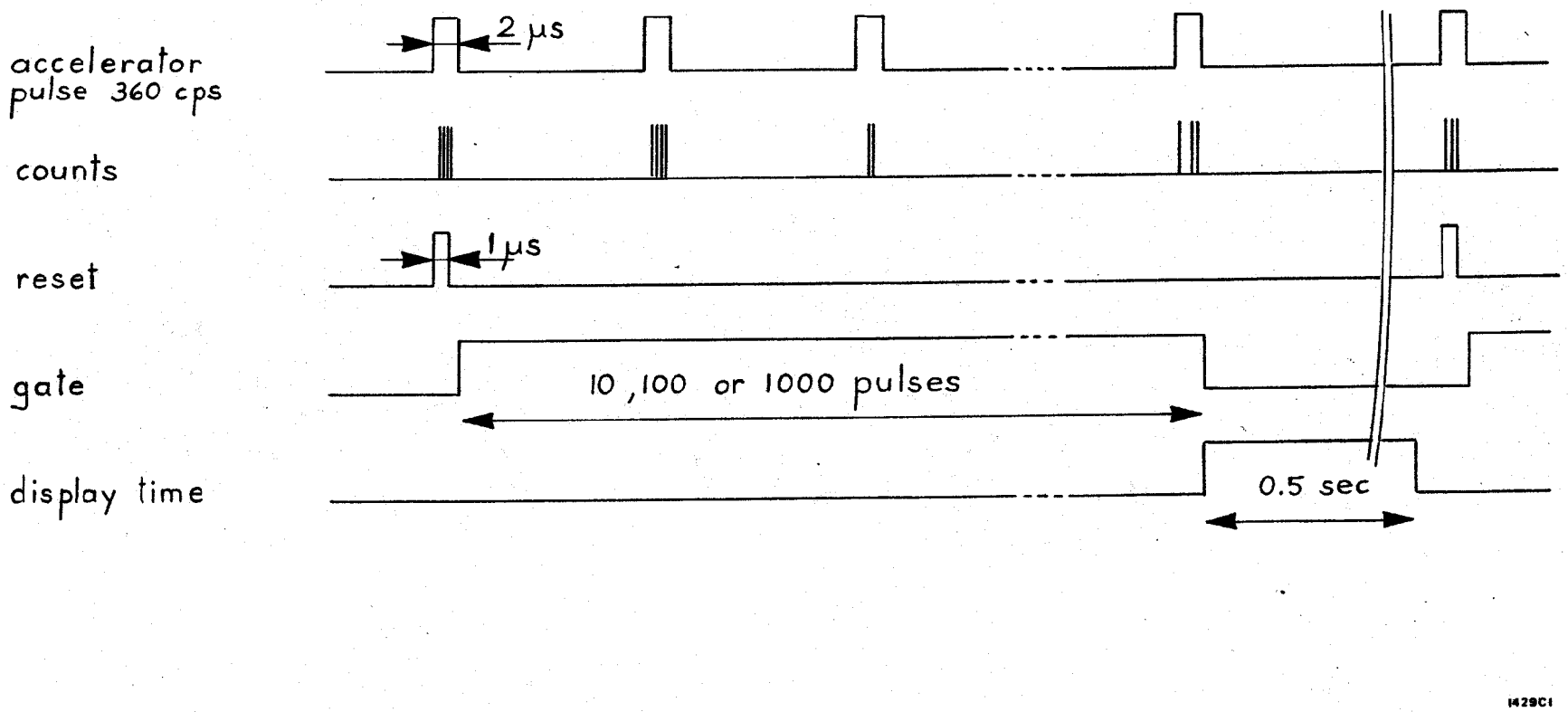

accelerator
pulse 360 cps
2 μs
counts
reset
1 μs
gate
10 , 100 or 1000 pulses
display time
0.5 sec
1429C1

Fig. 5

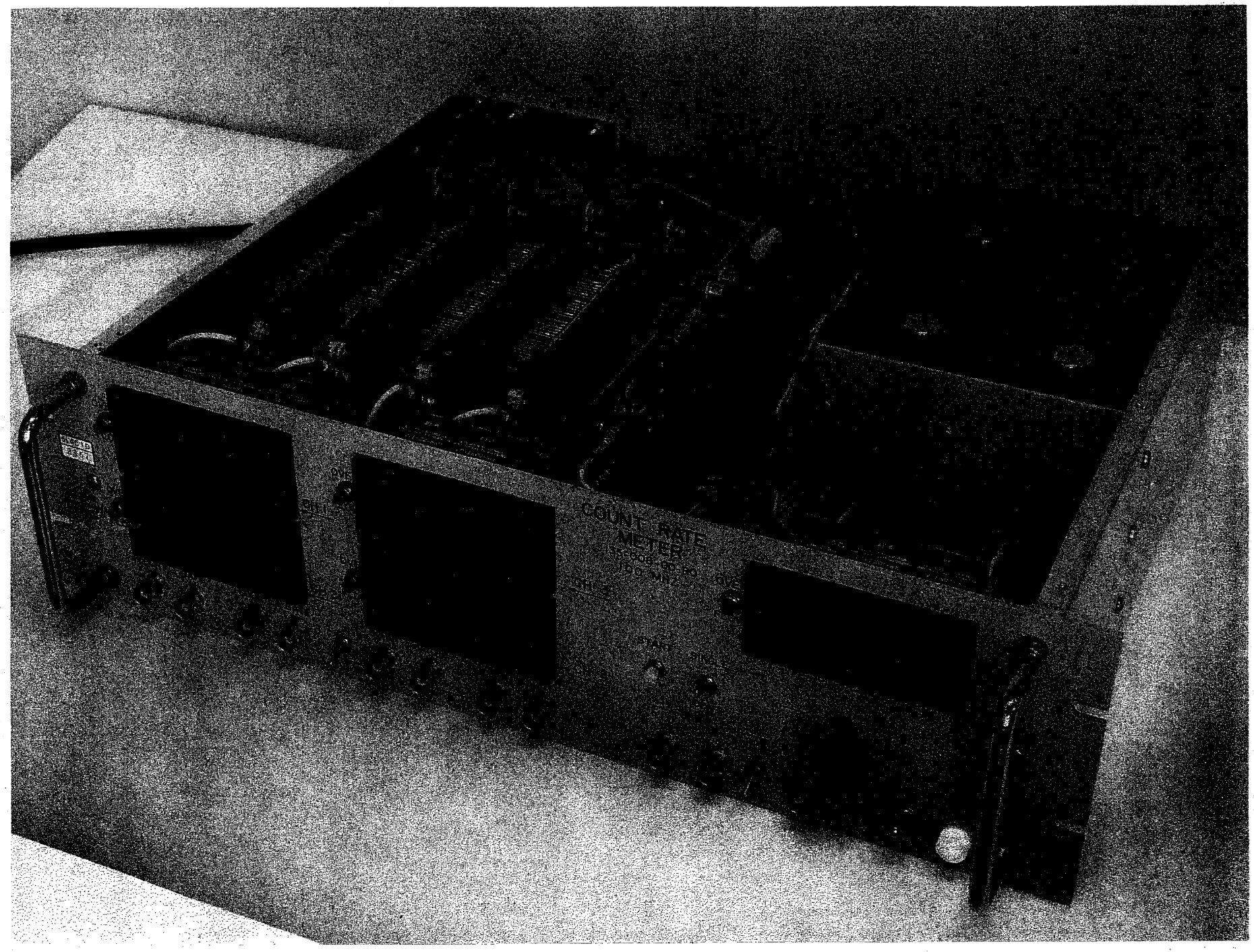


Fig. 6