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INTEGRATED-CIRCUIT DISCRIMINATOR WITH 10-NSEC PULSE PAIR RESOLUTION*

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ABSTRACT

A high-speed direct-coupled discriminator utilizing emitter-coupled integrated circuits is described. The threshold is continuously adjustable between -150 mV and -1.15 V, the pulse pair resolution is 10 nsec, and the maximum continuous repetition rate is 92 MHz. Two modes of operation, clipped and dc, are provided; output widths in the clipped mode are 5 nsec, 10 nsec, or 15 nsec. The use of integrated circuits result in a complete absence of trimming adjustments. Provision is made for remote control of the threshold, mode, and width.

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I. INTRODUCTION

The last few years witnessed the introduction and proliferation of emitter-coupled integrated circuits. These circuits are based on the emitter-coupled pair,[1] which is highly suitable for monolithic technology and is capable of high-speed operation. The emitter-coupled pair has found widespread application in high-speed circuitry, both laboratory[2] and commercial, and the emitter-coupled integrated circuits have now reached a comparable speed of operation.

The circuits utilized here are of medium speed and cost. The principal circuit is the MC1023L;[3] a schematic diagram is shown in Fig. 1. Four inputs, a noninverting (AND) output, and an inverting (NAND) output are provided. The circuit operates on -0.8 V and -1.6 V input and output levels, risetimes and delay times are in the vicinity of 2 nsec.

In addition, another circuit of the Series,[3] the MC1025L (Fig. 2), has been used. It consists of two composite transistors which can be made independent of each other by reverse biasing the substrate diodes on pin 7. Each composite transistor consists of several (4 or 5) sections, the active area can be varied by connecting or reverse biasing the individual bases. It was found that, for best high-speed operation, the optimum dc emitter current was in the vicinity of 7 mA per section.

The basic decision-making element is a 10-mA Gallium-Arsenide tunnel diode,[4] providing a high speed of operation and a closely controlled hysteresis.

II. DESCRIPTION

The discriminator consists of a Schmitt Trigger, a Shaper, and an Output Stage. The Schmitt Trigger Circuit (Fig. 3) operates on negative input signals with a threshold continuously adjustable from -150 mV to -1.15 V. It provides

an output pulse with a constant height and with a width equal to that of the input pulse above threshold. The input circuit is of the high-impedance bridging type. A signal entered on one of the terminals is available for further use on the other one with a delay of 1 nsec and a risetime deterioration of <2 nsec.

The Shaper (Fig. 4) provides an output pulse at each negative-going transition of the Schmitt Trigger output signal. In the clipped mode of operation, the output pulse width is 5 nsec, 10 nsec, or 15 nsec as selected by a 3-position WIDTH switch. The output pulse is followed by a deadtime which equals the output pulse width or the width of the negative-going output signal of the Schmitt Trigger circuit, whichever is greater. In the dc mode of operation, the width of the output pulse equals that of the negative-going output signal of the Schmitt Trigger circuit or it is 5 nsec, 10 nsec, or 15 nsec as selected by the 3-position WIDTH switch, whichever is greater. The deadtime following the output pulse is 5 nsec, 10 nsec, or 15 nsec, as selected by the 3-position WIDTH switch.

The Output Stage (Fig. 5) converts the -0.8 V to -1.6 V levels of the emitter-coupled integrated circuits (ECL) to those of Nuclear Instrument Modules (NIM).[5] Two true outputs (OUT) and two complementary outputs ($\overline{\text{OUT}}$) are available. Each of the four outputs is capable of providing a -0.8 V signal on a 50-ohm resistance with risetimes and falltimes of <2 nsec.

III. OPERATION

The Schmitt Trigger (Fig. 3)

The negative-going input signal, after level-shifting by emitter follower Q1A, is applied to emitter-coupled pair Q2A-Q2B which carries a dc current of 20 mA supplied by Q3A. Input threshold is adjusted via a 100 ohm helipot and level-shifter Q1B. Since Q1A and Q1B, and also Q2A and Q2B, are

transistors on the same chip, they are reasonably well matched in emitter-base voltage drop and in temperature coefficient, hence trimming adjustments on the threshold are not necessary.

At zero input voltage, most of the 20 mA standing current flows in Q2A and only a small fraction (<0.5 mA) in Q2B. Thus the 10 mA Gallium-Arsenide tunnel diode[4] is in its "low" state at near zero voltage. When slightly over half of the 20 mA standing current is transferred from Q2A to Q2B by a negative input signal, the tunnel-diode switches into its "high" state at $\approx$-1 V. The voltage swing of the tunnel-diode is shifted to the operating levels of the emitter-coupled integrated circuits by emitter-follower Q3B.

The Shaper (Fig. 4)

The operation of the Shaper circuit may be described as follows.

In the 5-nsec WIDTH position, integrated circuits P12 through P19 are deactivated and operation is restricted to P1 through P11. In the quiescent state, the output of the Schmitt Trigger circuit is at -0.8 V, and the non-inverting output of P2 and the lowermost input of P3 are at -0.8 V. The inverting output of P2 and the uppermost input of P4 are at -1.6 V, and the non-inverting output of P6 and the lowermost input of P4 are at -0.8 V. Both the SET (input of P5) and the RESET (input of P6) terminals of flip-flop P5-P6 are at -1.6 V. When, in response to a negative-going (-0.8 V to -1.6 V) signal at the output of the Schmitt Trigger circuit, the outputs of P2 switch states, flip-flop P5-P6 will be set via P3. After a delay of 5 nsec (intrinsic to the circuits), the non-inverting output of P5 and the uppermost input of P3 switch to -0.8 V, and the non-inverting output of P6 and the lowermost input of P4 switch to -1.6 V. Flip-flop P5-P6 will be reset at this time if the outputs of P2 had returned to their quiescent states in the interim, or will be

reset later when they will do so. Thus for each negative-going output signal of the Schmitt Trigger circuit, flip-flop P5-P6 produces a pulse with a ≥ 5 nsec width. In the dc mode, this pulse is processed without further shaping to the Output Stage via P7 and P11, since P8, P9, and P10 are deactivated by the DC-CLIPPED switch. In the CLIPPED mode, the output signal of P11 is inhibited via P8, P9, and P10 after a delay of 5 nsec (intrinsic to the circuits), thus a 5-nsec wide output pulse results.

In the 10-nsec WIDTH position, integrated circuits P4, P8, and P12 through P15 are deactivated. The SET feedback from the non-inverting output of P5 to the input of P3 is supplemented by one via P7, P16, and P17. The RESET feedback from the non-inverting output of P6 via P4 is substituted by one via P7, P16, P17, and P19. In the CLIPPED mode, the output signal of P11 is inhibited via P16, P17, P18, P9, and P10, resulting in a 10-nsec wide output pulse.

In the 15-nsec WIDTH position, P16 is substituted by P12 through P15, resulting in 15-nsec SET and RESET delays, and in a 15-nsec output pulse width in the CLIPPED mode.

Construction (Fig. 6)

The circuit was constructed on a Wire-Wrap[6] board. The particular board used[7] has the ground plane and the -5.25 V power plane on the two sides of the board; integrated circuits plug into sockets constituting an integral part of the board. Additional components were Wire-Wrapped or soldered to the pins assuring low stray inductances.

The ease of altering connections on the Wire-Wrap[6] board proved very convenient in the development of the circuit. It seems, however, that significant reduction of stray inductances, and an improvement in operation might be attained by printed-circuit construction which is now in progress.

Performance

Pulse-width dependence of the input threshold was measured for various values of threshold settings. It was found that the input threshold was within 15% of its nominal value set by the front-panel-mounted helipot for $\geq$ 6-nsec wide input pulses, and it was within 50% for 3-nsec wide input pulses.

Pulse-pair resolution was measured as 10 nsec for input pulse widths of 6 nsec to 7 nsec. For input pulses of 3 nsec to 7 nsec width and of pulse height exceeding the threshold by 50 mV, the maximum repetition rate was measured as 92 MHz.

The delay through the circuit is 20 nsec. The change of delay as function of input pulse height (slewing) is <1 nsec when the height of a 6-nsec wide input pulse is changed from twice the threshold to four times the threshold.

ACKNOWLEDGEMENTS

The work described here was performed in collaboration with Mr. Dale Horelick and Mr. Raymond S. Larsen, to whom we are indebted for stimulating discussions and comments. The assistance of Mrs. Ann Johnson is gratefully acknowledged.

FOOTNOTES AND REFERENCES

1. See e.g. R. Littauer, Pulse Electronics (McGraw-Hill, New York 1965).
2. A. Barna, J. H. Marshall, and M. Sands, A nanosecond coincidence circuit using transistors, Nucl. Instr. and Methods 7, 124-134 (1960).
3. MECL-II Series of Motorola Semiconductor Products Inc., Phoenix, Arizona.
4. Type LEA00010B02 of KMC Semiconductor Corporation, Long Valley, N. J.
5. A. Barna and E. L. Cisneros, Integrated circuit interfaces between nuclear instrument module and emitter-coupled logic levels, Nucl. Inst. and Methods (in print).
6. Trademark of Gardner Denver Co., Quincy, Illinois.
7. Type 8136-KG1-30 Augat Inc., Attleboro, Mass.

FIGURE CAPTIONS

1. Schematic diagram of the MC1023L integrated circuit. Two circuits as shown and a -1.2 V reference supply are included in a 14-pin dual-in-line package.
2. Schematic diagram of the MC1025L dual-in-line integrated circuit.
3. Schematic diagram of the Schmitt Trigger circuit. All transistors are $\frac{1}{2}$MC1025L; Q1A, Q1B, and Q3B utilize 1 section each, Q2A, Q2B, and Q3A 4 sections each.
4. Schematic diagram of the Shaper circuit. All integrated circuits are $\frac{1}{2}$MC1023L with unused inputs connected to -5.25 V and unused outputs left open-circuited. Voltages on lines A, B, and C are controlled by a 3-pole 3-position WIDTH switch according to the table.
5. Schematic diagram of the Output Stage.[5]
6. Two views of the discriminator.

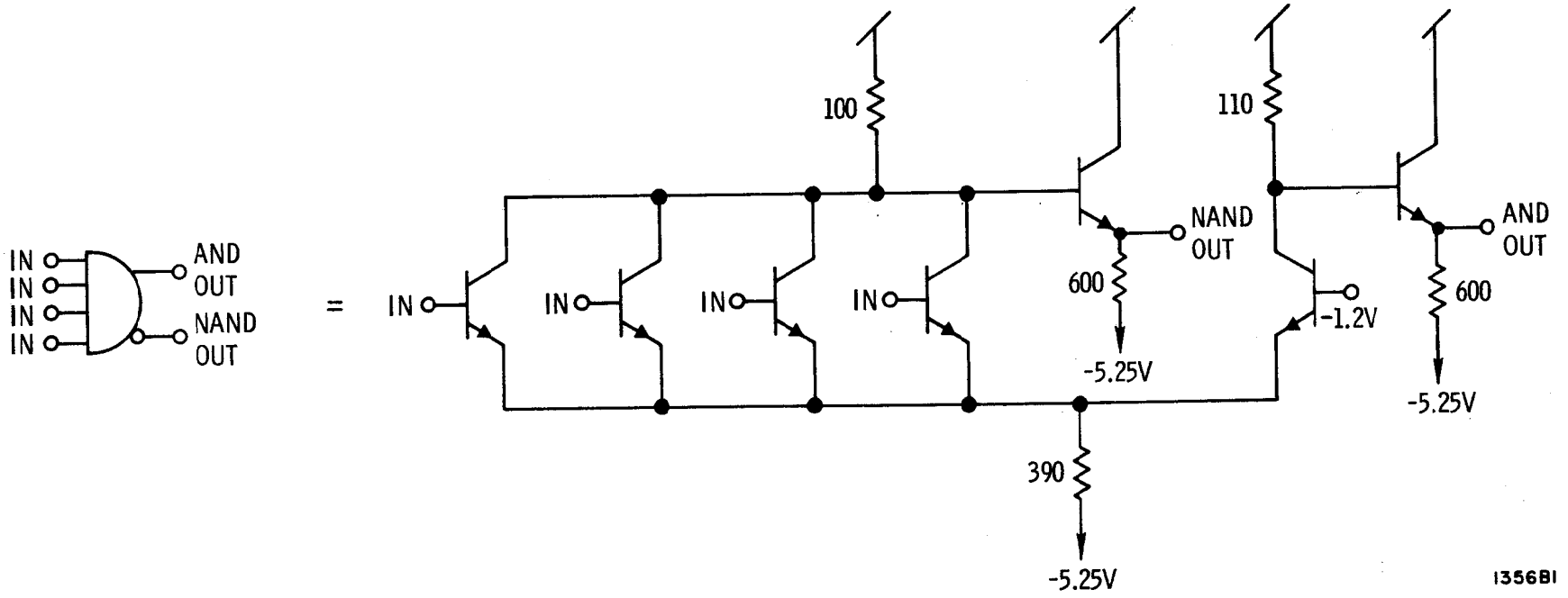

IN
IN
IN
IN
AND
OUT
NAND
OUT
=
IN
IN
IN
IN
100
600
-5.25V
390
-5.25V
NAND
OUT
110
-1.2V
AND
OUT
600
-5.25V
1356B1

Fig. 1

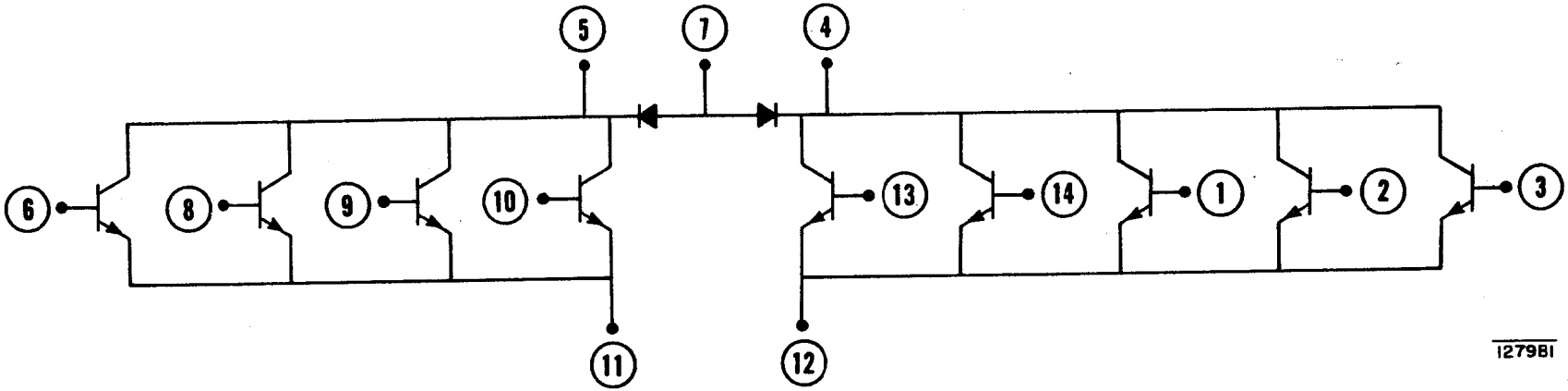
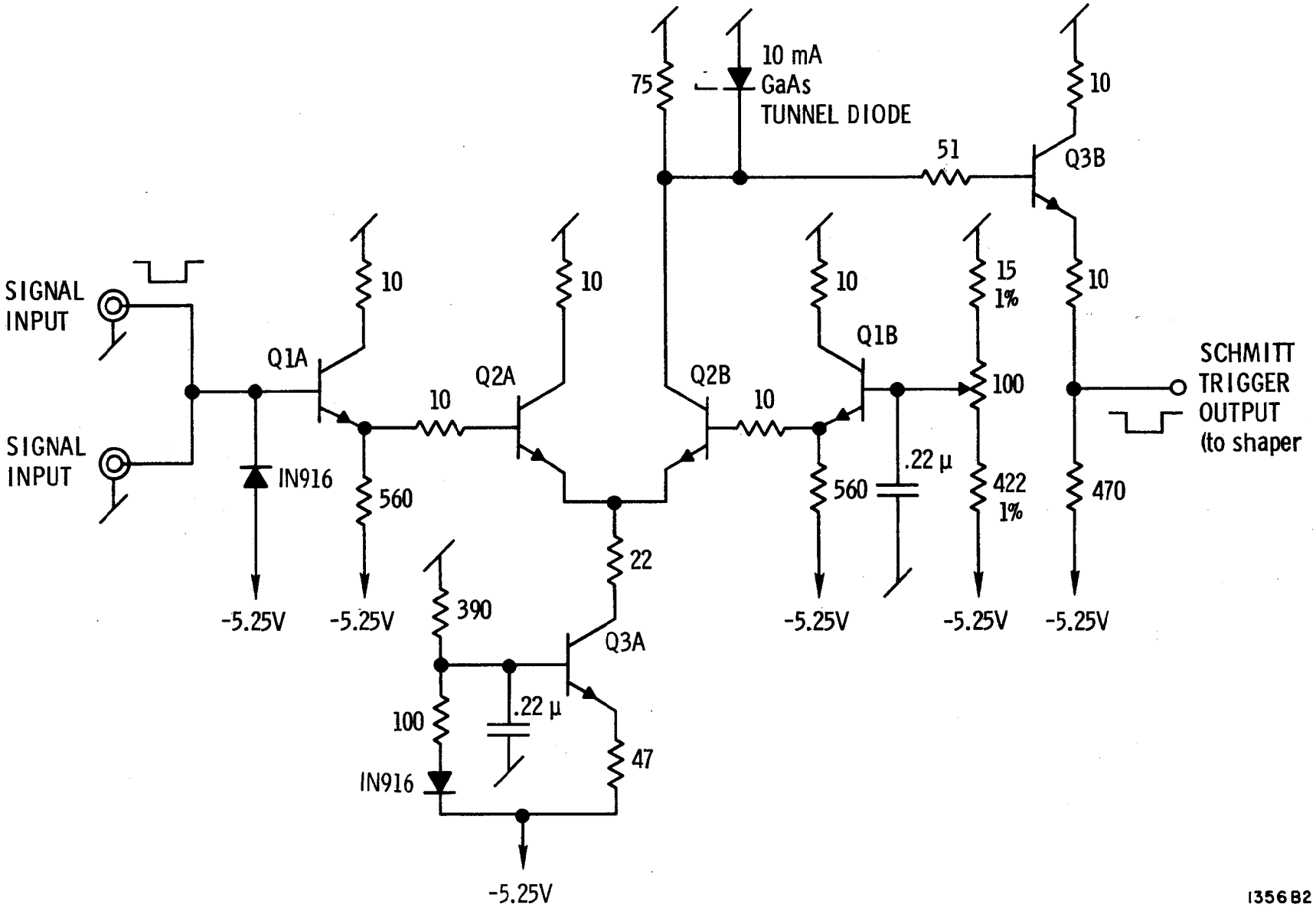


Fig. 2


10 mA
GaAs
TUNNEL DIODE
75
10
51
Q3B
SIGNAL
INPUT
SIGNAL
INPUT
Q1A
Q2A
Q2B
Q1B
10
10
10
10
10
15
1%
100
SCHMITT
TRIGGER
OUTPUT
(to shaper
IN916
560
10
560
.22 µ
422
1%
470
22
390
Q3A
100
.22 µ
47
IN916
-5.25V
-5.25V
-5.25V
-5.25V
-5.25V
-5.25V
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1356B2

Fig. 3

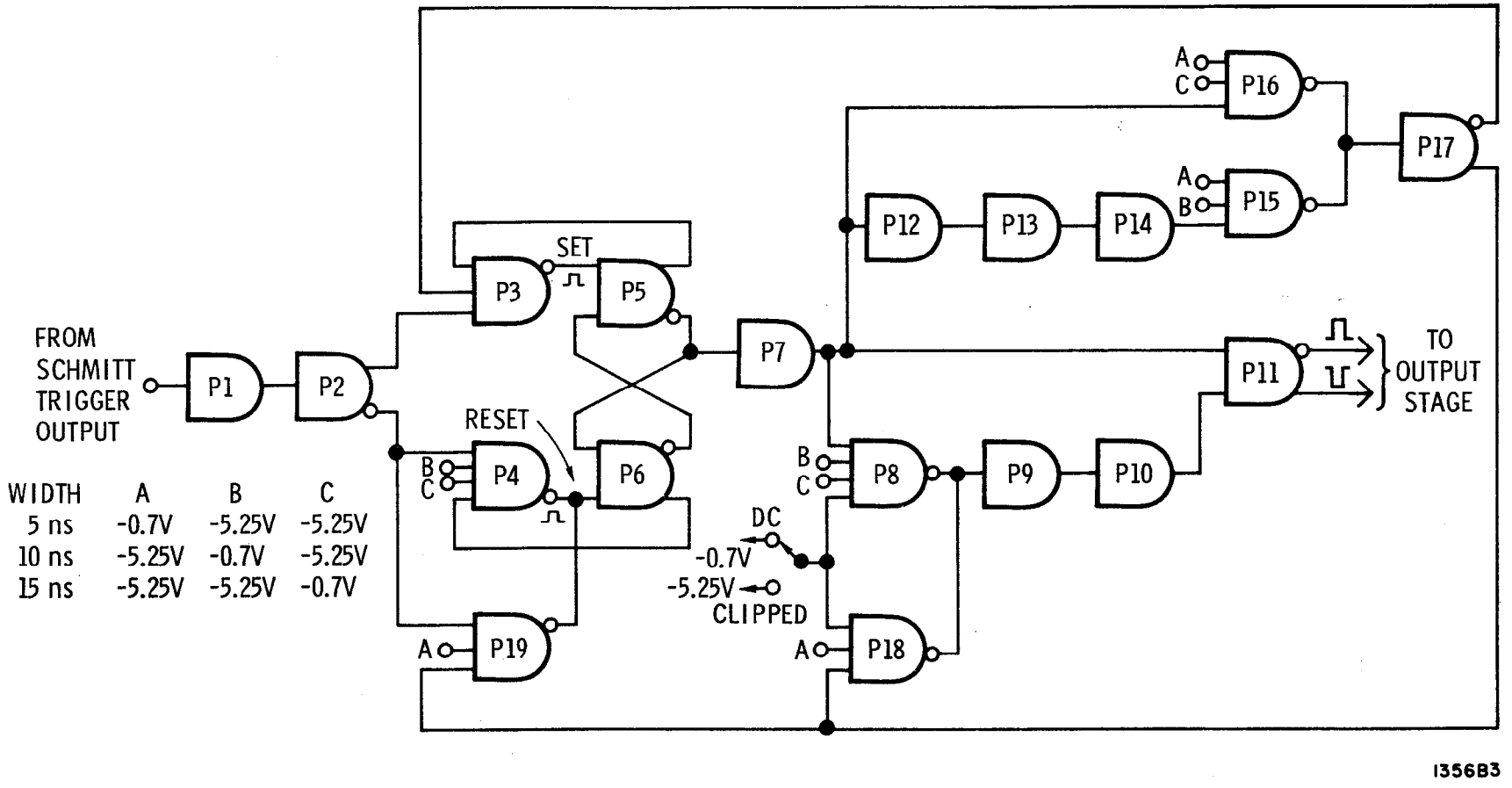
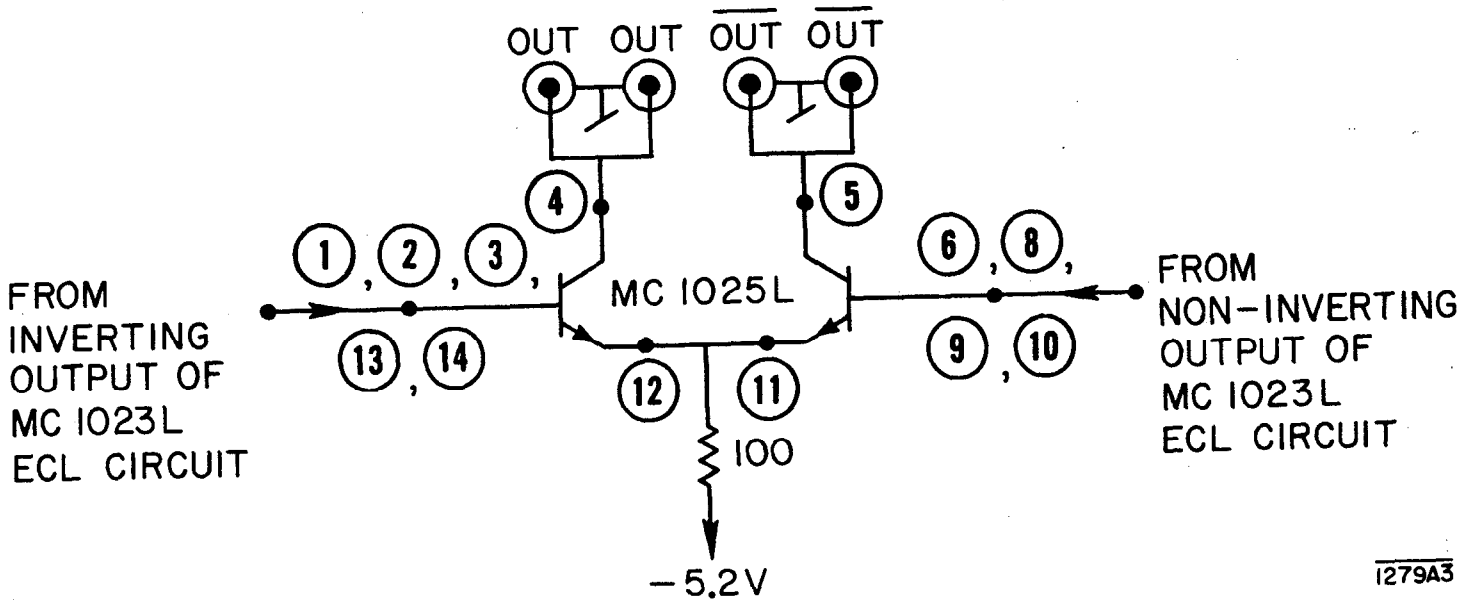

FROM
SCHMITT
TRIGGER
OUTPUT
P1
P2
P3
SET
P5
P4
RESET
P6
P7
P8
P9
P10
P11
P12
P13
P14
P15
P16
P17
P18
P19
A
B
C
DC
-0.7V
-5.25V
CLIPPED
TO
OUTPUT
STAGE
WIDTH A B C
5 ns -0.7V -5.25V -5.25V
10 ns -5.25V -0.7V -5.25V
15 ns -5.25V -5.25V -0.7V
135683

Fig. 4


OUT
OUT
$\overline{OUT}$
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4
5
1, 2, 3,
6, 8,
FROM
INVERTING
OUTPUT OF
MC 1023L
ECL CIRCUIT
MC 1025L
13, 14
12
11
9, 10
FROM
NON-INVERTING
OUTPUT OF
MC 1023L
ECL CIRCUIT
100
−5.2V
1279A3

Fig. 5

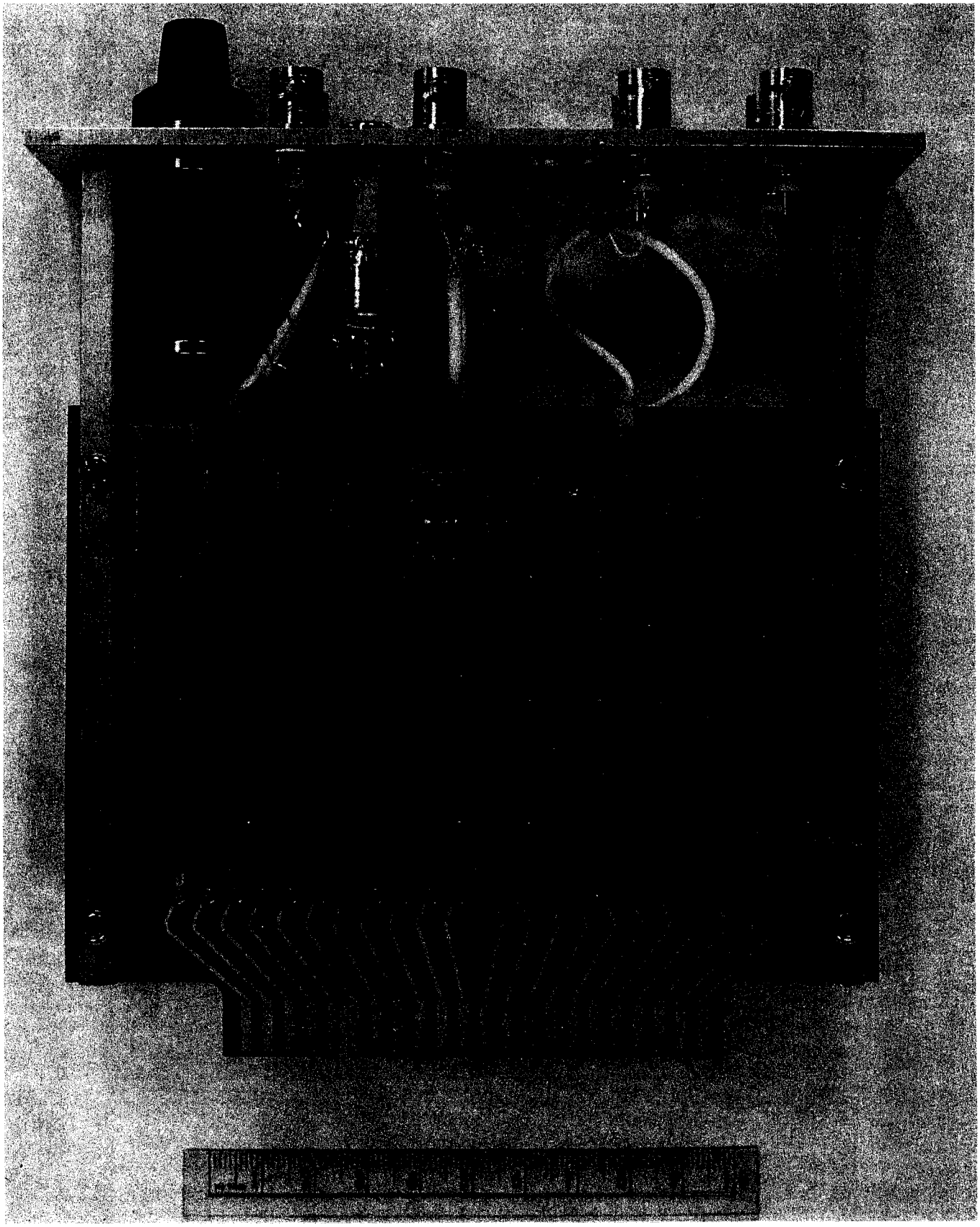

Fig. 6a

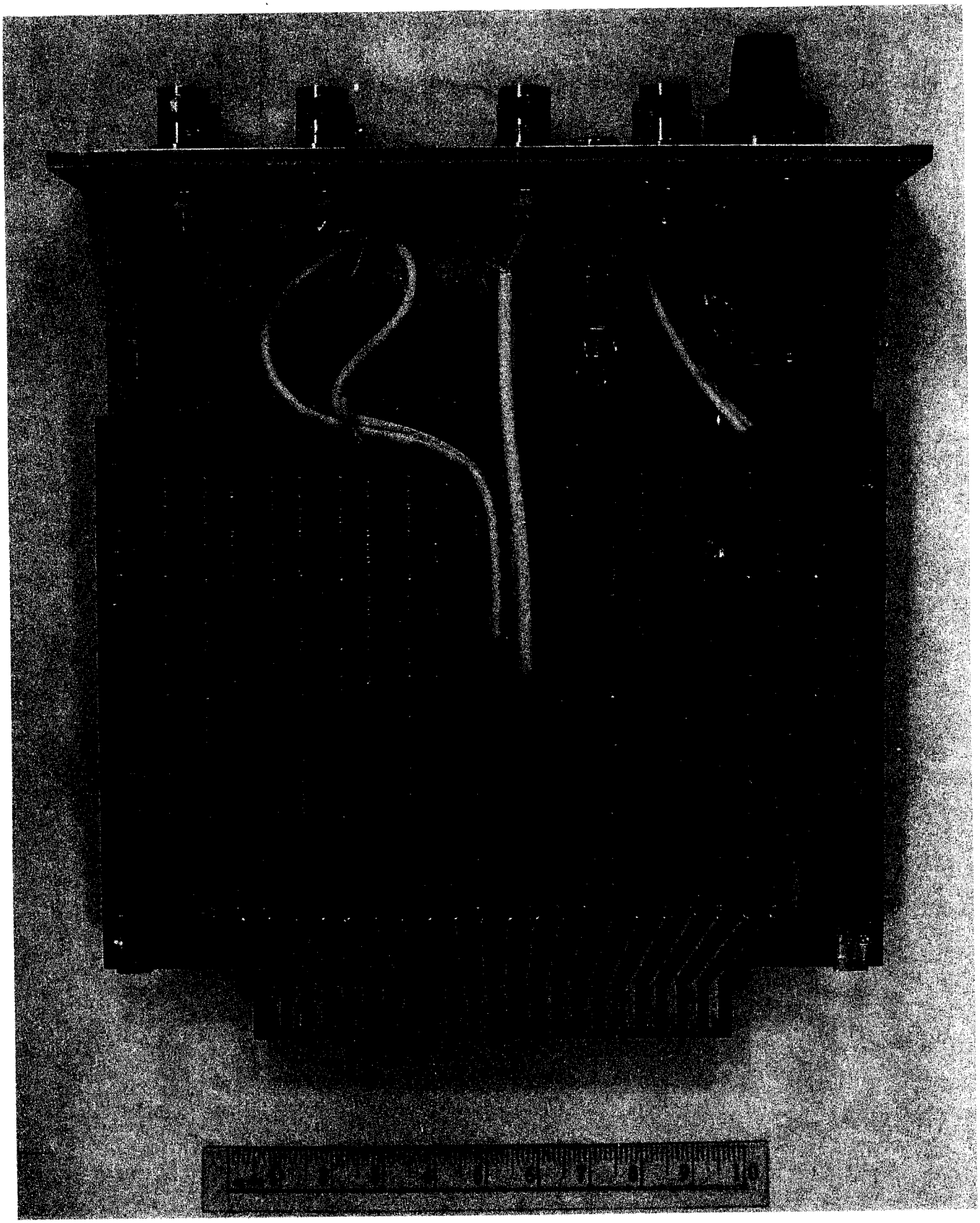

Fig. 6b