SLAC-PUB-590
May 1969
(EXPI)

ELECTRONIC INSTRUMENTATION FOR A NON-INTERCEPTING GAMMA-BEAM MONITOR*

A. Barna, E. L. Cisneros, C. Dale,
and A. Johnson

Stanford Linear Accelerator Center
Stanford University, Stanford, California 94305

ABSTRACT

The paper describes the electronic instrumentation for a nonintercepting gamma-beam monitor in use at the 82" bubble chamber at the Stanford Linear Accelerator Center. The position and the intensity of the beam are monitored by four shower-counters placed behind a 2-mm collimator. The bubble chamber flash-illumination and camera-advance are inhibited when the beam is not centered within 0.5 mm.

(Submitted to Nucl. Instr. and Meth.)

*Work supported by the U. S. Atomic Energy Commission.

1. INTRODUCTION

The instrument described here has been developed for use with a non-intercepting shower-counter gamma-beam monitor at the 82-inch bubble chamber at the Stanford Linear Accelerator Center. The purpose of the instrument is to inhibit the flash illumination and the camera advance if certain conditions on the position and on the intensity of the gamma-beam are not satisfied.

The position and the intensity of the beam are monitored by four shower counters.[1] The total charge of each counter during each 40-nsec-wide beam pulse is digitized by a seven-bit analog-to-digital converter.[2] The flash illumination and the camera advance can be inhibited by upper and lower limits set on each of the four charges, on the sum of the four charges, on the difference of the charges of the left and right counters, and on the difference of the charges of the up and down counters. The differences can be also monitored by means of two panel meters.

2. DESCRIPTION

A block diagram is shown in Fig. 1, simplified schematic diagrams in Fig. 2 through Fig. 6.[3]

Seven-Bit Analog-to-Digital Converter[2]

The converter has a maximum sensitivity of 1.2 p Coul/count and linearity, resolution, and stability of $< 1\%$ for up to ≈ 160 counts. The digital data is available on 8 data lines (not utilized here), and as a 10 MHz square-wave train starting 15 μsec after the beam pulse.

Shaper (Fig. 2)

The 10-MHz square-wave trains of the four analog-to-digital converters are shaped by four shaper circuits. Each shaper provides two outputs: A train of 10-nsec-wide pulses for the mixer, and a square-wave train for the digital storage register.

Adder and Divider (Fig. 3)

The number of pulses in the four pulse trains from the shaper are added by mixing, and the sum is utilized to monitor the beam intensity. The sum is also divided by a factor of 1, 2, 4, 8, 16, or 32, and the divided sum is used to set upper and lower limits on the sum of the four counter charges by means of additional equipment not shown.[4]

Scaler Buffers

The four scaler buffers process the output signals from the shapers to accumulating scalers. These scalers can be reset at each beam pulse (once every 2 seconds) to show the counts accumulated during the latest beam pulse.

Arithmetic Unit

The number of pulses in each of the four square-wave outputs of the shapers are stored in four 8-bit digital storage registers.[5] The stored data can be utilized to set individual upper and lower limits on the four counter charges by means of eight digital comparators (Fig. 4).[6]

The contents of the four registers are converted to 0V to -10V by means of four digital-to-analog converters.[7] Two linear substractors (Fig. 5) provide the difference of the left and right, and the up and down counter charges. Two panel meters display these differences, and upper and lower limits are set on each by means of two sets of analog comparators (Fig. 6).

All together, sixteen inhibit signals are produced in the arithmetic unit. These are OR-ed and the result interrogated by a pulse delayed by 40 μsec from the beam; the flash illumination and the camera advance of the bubble chamber are inhibited by the presence of any one or more than one, of the 16 inhibit signals.

3. CONSTRUCTION

The seven-bit analog-to-digital converters are constructed in a one-width module;[8] the shapers, the adder, and the divider in a two-width module, the scaler buffers in a two-width module, and the arithmetic unit in a four-width module. The analog-to-digital converters utilize a printed-circuit board,[2] the scaler buffers conventional construction, the remainder is built on wire-wrap[9] boards. A photograph of the shapers, the adder, and the divider is shown in Fig. 7. Two views of the arithmetic unit are shown in Fig. 8, two views of the wire-wrap[9] plug-in board with the analog circuitry in Fig. 9.

4. OPERATION

The instrument has been operated with the bubble chamber utilizing the gamma-beam, and it has exhibited a high degree of reliability. Stability and accuracy of the analog arithmetic circuitry has been better than 1%.

ACKNOWLEDGEMENTS

The writers are indebted to Drs. Roger Gearhart and Joseph Murray for their guidance, suggestions, and patience during the development of the instrument.

REFERENCES AND FOOTNOTES

1. The showers are produced by the periphery of the gamma-beam passing through a 2 mm collimator.
2. D. Porat and K. Hense, "Seven-Bit Analog-to-Digital Converter for Nanosecond Pulses," Nucl. Instr. and Methods 67, 229 (1969).
3. Complete documentation is available from the writers upon request.
4. Designed and built by John Saarloos of the Lawrence Radiation Laboratory, University of California, Berkeley, California.
5. Each 8-bit register consists of two Signetics N8281A 4-bit counters.
6. Based on a design described in Digital Logic Handbook, (Digital Equipment Co., Maynard, Massachusetts 1967).
7. Each 8-bit digital-to-analog converter consists of a Sprague UM1200 and a Sprague UM1210 4-bit converters.
8. The modules conform to Nuclear Instrument Module Standard TID-20893. They have a 200 mm height and a 250 mm depth. Widths of the one-width, two-width, and four-width modules are 34 mm, 68 mm, and 136 mm, respectively.
9. Registered trademark of the Gardner-Denver Co., Quincy, Illinois.

FIGURE CAPTIONS

1. Block diagram.
2. Shaper, one of four.
3. Mixer and divider.
4. Digital comparator, one of eight. Connections are shown for lower limit comparators; for upper limit comparator, connections of the binary-coded 16-position thumbwheel switches (S1, S2, $\overline{S2}$, etc.) and the connections to the digital storage register ($\overline{8}$, 16, $\overline{16}$, etc.) have to be substituted by their complements.
5. Linear subtractor, one of two.
6. Analog comparators, one of two sets.
7. A photograph of the shapers, the adder, and the divider.
8. Two views of the arithmetic unit.
9. Two views of a wire-wrap[9] plug-in board.

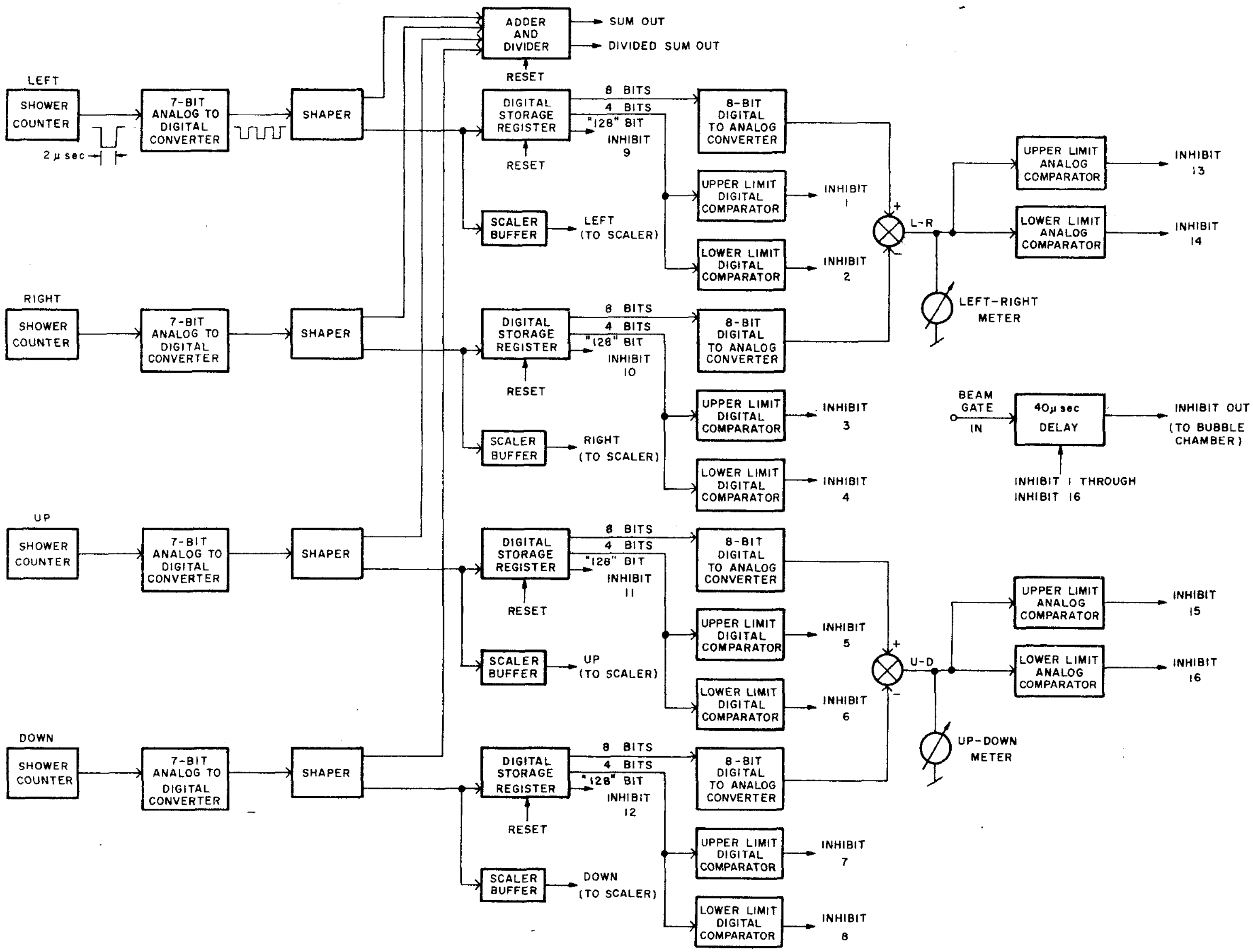
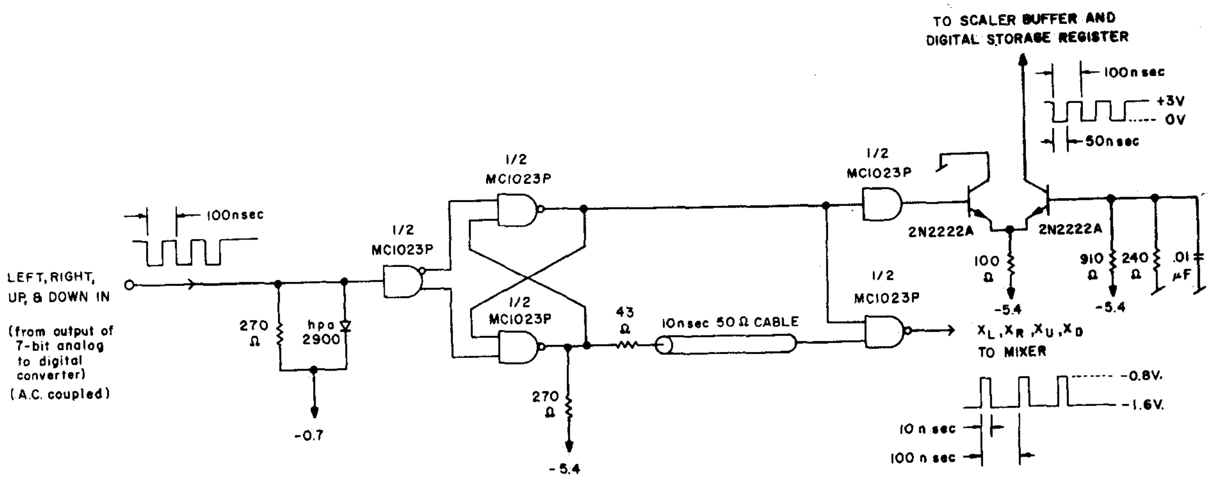


FIGURE 1

1352A1



1352A2

FIGURE 2

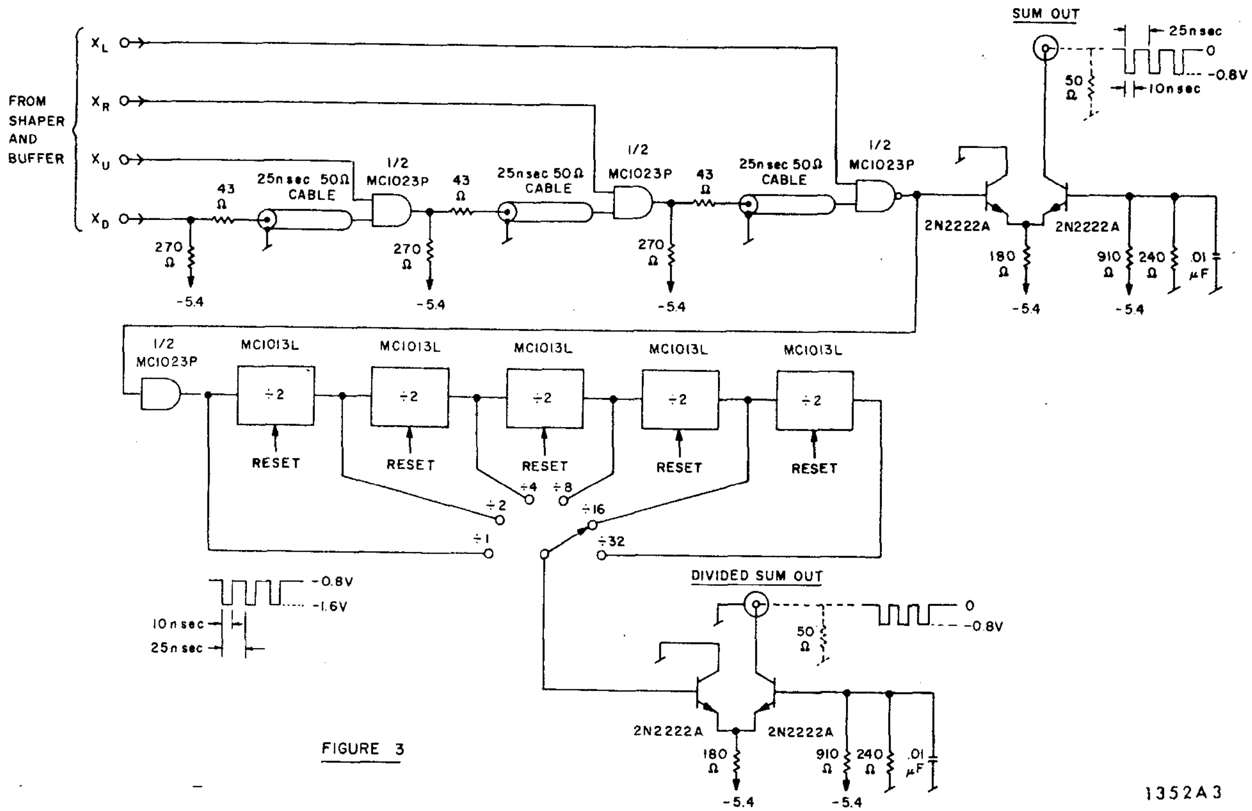
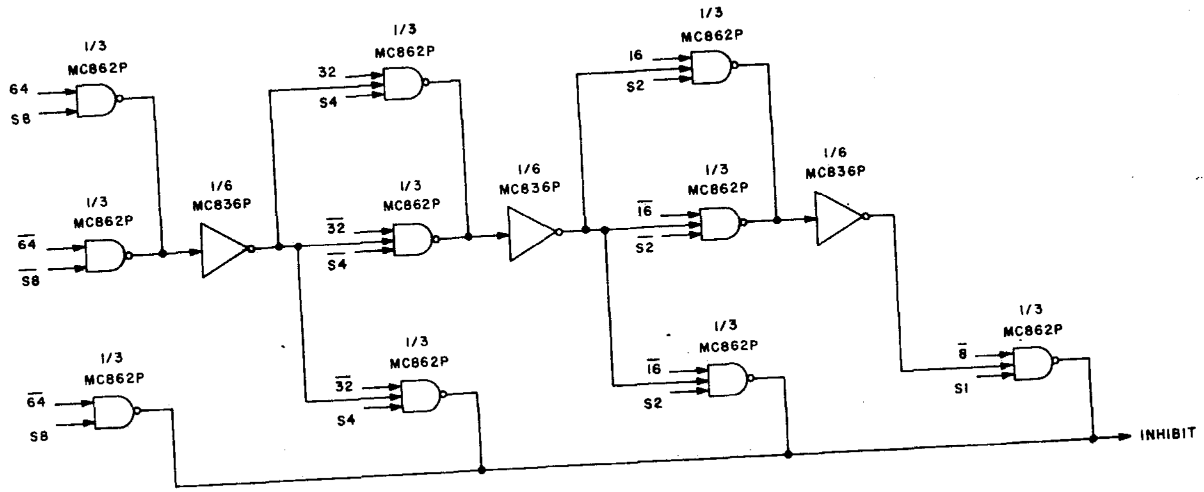


FIGURE 3

1352A3



1352A4

FIGURE 4

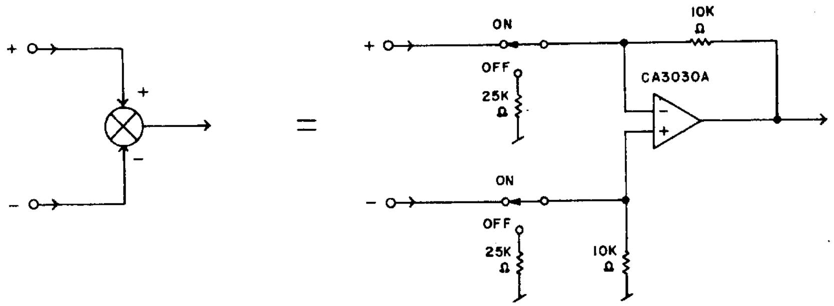


FIGURE 5

1352A5

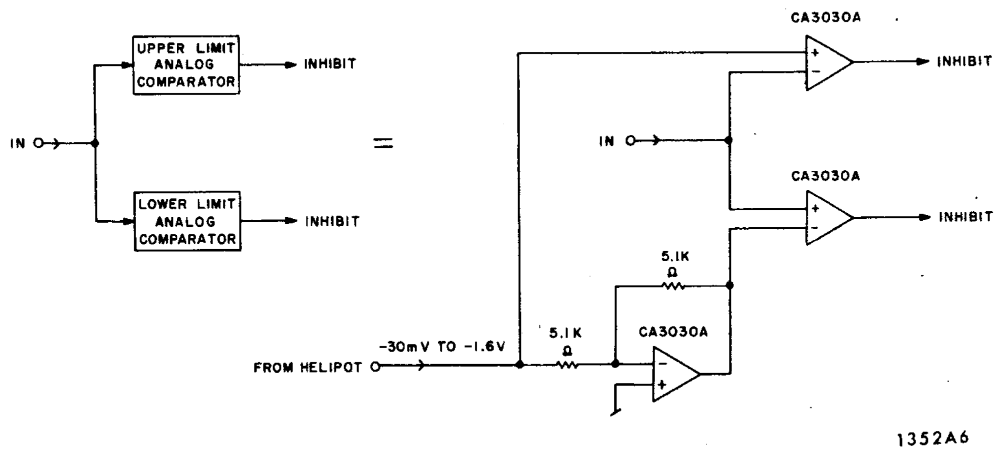

UPPER LIMIT ANALOG COMPARATOR
INHIBIT
IN
LOWER LIMIT ANALOG COMPARATOR
INHIBIT
=
CA3030A
INHIBIT
IN
CA3030A
INHIBIT
5.1K Ω
-30mV TO -1.6V
5.1K Ω
CA3030A
FROM HELIPOT
1352A6

FIGURE 6

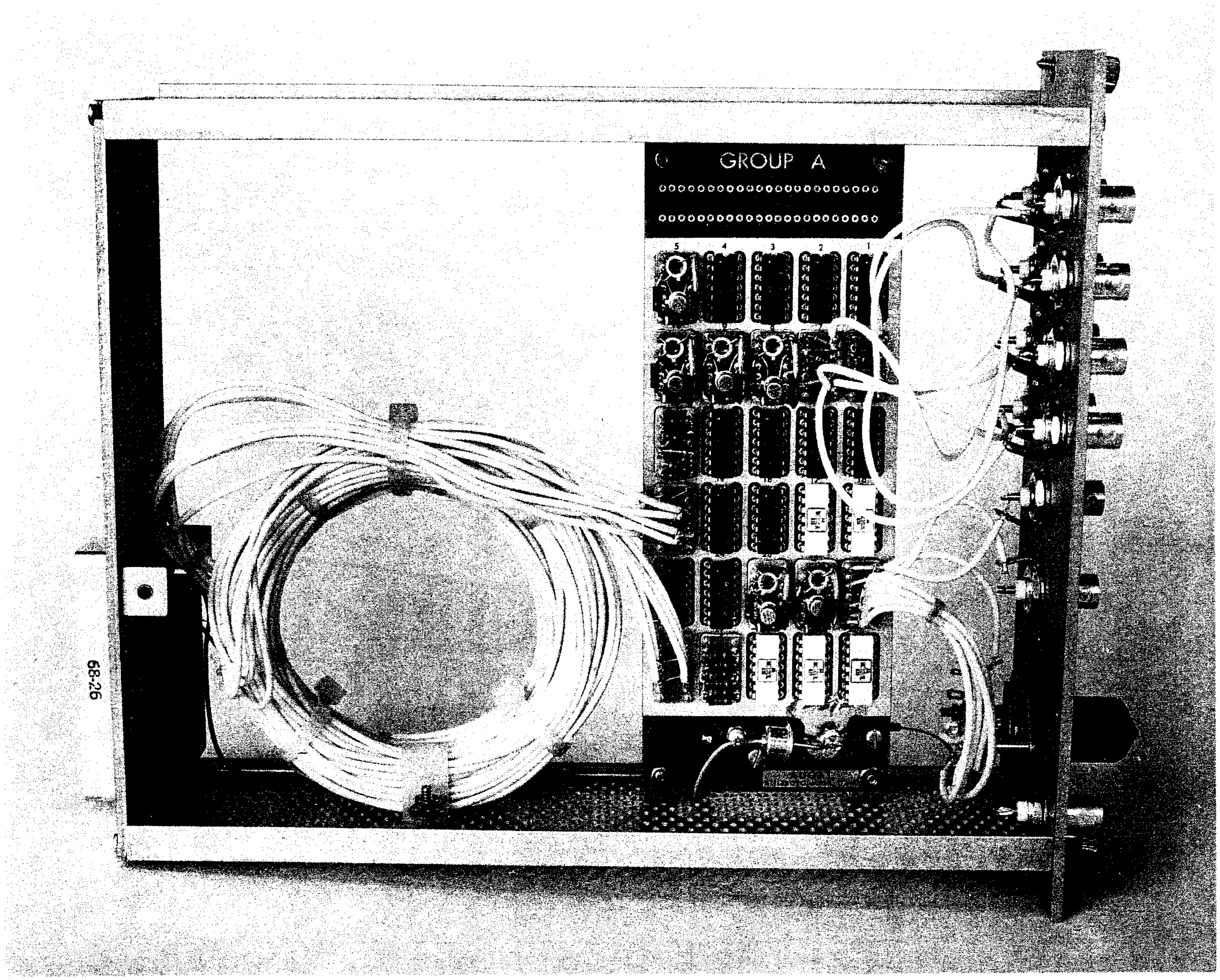


Fig. 7

1352A7

1352A8

Fig. 8a

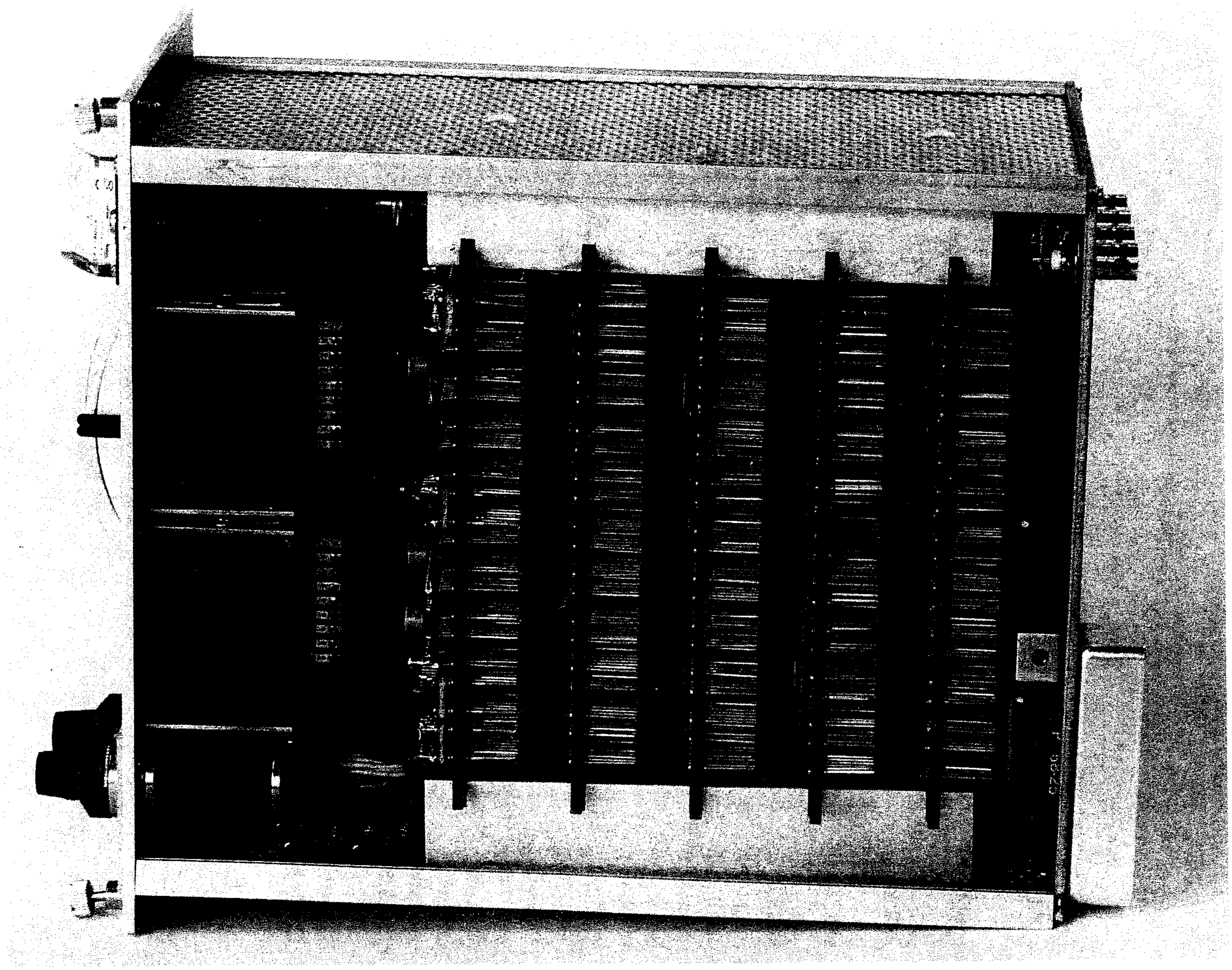


Fig. 8b

1352A9

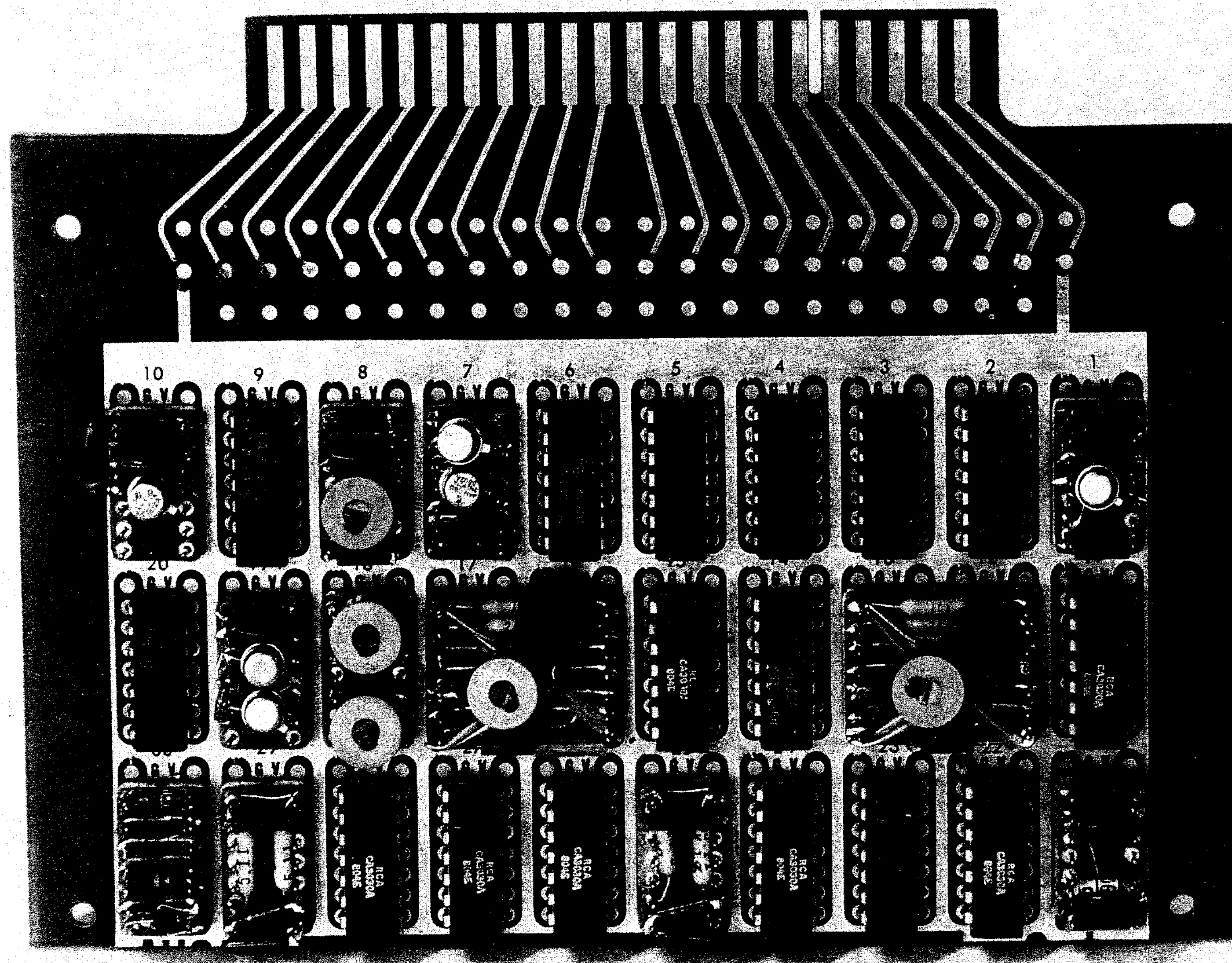
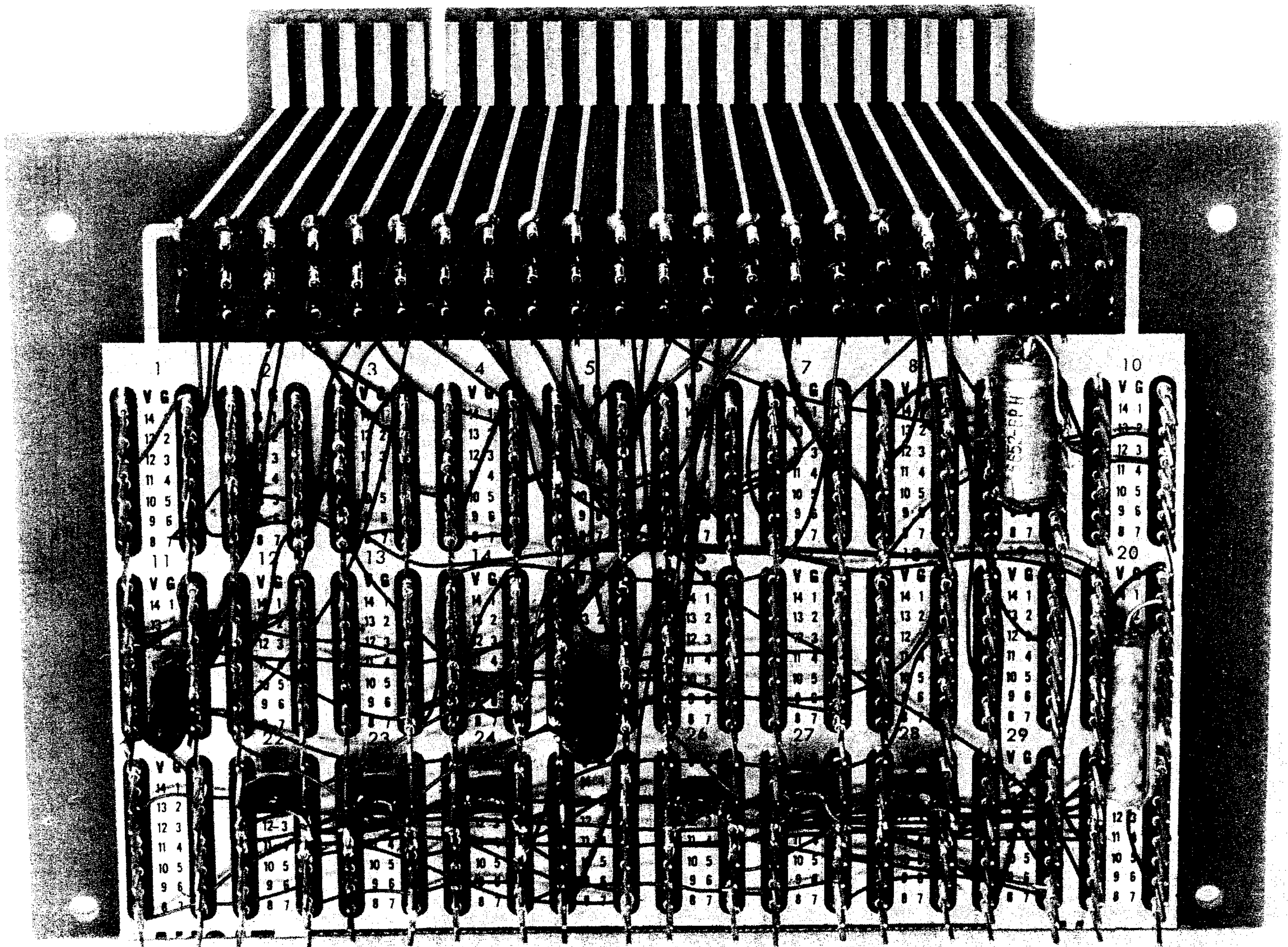


Fig. 9a

1352A10



1352A11

Fig. 9b