8 CHANNEL, 40 MHZ, 12 BIT
“VME”
ANALOG DIGITIZER

MODEL VTR812 / 40

Joerger ENTERPRISES, INC.
166 LAUREL ROAD, EAST NORTHPORT, NY 11731 U.S.A.

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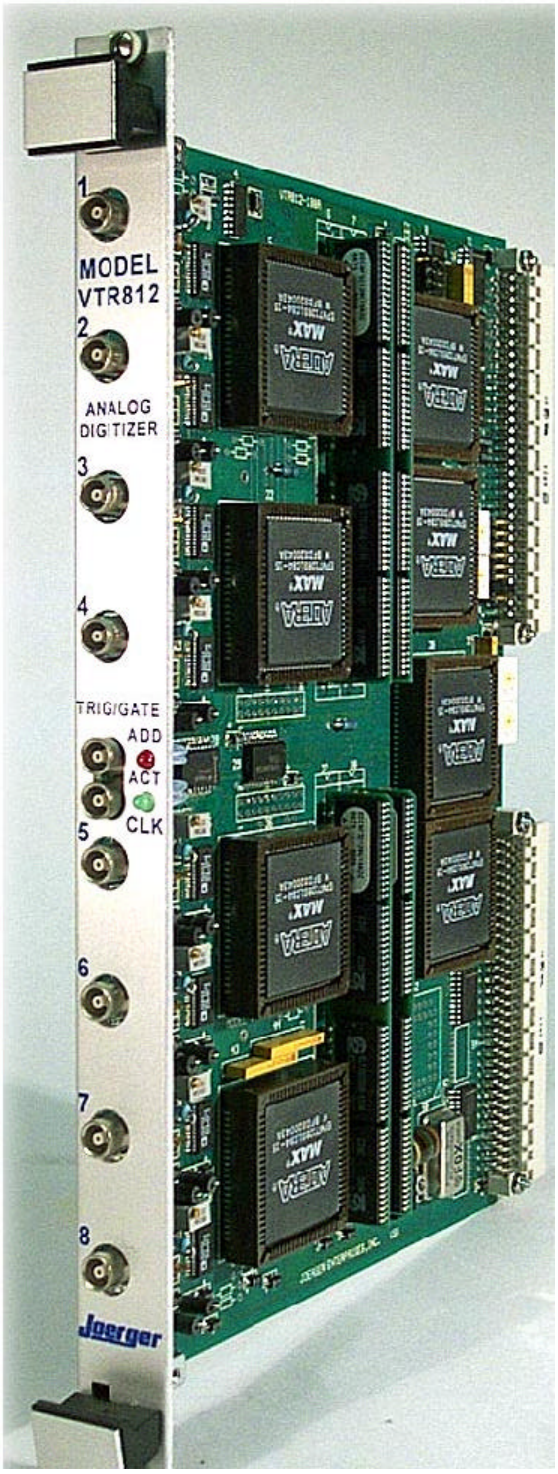
MODEL VTR812

EIGHT CHANNEL, 40 MHZ, 12 BIT "VME" ANALOG DIGITIZER WITH 8M WORD SRAM



FEATURES:

- EIGHT, INDEPENDENT, 40 MHZ, 12 BIT ANALOG DIGITIZERS
- 1M SAMPLES OF SRAM PER CHANNEL, 8M SAMPLES TOTAL
- PROGRAMMABLY SELECTABLE FOR 4 CHANNEL OPERATION WITH 2MSAMPLES OF SRAM PER CHANNEL
- WIDE INPUT BANDWIDTH FOR GOOD WAVEFORM TRACKING
- HIGH NOISE IMMUNITY AND LOW CHANNEL CROSSTALK
- REAL TIME READ OUT OF ADC DATA IN ACTIVE MODE
- HIGH SPEED READOUT, 2 CHANNELS PER READ
- PRE/POST & MULTIPLE PRE/POST TRIGGER RECORDING WITH ADDRESS LOCATIONS INTERNALLY STORED TO FACILITATE DATA READ OUT
- POST AND MULTIPLE POST TRIGGER RECORDING
- PROGRAMMABLE INTERNAL CRYSTAL CLOCK OR EXTERNAL CLOCK
- HIGH COMMON MODE REJECTION
- INTERRUPT STRUCTURE
- BLOCK TRANSFER MODE D32:BLT
- **" LABVIEW "** SOFTWARE AVAILABLE

APPLICATIONS:

- HIGH SPEED, ACCURATE, ANALOG DIGITATION
- REAL TIME DIGITAL RECORDING OF ANALOG SIGNALS
- OSCILLOSCOPES, USING ITS HIGH IMPEDANCE AND MEMORY PROVIDES FAST ACCURATE RECORDING AND TROUBLE SHOOTING OF ANALOG DATA

The JOERGER ENTERPRISES, INC. MODEL VTR812 Series contains eight, 12 bit analog digitizers in a 6U, VME module. The **Model VTR812/40** operates at 40Mhz and the **Model VTR812/10** operates at a clock speed of 10Mhz. It is completely self contained and can store 1M samples of data per channel in SRAM, 8M samples total in a single width. When additional memory is required the module may be programmably set to operate as a 4 channel recorder with 2M samples of data per channel. To insure the highest performance the ADC is driven differentially with an offset to match its input. A wideband, differential input/output amplifier with an output offset capability designed specifically for this type ADC is used. The differential inputs are buffered providing the module either single ended or differential inputs with an input impedance over 10MΩ's. This balances the module in either mode and for single ended inputs the return line is grounded internally. When lower impedances are required an on board jumper is provided for each channel. For single ended inputs the impedance is 50Ω's and for differential inputs 100Ω's is provided. Other impedances can be provided.

Its high input impedance and large memory allows it to be used in place of an oscilloscope for both analog monitoring and trouble shooting. When looking for problems even in slow speed systems it provides a complete picture of the event.

Each channel accepts an analog signal, digitizes it using a programmable internal crystal clock or an external clock and loads the data into its SRAM. To interface the ADC's output, high speed PLD's are used. In addition to writing the memory and gating the data for readout the active ADC's data is also latched and available for real time readout over the VME bus while the module is recording. The "active" data is also available from the P2 connector. Allowing the user the ability to monitor the ADC's output provides a wide possibility for uses in system operation. To insure high speed readout each module is read out 2 channels at a time on 32 data lines.

The addressing, address control, ADC interface, VME logic and commands are all done with high speed PLD's. The analog inputs have been designed to handle a wide variety of signals. Special care in the layout and filtering provide both low channel crosstalk and low noise, often a problem with multi-channel analog input modules. When an application requires filtering, external filters are recommended. All channels use a common clock and control signals and operate simultaneously.

Each channel's data is in a contiguous block of memory with the module's base address selected by switches. The three control and status registers are accessed via short addressing to a 256 byte block. The control register selects the operating parameters for the module. The gate duration register contains the number of samples to be taken after a trigger. The location register contains the pointer to the next memory address to be filled with data. In addition to controlling the module with registers it can be Triggered, Disarmed and the memory location can be reset with separate commands without data. To simplify system implementation " LABVIEW " software is available.

To add flexibility the module may be operated in several modes. Post trigger, multiple post trigger, pre/post trigger and multiple pre/post trigger operations can be selected. To facilitate

data readout the stop address is recorded in all modes and the number of valid cycles is recorded and can be readout. In multiple pre/post trigger the memory can be divided in up to 16 equal sections. Each section runs a normal pre/post trigger cycle and records that sections stop address in memory so data for that section can be read. This is repeated for each trigger and stops when the memory is full.

The external TRIGGER/GATE input allows the module to use this signal as a trigger or gate signal and is selected in software. When GATE is selected this determines the cycle gate time. If TRIGGER is selected the gate time is set by the internal gate duration register. In TRIGGER mode the post trigger cycle starts digitizing on receipt of a trigger, takes the number of samples set by the gate duration register, stops and sets an interrupt. If the Auto Reset is on, the next trigger will reset the location counter to zero and overwrite the previous samples. For multiple post trigger operation, Auto Reset is turned off and each following trigger will not reset the location counter and the samples will be stored sequentially until the memory is full. If the "Memory Wrap" mode is off, and the cycle is complete, an interrupt is set and further triggers are ignored. If the Wrap mode is on, when the memory fills, it will start overwriting the memory and accept triggers until the module is disarmed. In the pre/post trigger mode the module starts taking data when the unit is armed and cycles through the memory overwriting old data. Upon receipt of a trigger the module takes the number of samples set by the duration counter, stops and sets an interrupt. The complete memory is used with the post trigger samples preset by the gate duration. The balance of the memory contains pretrigger information. If GATE is selected its pulse width will determine the gate times.

SPECIFICATIONS

ANALOG INPUT	±2 Volts, single ended standard, differential input optional
INPUT IMPEDANCE	10 MΩ's, jumper selectable to 50Ω's, other impedance's optional
COMMON MODE REJECTION	-70dB min., DC to 500khz
CHANNEL CROSSTALK	-66dB min. at 10Mhz input rate
BANDWIDTH	VTR812/10, 10Mhz Minimum
	VTR812/40, 40Mhz Minimum
ACCURACY	. .05% typical
DIFFERENTIAL LINEARITY	±.3LSB, Typ., No missing codes
CONVERSION RATE	VTR812/10, 10Mhz maximum, VTR812/40 40Mhz maximum, selected from 8 scaled frequencies using either the SYS Clock, on board crystal oscillator or an external clock.
RESOLUTION	12 Bits.
MEMORY	128K samples/channel Standard, 512K, 1M samples/channel Optional.
	Note: module may be set to 4 channel mode doubling the
memory per	channel
TRIGGER/GATE INPUT	TTL Level, trigger or gate mode internally selectable
CLOCK INPUT	TTL Level
VME INTERFACE	D8 (EO), D32, D32:BLT, A16, A32 SLAVE
CONTROL/STATUS REGISTERS	Read/Write: select clock rate, disarm at cycle completion, bus trigger, external clock, external trigger, external gate, reset on trigger, wrap, post, pre/post and multiple pre/post trigger modes, arm, active, set to 4 channel mode, last channel read

GATE DURATION REGISTER	Read/Write: select the number of conversions to perform after a trigger.
LOCATION REGISTER	Read/Write: a pointer to the next sample location
INTERRUPT ID REGISTER	Read/Write Status/ID word
IRQ LEVEL REGISTER	Read IRQ level jumpers
SYSRESET, INT. RESET	Resets module and control register, aborts recording cycle
POWER REQUIREMENTS:	+5V, -12V, 13 watts total
SIZE:	Single width “VME” 6U card
CONNECTORS:	TRIGGER/GATE, CLOCK; LEMO RA00250
	SINGLE ENDED INPUTS; LEMO RA00250
	DIFFERENTIAL INPUTS; LEMO RA0302
OPTIONS:	1) MODEL VTR812/10, 10Mhz speed
	2) MODEL VTR812/40, 40Mhz speed
	3) 512K SRAM per channel
	4) 1M SRAM per channel
	5) Multiple pre/post trigger
	6) Differential inputs
	7) Active read out of channels 5-8 on P2

JEI010

PLEASE NOTE: When choosing an analog input module many factors should be considered. It is
recommended reading “SELECTING AN ANALOG INPUT MODULE” on our web site: www.joergerinc.com , under “What’s New”

166 LAUREL ROAD • EAST NORTHPORT, NY 11731, USA
1-631-757-6200 • FAX 1-631-757-6201 • Email: joerger@joergerinc.com • web: www.joergerinc.com

INTRODUCTION

The Joerger Enterprises, Inc. VTR812 contains eight complete digitizer channels and the VMEbus interface. This design uses a 12 bit ADC, with up to 1M samples of static memory for each of the eight channels. A four channel mode via software (see C/S#3 table) allows using four channels with double the memory per channel. The board appears to the bus as a 16M byte (for all memory options) RAM card in extended address space with registers in VMEbus I/O space for status and control. Memory may be accessed from the VMEbus as Lword only (D32), 2 channels at a time, channels 1, 2, 3 and 4 on D0-D15 and channels 5, 6, 7 and 8 on D16-D31. Registers are accessed as bytes, D8(O), located in short (I/O) address space. Readout of the registers is always allowed. Read out of the memory or writes to the registers are only allowed if the module is not active (except for a software trigger, setting digitizer armed bit to zero, master reset, IRQ reset, Disable-IRQ and internal reset). Provision is made for using internal or external triggers, digitizer clocks and gate signals. Block transfers are supported (D32:BLT) and an interrupt structure is provided. The 12 bit digitized data for channels 1, 2, 3 and 4 is read out on D0-D11(MSB). The 12 bit digitized data for channels 5, 6, 7 and 8 is read out on D16-D27(MSB). The output coding is straight binary. Unused data bits D12-15 and D28-31 return logic zero.

The standard single ended analog input impedance is greater than 10Mohm and can be terminated with an on board jumper to use 50 ohm termination (or other resistor values can be substituted). The input range is -2v to +2v. Differential inputs are optional.

8 bit Read/Write parameter registers, located in VME I/O space are as follows:

Control and Status Registers (C/S)	These bit-significant registers select the operating characteristics of the board. (3 bytes)
Memory Location Counter	A pointer to the next data sample location to be filled with the digitizer data. (3 bytes)
Gate Duration Register	The number of conversions to be performed following a trigger (3 bytes)
Interrupt Status/ID Register	The response word for an IACK cycle (1 byte)
IRQ Level Register	The IRQ level set with the on board jumpers I1,I2 and I4. read only (1 byte)
Read Last Register	The location to readout the last conversion from the selected 2 channels (Lword access,4 byte)
Post Counter / Pmem Register	Read Post Ctr, Write Pmem Read Reg. (1 byte)
Mutli Pre/Post Register *	Select Multi Pre/Post mode and parameters (1 byte)

* = Optional Feature

The following AM Codes are used:

All Register access	Short Address D8(O)	AM 2D or 29
Memory access	Extended Address D32	AM 09 or 0D
	Extended Block Transfer D32	AM 0B or 0F
Internal Reset	Short Address	AM 1D or 19

OPERATION

Several operating modes are possible, each of them defined by setting values into the above registers. All eight channels operate simultaneously with the same setup parameters. The module must be in the armed state to be active and digitizing. The module may be disarmed at any time by writing to Add 25H or by setting the Digitizer Armed bit in the C/S#2 register to zero, this will stop any cycle without changing the setup (see tables). If the digitizer is active, an internal interrupt will be set and if the IRQ is enabled a bus IRQ will be generated.

READ LAST: The analog converters are always converting whether the digitizer is armed and active or not. This allows the readout of the last conversion from 2 selected channels at any time, (even if the module is active). Similar to a free running ADC with readout 'on the fly'. This can be used to track the inputs for setup, offset or test without any special setup and without changing any mode the module may already be set to. The channels can even be sampled during an active cycle. This is in addition to the data being written into the onboard memory and does not interfere with normal operation in any way. The 2 channels to be monitored are selected in C/S#3, and are readout using Lword access from an I/O address (10H). See tables.

4 CHANNEL MODE: If more memory per channel is needed a bit in the C/S#3 register may be set which will double the memory for 4 channels. This is done by disabling channels 2,4,6 &8 inputs and allowing channels 1,3,5 &7 to use the adjacent channel's memory. This would make an 8 channel 128ks/ch VTR812 into a 4 channel 256ks/ch VTR812. The readout is organized so that the ch1 (odd channel) data is read first from the ch1 area and the second half of ch1 data is read from the normal ch2 (even channel) area. At the end of a cycle if the memory location counter contains a number larger than the memory per channel for the normal (8 channel) mode, then the location is actually in the 'even channel' memory block, since after the counter reaches the end of the 'odd channel' memory size it starts to fill the next block which is the 'even channel' memory block. As an example for a 128ksample/ch module: if the memory location counter reads out as 138k, then the actual location in memory is 10ksamples into the 'even channel' memory block. The 138k number is not used to directly address the memory location as the memory location counter usually would in the normal 8 channel mode. Use the Memory Map to calculate these locations. Note that for most memory size options the data memory map contains "holes" in used addresses between channels. The other channels are paired similarly, 3&4,5&6, and 7&8. See the Data Memory Space (4 channel mode) table for further information. The 4-channel mode is useable with any operating mode except Multi Pre/Post Trigger mode. The memory location and gate duration registers have the extra bit needed for the double length memory operation.

NORMAL MODE: In the Normal mode, digitizing begins at the selected clock rate following a trigger and takes the number of samples contained in the Gate Duration Register and loads them in memory. The Auto-Reset bit of the C/S#2 register determines whether the location counter is reset by a trigger event. When the Location Counter is not reset by each trigger, data following successive triggers is stored sequentially in memory until the memory is filled, (multi post trigger cycles). If Auto Reset is on, old data is overwritten by new data each time a trigger is received. Operation is the same if using the External Gate mode.

The Wrap bit in the C/S#2 register determines if the digitizer stops at the end of memory or wraps around and begins to refill memory starting at location zero. If the Wrap bit is off and the memory has been filled, the module is disarmed and additional triggers are ignored This will occur regardless of the condition of the Disarm at End of Cycle bit. The Wrap bit operates the same in the External Gate mode.

The Disarm at End of Cycle bit determines if the module is disarmed at the end of a cycle. When the gate time is over, active goes to off, the module is disarmed and will not respond to any further triggers or external gate inputs until it is rearmed.

PRE/POST TRIGGER MODE: This mode is started by writing to the C/S#2 register twice with the appropriate bits set. The first write sets the Pre/Post Trigger bit and the second write uses that bit in the register to set active and start the digitizer. In this mode, the digitizer continuously fills the total memory and is stopped by triggering. As in the Normal Mode, the number of conversions that follow the trigger is given by the value stored in the Gate Duration Register. This allows the capture of data both before and after a trigger. The Wrap bit must be set to allow the memory to be refilled after the address counter overflows. If the memory should not be overwritten set the Wrap bit to zero. The Disarm at End of Cycle bit is available in this mode also. In addition to triggered operation, this mode can be combined with the External Gate mode allowing capture of data before an external gate. The Pre/Post Trigger bit in the C/S#2 register is reset on active going to zero. A bit in the C/S#1 Register will be set if the memory address counter overflows at least once.

* MULTI-PRE/POST TRIGGER MODE: This mode allows for multiple (the total memory divided into 2, 4, 8 or 16 segments) Pre/Post Trigger cycles to be recorded along with the address of the last sample recorded in each segment. The Post Counter stores the number of post trigger cycles completed, can be readout while module is active and is useable in all modes, with a maximum count of 16. The last address of each completed post trigger cycle is stored in the 'Post Trigger Memory' (Pmem) and is read by first selecting the cycle by writing to the Pmem Register and then reading that cycles last address using the VME addressing listed in the following tables.

The mode is set up by writing to the Multi Pre/Post Setup Register and setting the Gate Duration Register with the number of post trigger samples required. The digitizing is started by writing to the C/S#2 register twice with the appropriate bits set. The first write sets the Pre/Post Trigger bit and the second write uses that bit in the register to set active and start the digitizer. The samples are recorded in the first segment in a circular overwriting manner until a trigger is received. Then the number of post trigger samples selected are taken, the address of the last sample for that segment is stored in the Pmem, and the next segment is automatically started. When the last segment (2, 4, 8 or 16) is completed, the module is disarmed ,the digitizing is stopped and the total memory is filled. The module can also be stopped by disarming it at any time and the Post Counter will contain the number of completed segments.

Data readout is organized as follows. The number of segments set, the total module memory size and the channel number determine the lowest and highest VME address for each segment. The address for the last sample of each segment is retrieved by writing the PMem Register with the cycle number (see tables) and then reading the PMem address from Short I/O address space (see tables) for that cycle. This allows readout of the total memory and all the PMem addresses for later organization or readout of specific samples for each segment. A readout of the Post Counter will always contain the number of completed post trigger cycles and should be used to read the number of valid segments recorded. The Post Counter can be also be read while the module is active to check on the progress of the cycles.

Multi Pre/Post mode is not available in 4 channel mode.

EXTERNAL GATE MODE: This mode is enabled by setting the Ext Gate Enabled bit in the C/S#2 and arming the module. Setting this bit automatically changes the function of the Trig/Gate input to the gate function. This allows the front panel input to start (up edge) and stop (down edge) the digitizer. The Disarm at End of Cycle, Wrap, Pre/Post Trigger and Auto Reset bits all work normally and the interrupt is set when the Trig/Gate input goes to zero (active also goes to zero).

RESET: A complete reset of the module (the same as Sysreset) is done with an I/O write to Address base +01H, or a write to the Master Reset bit in C/S#3 register or (for backwards compatibility) with a write to the base short address with AM code 1D or 19. This will abort the cycle, reset the control register, reset the gate register, reset the memory location register, reset the interrupt ID register, reset the internal interrupt latch, take any pending IRQ off the bus and enable the IRQ response. This leaves the VTR812 in it's power up condition with all registers set to zero.

INTERRUPT: The interrupt level is selected by two sets of on board jumpers. One jumper to select the IRQ line (IRQ1 to IRQ7 or none, IRQ1 is standard) and three jumpers to code the selected level into the IRQ Level Register (I1, I2, I4). These jumpers must match. See the partial board layout page. The IRQ may be disabled by setting a bit in C/S#3 register (this also clears the internal IRQ status). The status of the internal interrupt may be read from CS#3, and can be used with the Disable IRQ bit set. The interrupt is set in any operating mode when a cycle is completed (active goes to zero). The IRQ is reset on acknowledge for an addressed IACK cycle (ROAK), or by Sysreset, Internal Reset, Master reset or Reset IRQ in C/S#3. The byte stored in the Status/ID Register is returned with the acknowledge for the IACK cycle.

FRONT PANEL SIGNALS: The standard analog signal inputs are single ended and use single pin Lemo connectors, 2pin Lemo connectors are used for the optional differential inputs. The Trig/Gate in and Clock in use standard single pin Lemo connectors and are normally low TTL signals. The rising edge is the active edge for the trigger and clock inputs. The clock input must meet or exceed a minimum pulse width both high and low of 45ns. The Ext Clock frequency range for the specified performance is 40Mhz to 1Khz min. The gate input uses the rising edge to start the digitizer and the down edge to stop. Setting the Ext Gate Enabled bit in C/S#2 automatically changes the function of the Trig/Gate input to the gate function.

VMEbus ADDRESSING: The digitizer board occupies 16M bytes of extended address memory space (all memory versions), and 256 bytes of short I/O space. The memory access base address is set with two hexadecimal switches, labeled 'EXT.ADDRESS' 'A24-27' (SW3) and 'A28-31' (SW4), msb. The I/O base address is set with two hexadecimal switches labeled 'I/O 8-11' (SW1) and 'I/O 12-15' (SW2),msb. See the partial board layout page. Memory on the board is accessed as Lword (D32) only. Blocks for block transfer mode must start on a 256 byte boundary (A1 - A7 = 0) When the board is active, the memory cannot be accessed for read or write from the bus. The board will not acknowledge. To read or write memory the digitizer must be disarmed.

ID Register: The ID register contains a byte to identify the module and it’s major options. See the tables for full information.

ANALOG INPUT:

Standard Input Range	-2v to +2v
Input Impedance	The standard single ended analog input impedance is greater than 10Mohm and can be terminated with an on board jumper to use 50 ohm termination (or other resistor values can be substituted). Differential inputs are optional.
Offset error	±2 bits typical
Gain error	±1 bit typical
Bandwidth	40Mhz typical
Crosstalk	<1 Lsb typical (10 mhz sine input)

DATA READOUT:

The 12 bit digitized data for channels 1, 2, 3, and 4 is read out on D0-D11(MSB). The 12 bit digitized data for channels 5, 6, 7, and 8 is read out on D16-D27(MSB). Unused data bits D12-15 and D28-31 return logic zero. The output coding is straight binary. The data is normally read out of the onboard memory after a digitizing cycle is complete, but another readout method is available similar to a free running ADC with readout 'on the fly'. See Read Last section above. See the Memory map for the data location of the channels.
The Memory Location Counter contains the next location to be filled with data. After a cycle, this is used to organize the data for readout and to find the location of the trigger in Pre/Post Trigger mode. This is a word location and the value must be quadrupled for the bus memory address.

MEMORY MAP

DATA MEMORY SPACE (8 channel mode)

Channel	128K version ∗ 128K samples/channel Address A23 - A0	512K version ∗ 512K samples/channel Address A23 - A0	1M version 1M samples/channel Address A23 - A0
CH1	00 0000 - 07 FFFF	00 0000 - 1F FFFF	00 0000 - 3F FFFF
CH2	40 0000 - 47 FFFF	40 0000 - 5F FFFF	40 0000 - 7F FFFF
CH3	80 0000 - 87 FFFF	80 0000 - 9F FFFF	80 0000 - BF FFFF
CH4	C0 0000 - C7 FFFF	C0 0000 - DF FFFF	C0 0000 - FF FFFF
CH5	00 0000 - 07 FFFF	00 0000 - 1F FFFF	00 0000 - 3F FFFF
CH6	40 0000 - 47 FFFF	40 0000 - 5F FFFF	40 0000 - 7F FFFF
CH7	80 0000 - 87 FFFF	80 0000 - 9F FFFF	80 0000 - BF FFFF
CH8	C0 0000 - C7 FFFF	C0 0000 - DF FFFF	C0 0000 - FF FFFF

∗ Addresses are not contiguous, there are 'holes' between channels

Note: Ch1,2,3 &4 data on D0-D15. Ch5,6,7 & Ch8 data on D16-D31
All addresses are +extended base address

DATA MEMORY SPACE (4 channel mode)

Channel	128K version ∗ 256K samples/channel Address A23 - A0	512k version ∗ 1M samples/channel Address A23 - A0	1M version 2M samples/channel Address A23 - A0
CH1	00 0000 - 07 FFFF	00 0000 - 1F FFFF	00 0000 - 3F FFFF
	40 0000 - 47 FFFF	40 0000 - 5F FFFF	40 0000 - 7F FFFF
CH3	80 0000 - 87 FFFF	80 0000 - 9F FFFF	80 0000 - BF FFFF
	C0 0000 - C7 FFFF	C0 0000 - DF FFFF	C0 0000 - FF FFFF
CH5	00 0000 - 07 FFFF	00 0000 - 1F FFFF	00 0000 - 3F FFFF
	40 0000 - 47 FFFF	40 0000 - 5F FFFF	40 0000 - 7F FFFF
CH7	80 0000 - 87 FFFF	80 0000 - 9F FFFF	80 0000 - BF FFFF
	C0 0000 - C7 FFFF	C0 0000 - DF FFFF	C0 0000 - FF FFFF

∗ Addresses are not contiguous, there are 'holes' between channels

Note: Ch1 &3 data on D0-D15. Ch5 & Ch7 data on D16-D31
All addresses are + extended base address

CONTROL / STATUS REGISTER #1 (C/S#1)

Short Base + 21H (A7-A0) (DS0=1) BYTE 1

D7	NOT USED	
D6	1=ENABLE P2 REALTIME READOUT	OPTIONAL R/W
D5	1=DISARM AT END OF CYCLE	R/W
D4	1=MEMORY COUNTER OVERFLOW	READ ONLY
D3	NOT USED	
D2	DIGITIZE RATE SEL BIT 2	R/W
D1	DIGITIZE RATE SEL BIT 1	R/W
D0	DIGITIZE RATE SEL BIT 0	R/W

RATE SELECT CODING

BIT 0-2	INT CLK RATE	EXT CLK RATE *
0	40MHz	EXT CLK ÷ 1
1	20MHz	EXT CLK ÷ 2
2	10MHz	EXT CLK ÷ 4
3	4MHz	EXT CLK ÷ 10
4	2MHz	EXT CLK ÷ 20
5	1MHz	EXT CLK ÷ 40
6	0.500MHz	EXT CLK ÷ 80
7	0.250MHz	EXT CLK ÷ 160

* The external clock input must meet or exceed a minimum pulse width both high and low of 12ns.
Frequency range from 40Mhz to 1Khz min for the specified performance.

CONTROL / STATUS REGISTER #2 (C/S#2)

Short Base + 23H (A7-A0) (DS0=1) BYTE 1

D7	1=DIGITIZER ACTIVE	READ ONLY
D6	1=DIGITIZER ARMED *	R/W
D5	1=PRE/POST TRIGGER ENABLED **	R/W
D4	1=WRAP MODE ENABLED ***	R/W
D3	1=AUTO RESET LOCATION COUNTER	R/W
D2	1=EXT TRIGGER ENABLED	R/W
D1	1=EXT GATE ENABLED	R/W
D0	1=EXT DIGITIZE CLOCK ENABLED ****	R/W

* To abort (stop) cycle set Digitizer Armed to zero. If active an interrupt will be set.

** To start, this bit must be written to twice, it is automatically reset on active going to zero.
Valid in Ext Gate mode also, leading (up) edge of gate input acts like a trigger.

*** Wrap Mode must be enabled for Pre/Post Trigger Mode or recording will stop on memory address overflow.

**** The external clock input must meet or exceed a minimum pulse width both high and low of 45ns.
Frequency range from 40Mhz to 1Khz min for the specified performance.

CONTROL / STATUS REGISTER #3 (C/S#3)

Short Base + 0DH (A7-A0) (DS0=1) BYTE 1

D7	1=SET TO 4 CHANNEL MODE (Double Memory for Channels 1, 3, 5 & 7) (Input Channels 2, 4, 6 & 8 aren't used)	R/W
D6	1=ENABLE REALTIME DAC OUTPUT	OPTIONAL R/W
D5	READ LAST, SEL CH BIT2	R/W
D4	READ LAST, SEL CH BIT1	R/W
D3	Not used	
D2	1=DISABLE IRQ *	R/W
D1	Write ≡ 1 = RESET IRQ Read ≡ 1 = INTERNAL IRQ IS SET	R/W
D0	1=MASTER RESET	WRITE ONLY

* Resets to Enable IRQ (1 ≡ IRQ is Disabled)

READ LAST, SELECT CHANNEL CODING

BIT 1-2	CHANNEL
0	CH1 & CH5
1	CH2 & CH6
2	CH3 & CH7
3	CH4 & CH8

ADDRESS A7-A0 + Short Base address

01H	MASTER RESET	Write only (no data looked at)
09H	Interrupt Status/ID Register	IACK cycle response byte. Read / Write
0BH	IRQ Level Register	Readout of on board IRQ jumpers coded onto D0 - D2 Read Only
0DH	Control Status Register #3	
0FH	ID Register (Module Type)	
10H	Read Last Data	Lword access of 4 bytes of data See C/S Reg#3 to select channels
21H	Control Status Register #1	
23H	Control Status Register #2	
25H	Disarm	Write only (no data looked at)
27H	Low Byte Gate Duration Register	The number of conversions following a trigger. Read / Write
29H	Mid Byte Gate Duration Register	
2BH	High Byte Gate Duration Register	
2DH	Software Trigger	Write only (no data looked at)
2FH	Reset Memory Location Counter	Write only (no data looked at)
31H	Low Byte Memory Location Counter	Word location. For memory address the value must be quadrupled. Read / Write
33H	Mid Byte Memory Location Counter	
35H	High Byte Memory Location Counter	
∗37H	Low Byte PMem Address	Word location. For Post Trigger last address the value must be quadrupled. Read only
∗39H	Mid Byte PMem Address	
∗3BH	High Byte PMem Address	
∗3DH	Pmem Counter/Register	Read Pmem Ctr, Write Pmem Read Reg
∗3FH	Mutli Pre/Post Register	Select Multi Pre/Post mode and parameters. Read / Write

∗ = Optional Feature

MASTER RESET

Short Base + 01H (A7-A0) (DS0=1) BYTE 1

Write only Data ignored, complete reset, same as SYSRESET or Power up
Resets all registers to zero and aborts any cycle.
Does not change channel memory data.

IRQ LEVEL REGISTER

Short Base + 0BH (A7-A0) (DS0=1) BYTE 1

D7	NOT USED	
D6	NOT USED	
D5	NOT USED	
D4	NOT USED	
D3	NOT USED	
D2	I4 IRQ level select on board jumper	Read Only *
D1	I2 IRQ level select on board jumper	Read Only *
D0	I1 IRQ level select on board jumper	Read Only *

IRQ jumper coding

D0-D2	LEVEL
0	NOT USED
1	IRQ1 (As Shipped)
2	IRQ2
3	IRQ3
4	IRQ4
5	IRQ5
6	IRQ6
7	IRQ7

DISARM

Short Base + 25H (A7-A0) (DS0=1) BYTE 1

Write only, Data ignored. Resets Digitizer Armed bit in C/S#2

SOFTWARE TRIGGER

Short Base + 2DH (A7-A0) (DS0=1) BYTE 1

Write only, Data ignored. Same as front panel Trig input

RESET MEMORY LOCATION COUNTER

Short Base + 2FH (A7-A0) (DS0=1) BYTE 1

Write only, Data ignored. Not Active only.

ID REGISTER

Short Base + 0FH (A7-A0) (DS0=1) BYTE 1

D7	NOT USED	
D6	NOT USED	
D5	MEMORY SIZE BIT 2	READ ONLY
D4	MEMORY SIZE BIT 1	READ ONLY
D3	MEMORY SIZE BIT 0	READ ONLY
D2	MODULE TYPE BIT 2	READ ONLY
D1	MODULE TYPE BIT 1	READ ONLY
D0	MODULE TYPE BIT 0	READ ONLY

MODULE TYPE CODING

BIT 0-2	MODULE TYPE
0	NOT USED
1	VTR1012A
2	VTR3012A
3	VTR10010
4	VWG
5	VTR812/10
6	VTR812/40
7	NOT USED

MEMORY SIZE CODING

BIT 0-2	MEMORY SIZE
0	128 K
1	256 K
2	512 K
3	1 M
4	2 M
5	4 M
6	8 M
7	NOT USED

GATE DURATION REGISTERS

(# of Post Trigger samples)

LOW BYTE

Short Base + 27H (A7-A0) (DS0=1) BYTE 1

D7	1= 128 Samples	R/W
D6	1= 64 Samples	R/W
D5	1= 32 Samples	R/W
D4	1= 16 Samples	R/W
D3	1= 8 Samples	R/W
D2	1= 4 Samples	R/W
D1	1= 2 Samples	R/W
D0	1= 1 Sample	R/W

MID BYTE

Short Base + 29H (A7-A0) (DS0=1) BYTE 1

D7	1= 32768 Samples	R/W
D6	1= 16384 Samples	R/W
D5	1= 8192 Samples	R/W
D4	1= 4096 Samples	R/W
D3	1= 2048 Samples	R/W
D2	1= 1024 Samples	R/W
D1	1= 512 Samples	R/W
D0	1= 256 Samples	R/W

HIGH BYTE

Short Base + 2BH (A7-A0) (DS0=1) BYTE 1

D7	NOT USED	
D6	NOT USED	
D5	NOT USED	
D4	1= 1048576 Samples	R/W
D3	1= 524288 Samples	R/W
D2	1= 262144 Samples	R/W
D1	1= 131072 Samples	R/W
D0	1= 65536 Samples	R/W

Note: Recommended minimum Gate Duration of 4 samples.

To calculate Gate Duration (# of post trigger samples) add samples of selected bits.

∗ **PMEM (**last memory address for the post trigger cycle selected in PMEM Register)

∗ = Optional Feature

Short Base + 37H (A7-A0) (DS0=1) BYTE 1

Read only, Low byte = A02 - A09

Short Base + 39H (A7-A0) (DS0=1) BYTE 1

Read only, Mid byte = A10 - A17

Short Base + 3BH (A7-A0) (DS0=1) BYTE 1

Read only, High byte = A18 - A21

∗ **PMEM REGISTER / POST COUNTER**

∗ = Optional Feature

Short Base + 3DH (A7-A0) (DS0=1) BYTE 1

D7	NOT USED		
D6	NOT USED		
D5	NOT USED		
D4	PMem/Post Ctr BIT 4 **	Coded	R/W
D3	PMem/Post Ctr BIT 3 **		R/W
D2	PMem/Post Ctr BIT 2 **		R/W
D1	PMem/Post Ctr BIT 1 **		R/W
D0	PMem/Post Ctr BIT 0 **		R/W

** Read = Number of post trigger cycles completed (0-31), valid for all modes

Write = Select the cycle (0-15) for the last address for readout from the PMEM

Address data readout from VME Short Base + :37H, 38H and 3BH

POST COUNTER READ CODING

BIT 0-4	Completed Post Trigger cycles (segments)
0	NONE
1	1
2	2
~	~
31 *	31

* 16 is highest valid number for Multi Pre/Post mode

Note that it does not count triggers but rather completed post trigger cycles. If the end of a post trigger cycle ends exactly at the end of memory and the Wrap bit is off, the Post Counter will read 1 cycle short, Therefore if the gate setup is exactly divisible into the memory size and Wrap is off, the cycles will be complete when the Memory Counter Overflow bit (C/S#1) is set, and the Post Counter will readout 1 cycle short.

PMEM WRITE CODING

BIT 0-4	Get Pmem Address for cycle (segment) number
0	1
1	2
2	3
~	~
15	16

∗ MULTI PRE/POST SETUP REGISTER

∗ = Optional Feature

Short Base + 3FH (A7-A0) (DS0=1) BYTE 1

D7	NOT USED	
D6	NOT USED	
D5	NOT USED	
D4	NOT USED	
D3	NOT USED	
D2	1 = ENABLE MULTI PRE/POST MODE *	R/W
D1	NUMBER OF SEGMENTS BIT 2	R/W
D0	NUMBER OF SEGMENTS BIT 1	R/W

* Not available in 4 channel mode

SEGMENT CODING

BIT 0-1	Total Memory Divided Into
0	2 Segments
1	4 Segments
2	8 Segments
3	16 Segments

NOTES:

Writing to the memory from the bus is allowed if the module is disarmed, Lword access only and 12 bits for each channel (D0-D11 and D16-D27) This will allow a memory check for each channel (2 channels at a time) to be done separately if the memory is suspected to be faulty. The main reason for supporting memory writes is to allow for troubleshooting. Note that the address should be divided by 4 to get the number to write into the memory location register

Identification words can also be stored in each channel before acquiring data. However since only Lword access is supported, you will write 2 channels at a time. The memory location register should be set to the first unused memory location above stored words before arming the module. This will put the ID word in the beginning of memory for each channel but the Auto Reset, Wrap and Pre/Post Trigger bits cannot be set. If the ID words are written to the top of memory where acquired data will not be written, then Auto Reset can be used. Identification words may also be written after the data has been acquired overwriting memory locations as desired.

Rev-C, 07/23/02