PRELIMINARY

SPEAR III MCOR

Frankenstein Board Concept

Thursday, October 17, 2002

The Frankenstein Board Concept moves the ADC's and DAC's to a daughter card on the MCOR30 Controller, the Bride of Frankenstein. An adapter board, the Frankenstein Board, makes it possible to plug a standard VME processor into the MCOR30 Chassis. The Frankenstein board takes standard VME interface on one side, and 8 digital serial interfaces on the MCOR30 side.

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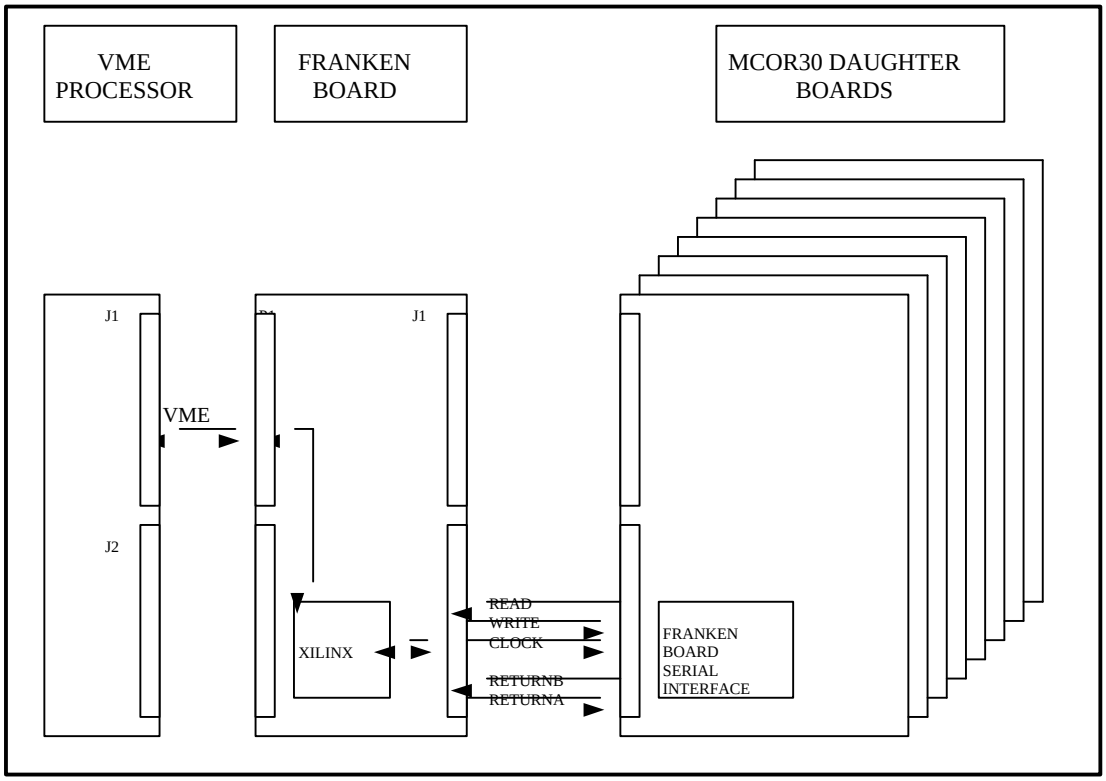

PRELIMINARY

Frankenstein Board Backplane Signals				
Pin		Name	Function for SPEARIII MCOR	Function for Serial Digital Interface
Row	Col			
A	1	SGND0	Ground reference for +Vout and -Vout voltage readback	
A	2	N/A		
A	3	N/A		
A	4	-VOUT0	10:1 readback signal of -OUT	WRITE - Serial data to MCOR interface
A	5	STRB0	Strobe for fault status readback	READ - Serial data from MCOR interface
A	6	+VOUT0	10:1 readback signal of +OUT	CLOCK - Serial interface CLOCK (1Mhz)
A	7	SGND0	Ground reference for MON and FEEDBACK current	
A	8	+REF0	Differential +/-10V FS analog control	RETURNA - Signal return for MCOR
A	9	-REF0		
A	10	MON0	+/-10V FS current readback	
A	11	FAU0	Digital Serial STATUS	
A	12	FDBK0	+/-10V FS current readback	
A	13	SGND1	Ground reference for +Vout and -Vout voltage readback	
A	14	N/A		
A	15	N/A		
A	16	-VOUT1	10:1 readback signal of -OUT	
A	17	STRB1	Strobe for fault status readback	
A	18	+VOUT1	10:1 readback signal of +OUT	
A	19	SGND1	Ground reference for MON and FEEDBACK current	
A	20	+REF1	Differential +/-10V FS analog control	
A	21	-REF1		
A	22	MON1	+/-10V FS current readback	
A	23	FAU1	Digital Serial STATUS	
A	24	FDBK1	+/-10V FS current readback	

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FRANKEN Board

1. VME to MCOR Serial Interface
    a. Map MCOR30 DAC/ADC's into VME registers
    b. Serialize commands from VME to MCOR
2. VME backplane termination
3. VME backplane power

XILINX Pin Requirements		
Name		Quant
VME Data		32
VME Address		16
VME Control	IRQ	7
	Interrupt	3
	Address Mod	6
	Control	9
MCOR Daughter Board	5 Each	40
Other Functions	???????	0
	Total	113

XILINX PQ160 has 129 MAX user IO
XILINX PQ208 has 160 MAX user IO in smaller footprint.

MCOR30 Daughter Card

1. Serial Interface
    a. 1MHz Serial Clock Rate
    b. Receive Cmd and Data from FRANKEN Board
    c. Transmit Data to FRANKEN Board

2. RS232 Interface
    a. 115.2Kb ASCII HEX interface
    b. All Commands start with CB0X, followed by command and data in HEX

3. Control Logic
    a. Continuously update local copies of ADC values
    b. 20Mhz System Clock Rate
    c. Control MUX

All of the devices on the MCOR Daughter board are memory mapped into VME A16 address space, D32 data space.

Opps: In order to implement block transfers, the interface was redefined as A24D32, however, the upper 8 bits of the address are not used. This could cause a problem.

FrankenBoard Command

RS232		VME			
CMD	ADDR	A[9:0]	Name	DIR	Data[31..00]
0	0-F				Reserved
1	0-7	000-01C	I1MUX	Read	CANDI IMUX1[7:0] From Local RAM
2	0-7	020-03C	I2MUX	Read	CANDI IMUX2[7:0] From Local RAM
3	0-7	040-05C	VMONMUX	Read	CANDI VMONMUX[7:0] From Local RAM
4	0-7	060-07C	RCSR	Read	CANDI CSR[7:0] From Local RAM
5	0-7	080-09C	RSP	Read	CANDI Set Point DAC[7:0] From Local RAM
6	0-7	0A0-0BC	RCAL	Read	CANDI Cal DAC[7:0] From Local RAM
7	0-7	0C0-0DC	RESET	CMD	CANDI Reset Status Latch[7:0]
8	0-7	0E0-0FC	WCSR	Write	CANDI CSR[7:0]
9	0-7	100-11C	WSP	Write	CANDI Set Point DAC[7:0]
A	0-7	120-13C	WCAL	Write	CANDI Calibration DAC[7:0]
B	0-7	140-15C	REFRESH	Write	Send Read Command to CANDI to refresh Local RAM CANDI command is 4 LSBs
C	0-7	160-17C	WFBCSR	Write	FrankenBoard CSR[7:0] (Currently VME only write)
D	0-7	180-19C	RFBCSR	Read	FrankenBoard CSR[7:0]
E	0-F	1A0-1CC	FBMON	Read	FrankenBoard Voltages[15:0]
F	0	1D0	VMESYNC	Write	

bb is the Base Address of the Franken Board determined at XILINX compile time.

CSR0 -- Franken Board Link Status
(Write = 160, Read = 180)

Bits	Name	Dir	Definition
[32..24]	Version	Read	FirmWare Version
[23..16]	Unused	---	Unused
[15..08]	Perror	Read	Link Parity Error
[07..00]	TimeOut	Read	Link Timeout Bits

CSR1 -- Internal Sync Timer
(Write = 164, Read = 184)

Bits	Name	Dir	Definition
[31..24]	Unused	R	
[23..00]	INT_SYNC	R/W	Internal Sync Pulse delay

CSR2 -- System Sync word Low
(Read = 188)

Bits	Name	Dir	Definition
[31..00]	SyncLow	R	Low 32 bits of System Sync

CSR3 -- System Sync word High
(Read = 18C)

Bits	Name	Dir	Definition
[31..00]	SyncHigh	R	High 32 bits of System Sync.

CSR4 -- Aux Card Interface and Operation mode Bits
(Write = 170, Read = 190)

Bits	Name	Dir	Definition
[26..11]	DATA_MODE	R/W	"00" => DACSAM Mode "01" => VME Mode "10" => Sum Mode
[10..09]	SYNC_MODE	R/W	"00" => CPU SYNC "01" => External SYNC "10" => Internal SYNC
08	EXT_Reset	R	Reset Bit from AUX Board Switch
07	GFAULT	R	Ground Fault Status
06	EXT_MODE	R	Mode Bit from AUX Board Switch
[05..00]	ID	R	ID from AUX Board Switch

CSR5 -- Daughter Card Interface and Reset (Set/Reset Register)
(Write = 174, Read = 194)

Bits	Name	Dir	Definition
[31..20]	Unused		
19	DBRESET_RESET	W	ReSet RESET on CANDI
18	INH_RESET	W	ReSet INH on CANDI
17	XBOOT_RESET	W	ReSet XBoot on CANDI
16	INTLK_RESET	W	ReSet INTLK Crate output
[15..07]	Unused		
06	ADCCAL	R W	Calibration in progress Start ADC Calibration (4ms)
05	CHIPRESET	W	Reset Internal registers
04	SYSRESET	R/W	Set VME SYSReset
03	DBRESET_SET	R/W	Set RESET on CANDI
02	INH_SET	R/W	Set INH on CANDI
01	XBOOT_SET	R/W	Set XBoot on CANDI
00	INTLK_SET	R/W	Set INTLK Crate output

CSR6 -- Internal Sync Counter ReadBack
(Read = 198)

Bits	Name	Dir	Definition
[31..24]	Unused	R	
[23..00]	INT_COUNT	R	Internal Sync Count

Calibration DAC Format (MAX 542)

DAC Latch Contents	Analog Output, Vout
1111 1111 1111 1111	+VREF * (32,767 / 32,768)
1000 0000 0000 0001	+VREF * (1/32,768)
1000 0000 0000 0000	0V
0111 1111 1111 1111	-VREF * (1 / 32,768)
0000 0000 0000 0000	-VREF

SetPoint DAC Format (PCM1704)

Binary 2's Complement Input Data (HEX)	DAC Output
7FFFFF	+ Full Scale
000000	Bipolar Zero
FFFFFF	Bipolar Zero - 1 LSB
800000	-Full Scale

Serial Interface Operation:

The Serial Interface between the Franken Board (FB) and the CANDI board is a 2Mhz bit serial interface. 36 bit messages are transfered constantly between the two boards at a 4KHz rate. When Data is written into the FB via the VME interface, the data is sent to the CANDI. Upon receipt of the Set Point Command, the CANDI will send back four 36 bit messages. Read operations from the VME registers return the most recent value received from the CANDI.

The four messages returned after the Set Point Command are:

1. Status
2. IMon1 ADC (Data as selected by the Multiplexor)
3. IMon2 ADC (Data as selected by the Multiplexor)
4. VMON ADC (Data as selected by the Multiplexor)

Command/Data format

Write Data Bits			
	[00..03]	[04..35]	
S	CMD[00..03]	D[00..31]	P

This data is memory mapped into VME space to be read via VME at any time.

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MCOR30 Daughter Card RS232 Interface Operation:

The RS232 port is provided to perfrom monitoring and diagnostic functions. The RS223 port runs at a fixed rate of 115.2Kbd, Even Parity, 8 Data bits, 1 Stop bit (115.2K, E, 8, 1). In order to minimize the possibility of noise generating a command, the following format for the data is used:

CB0Xcddddddddd

where:

RS232 Commad Format	
FB0X	Header FB for the CANDI Board
c	8 bit command in HEX ASCII
dddddddd	32 bit data in HEX ASCII
CRLF	Cr LF

Commands:

The commands are the same whether they come from the Frankenboard Serial interface or over RS232.

CMD[03..00]	Name	Direction	Data[31..00]
0			Reserved
1	IMUX1	Read	IMUX1 Data as selected in CSR I1MUX
2	IMUX2	Read	IMUX2 Data as selected in CSR I2MUX
3	VMONMUX	Read	VMONMUX Data as selected in CSR MONMUX
4	RCSR	Read	CSR
5	RSP	Read	Read Set Point DAC Register
6	RCAL	Read	Read Calibration DAC Register
7	RESET	CMD	Reset Status Latch
8	WCSR	Write	CSR
9	WSP	Write	Set Point DAC
10	WCAL	Write	Calibration DAC
[16..11]			Reserved

Format of the CANDI Control and Status Register (CSR)

Data	Name	Function	Default
[31..29]	Zero	Returns "0000" from CANDI	"0000"
[28..21]	Version	8 Bit CANDI version number	
[20]	RESET	1 => Reset asserted on the Backplane	
[19]	FAULT	1 => MCOR Protection Fault	
[18]	BULKON	1 => BULK Supply ON (Over 10V)	
[17]	INHB	1 => Inhibit asserted on the Backplane	
[16]	PGMBRD	1 => MCOR Programming Module is missing	
[15]	OCFILT	1 => MCOR Filter Current excessive	
[14]	OTSINK	1 => MCOR Heat Sink temperature is excessive	
[13]	OCOUT	1 => MCOR Output Current is excessive	
[12]	BALOUT	1 => MCOR Output Connections do not share similar current levels	
[11]	OVSUPP	1 => MCOR Supply Bus is excessive	
[10..07]	Unused	R/W	
[06]	SYNC	0 => Async Mode; Set Point is transfered to the DAC as it is received from the FrankenBoard 1 => Sync Mode; Set Point is transfered to the DAC after receiving SYNC input from Backplane	0
[05..04]	VMONMUX	00 => VMON1 01 => VMON2 10 => CAL DAC 11 => VMON1 - VMON2	"00"
[03..02]	I2MUX	00 => IMON2 01 => CAL DAC 10 => GND 11 => SET POINT DAC	"00"
[01..00]	I1MUX	00 => IMON1 01 => CAL DAC 10 => GND 11 => TEMP (Relative Measurement)	"00"

Format of the FrankenBoard Control and Status Register (CSR0)

Data	Name	Function
[31..29]	Zero	Returns "0000" from FB
[28..21]	Version	8 Bit FB version number
[20.18]	Unused	
[16]	RESET	Reset asserted on the Backplane
[15]	FAULT	OR MCOR Protection Fault
	BULKON	OR MCOR BULK ON
[17]	INHB	INHB asserted on Backplane
[14]	PGMBRD	OR MCOR Programming Module is missing
[13]	OCFILT	OR of MCOR Filter Current excessive
[12]	OTSINK	OR of MCOR Heat Sink temperature is excessive
[11]	OCOUT	OR of MCOR Output Current is excessive
[10]	BALOUT	OR of MCOR Output Connections do not share similar current levels
[09]	OVSUPP	OR of MCOR Supply Bus is excessive
[08]	UNUSED	
[07..06]	UPDTMD	00 => Set Point DAC updated immediately 01 => All Set Point DAC's VME UPDT register is written to 10 => All Set Point DAC's updated when an external UPDATE signal is received on the backplane
[05..00]		

FrankenBoard Command

CMD[3:0]	Add[3:0]	VME[7:0]	Name	Direction	Data[31..00]
0000 0000	0000 1111				Reserved
0001 0001	0000 0111	00000000 00000111	IMUX1	Read	CANDI IMUX1[7:0] From Local RAM
0010 0010	0000 0111	00001000 00001111	IMUX2	Read	CANDI IMUX2[7:0] From Local RAM
0011	0000 0111	00010000 00010111	VMONMUX	Read	CANDI VMONMUX[7:0] From Local RAM
0100 0100	0000 0111	00011000 00011111	RCSR	Read	CANDI CSR[7:0] From Local RAM
0101 0101	0000 0111	00100000 00100111	RSP	Read	CANDI Set Point DAC[7:0] From Local RAM
0110 0110	0000 0111	00101000 00101111	RCAL	Read	CANDI Cal DAC[7:0] From Local RAM
0111 0111	0000 0111	00110000 00110111	RESET	CMD	CANDI Reset Status Latch[7:0]
1000 1000	0000 0111	00111000 00111111	WCSR	Write	CANDI CSR[7:0]
1001 1001	0000 0111	01000000 01000111	WSP	Write	CANDI Set Point DAC[7:0]
1010 1010	0000 0111	01001000 01001111	WCAL	Write	CANDI Calibration DAC[7:0]
1011 1011	0000 0111	01010000 01010111	CMD	Write	Send Read Command to CANDI to refresh Local RAM CANDI command is 4 LSBs
1100	0000				Reserved

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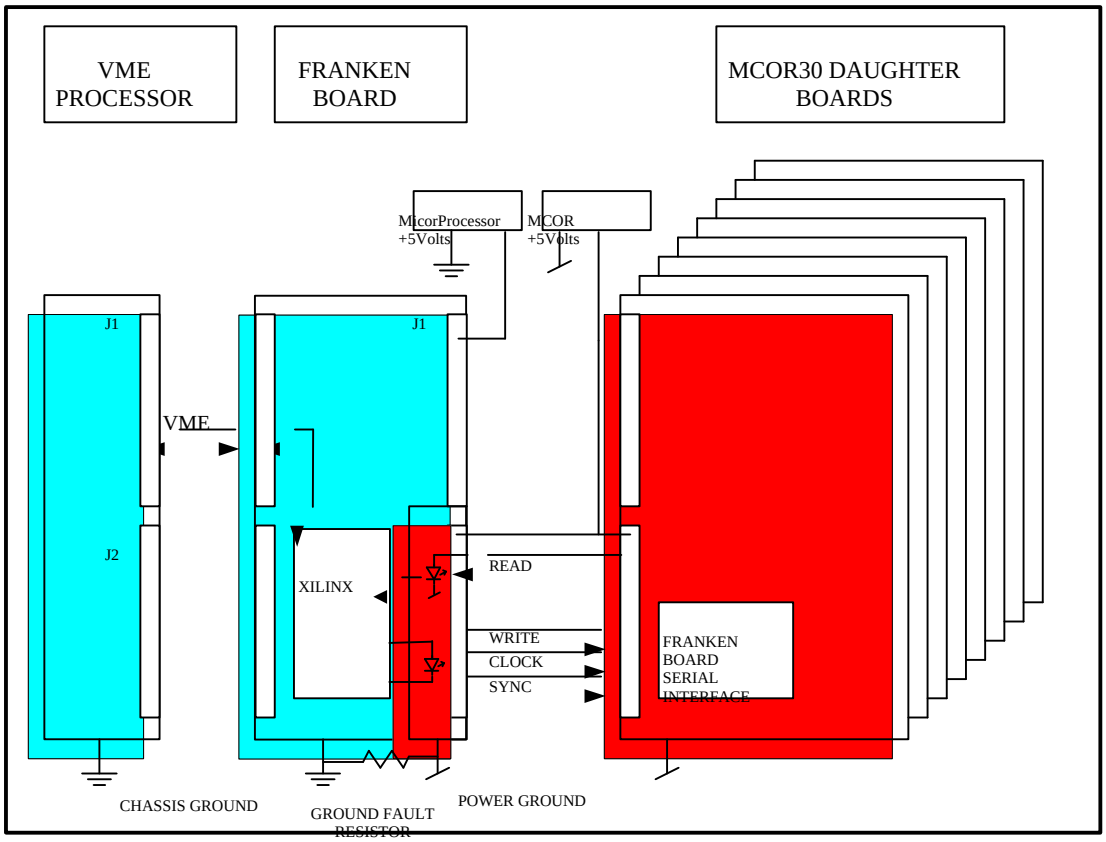
Power Distribution



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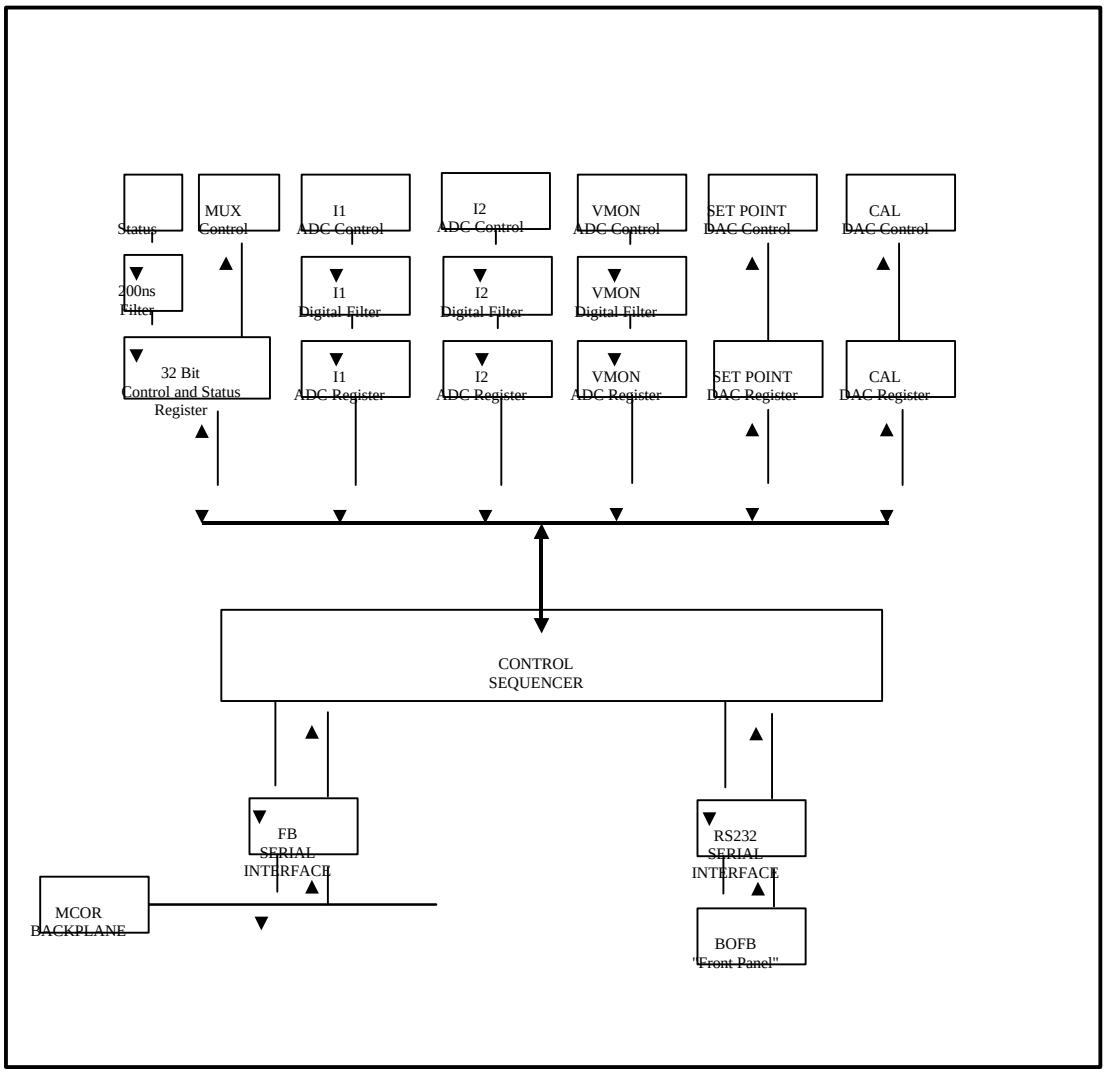
MCOR Daughter Board (CANDI) XILINX Block Diagram



PRELIMINARY

Franken Board Operation:

The Franken Board has several configurations:

1). Crate Local Mode - Controlled by the external MODE pin. When this input is pulled low, the Franken Board will configure all of the MCOR30 Daughter Cards to the default configuration. The 8 analog inputs are digitized at 4khz and sent to the Daughter Cards. A SYNC pulse is generated by an internal 4Khz clock to update all MCOR30 Daughter Cards synchronously. This operation takes place whether there is a CPU connected or not. If a CPU is connected, it can only read from the Franken Board. Writes to the Franken Board will be ignored.

2). CPU Local/Remote Mode - Controlled by the external MODE pin. When this input is left open or pulled high, the CPU has control over which channels use the analog input data (Local) and which use the Eithernet Feedback data (Remote). The Local/Remote operation of each channel is controlled by a bit in the Franken Board CSR.

3). Ethernet Update Mode - In this mode, Daughter Cards configured for CPU Remote will receive Feedback Set Point data at a rate determined by Ethernet packet timing. Daughter Cards that are configured as CPU Local will receive the digitized analog input at the 4Khz rate. The Daughter Card will either update the Set Point DAC immediately, or wait for a Sync generated by the CPU depending on the Daughter Card's Local Sync Mode bit.

4) External Sync Mode - In this mode, an external SYNC input controls the updating of the Set Point DAC's. The external SYNC sets the EXTSYNC bit in the Franken Board CSR and issues a SYNC to the Daughter Cards on the Backplane. If enabled in the Franken Board CSR, a VME interrupt will be generated. Feedback data for Daughter Cards configured as CPU Remote must have been written prior to the SYNC pulse. Daughter Cards that are configured as CPU Local will receive the digitized analog input at the 4Khz rate. The Daughter Card will either update the Set Point DAC immediately, or wait for the SYNC generated by the external SYNC signal depending on the Daughter Card's Local Sync Mode bit. The EXTSYNC bit is cleared by writing to the CSR.

5) Internal Sync Mode - Same as the External Sync Mode except that in this mode, the internal 4Khz is used to generate the synchronization.

03/13/2002

Change SLINK to 2Mbit
MCOR30DB Power UP
Set SP DAC to 0
Set Inhibit
Comparator and ADC on Bulk

Comparator and ADC? on +5V, +-15V

Decouple SP Write and Status return. Return status on sync in sync mode, after SP Write in non-sync mode

LED to indicate Interlock status on AUX card

SYNC to a 8Byte RS232 like structure containing the SYNC count

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Concerns as of July 02, 2001

1. VME Processor Power
    a. Where does it come from?
    b. How does it get to Processor? (CAMAC DAC/SAM 36 Pin AMP on backplane?)
    c. How much power?

2. Franken Board and Daughter Card Power
    a. Current design is ~200-300ma for each board. Mostly XILINX
    b. 1.8-2.7A total needed
    c. 3.0 AMP Max available

3. Daughter Card Space
    a. Fairly crowed with current design
    b. Priority must be given to a very clean Analog layout
    c. Remove some design features if necessary.
        i. Remove one of the 3 ADC channels and mux I1 and I2 into 1 ADC.
        ii. Use 5V only XILINX and remove JTAGablity saving DC-DC converter and JTAG connector.
        iii. Remove RS232 interface saving components and connector

PRELIMINARY

09/05/02
After discussing the operation on the FrankenBoard with Till, a couple of changes have been recommended.

The CANDI's will always be updated with the SYNC pulse, whether it is generated Externally, Internally, or via VME.

Set Point DAC values and CAL DAC values will be sent to the CANDI immediately, but will not update the DAC until the CANDI receives a SYNC. Upon receiving the SYNC, the CANDI will return 6 items: IMON1, IMON2, VMON, RCSR, RSP, RCAL. The FrankenBoard Memory will be double-buffered. The buffer pointer will switch with sync so that new data is written into the Write Memory, and the previous data is available to be read via VME.

Generate a VME Interrupt on SYNC. At this point, the VME processor can download new set points and read previous status information.

Use A24, Supervisory address modifier codes: 3D and 3F. Again note that the upper 8 bits of the address are NOT decoded.

Read back of the internal SYNC counter.