Controller Analog / Digital Interface Manual

Evgeny Medvedko

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1.0 Introduction.

The corrector magnets for the SPEAR-3 synchrotron radiation source require precision, high-speed control for use with the beam-based orbit feedback. A new Multi-Channel Corrector Magnet Controller, a bipolar ±30 A supply (MCOR30), and a new Controller Analog/Digital Interface card (CANDI) have been developed for these purposes. The CANDI card plugs into the MCOR module as it is shown on Figure 1. The CANDI has a 24-bit DAC for current control and three 24-bit Δ-Σ ADCs to monitor the current and the voltages. The ADCs can be read and the DAC updated at the 4 kHz rate needed for feedback control. A precision 16-bit DAC provides on-board calibration. Programmable multiplexers control internal signal routing for calibration, testing, and measurement. Feedback can be closed internally on current setpoint, externally on supply current, or beam position. Noise is better than 17 effective bits in a 10 mHz to 2 kHz bandwidth. Linearity and temperature stability are excellent.

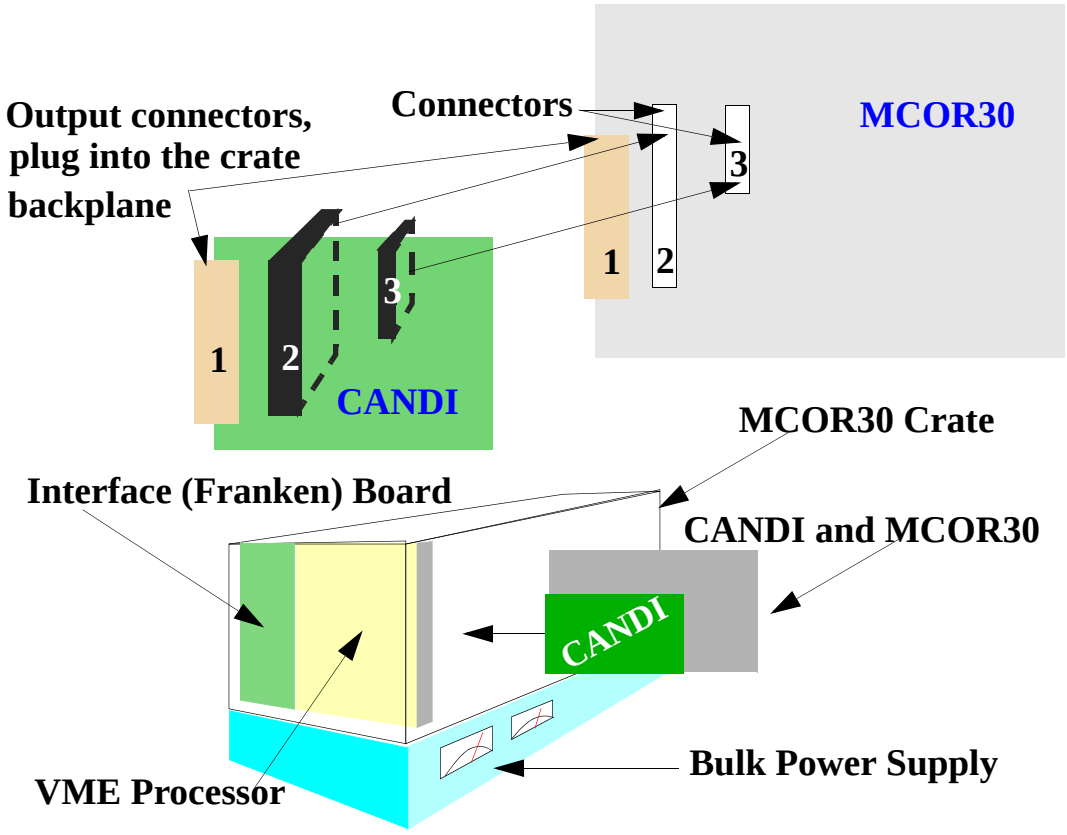

FIGURE 1. CANDI card and MCOR30 module general setup.

Each magnet for orbit correction at SPEAR 3 will have one MCOR supply with the CANDI daughter board. One unit occupies two slots in a 17-slot crate. One crate can support 8 MCORs. The CANDI board controls and monitors the supply's current and voltage, exchanges data with the interface board and the standard VME processor via

the crate backplane. The processor plugs into the interface board, which adapts the VME processor to the MCOR crate.

2.0 MCOR30 Overview.

The MCOR30 supplies 0 to +/- 30 A current to the load. The MCOR30 diagram is shown on Figure 2 below. The CANDI setpoint signal goes to the summing amplifier (SA) on the MCOR30 board. The another SA input is the signal from the current sensing shunt. The SA output drives the pulse-width modulation (PWM) controller. The PWM signal (40 kHz - 60 kHz) controls the H - Bridge Driver. The H-Bridge has four MOSFET transistors. The pair of diagonally located transistors could be closed at one time, the current through the load is reversible.

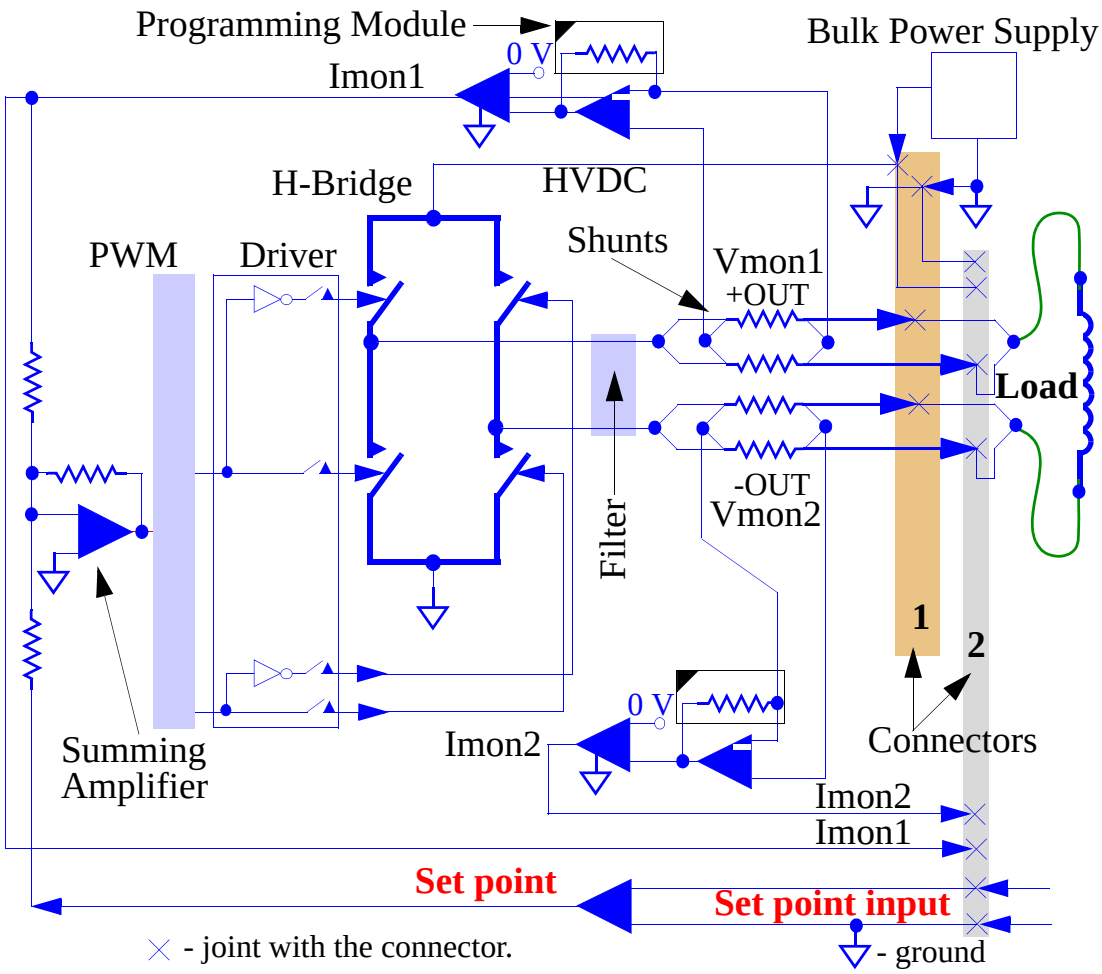

FIGURE 2. MCOR30 block diagram.

To smooth the ripples, the pulsed signal from the H-Bridge go to the filter, then the signal splits in two streams 15 A each and go through the shunts to the MCOR30 outputs +Out and -Out. The signal from connector 1 goes to the crate backplane, the

signal from connector 2 goes to the CANDI board. The CANDI's 15 A output combine with the 15 A MCOR30 output on the crate backplane to make the load current 30 A.

The shunt's impedance is 0.01 Ω. Two shunts are connected together through the resistive dividers (not shown on the Fig. 2). The voltage across the shunts applies to the amplifier with the scaling resistor in the feedback loop, to make 10 V output voltage at 30 A current (the resistor is located on the programming module - MCOR's daughter board). The floating output voltage goes to the differential amplifier with one of the inputs connected to the floating 0 V. The output signal is referred to the local ground. The signal from the +Out shunt is used for the local feedback and for the current monitoring (Imon1), the signal from the -Out shunt is the second current monitor source (Imon2). Imon1, Imon2 and Vmon1, Vmon2 (the voltage across the load) go to connector 2 to the CANDI card.

The MCOR30 generates the fault indicating signals, they go to the CANDI card via connector 3.

The bulk power supply output is connected to the crate backplane then to connectors 1 and 2. The high voltage DC (HVDC) input goes up to +70 V.

The MCOR30 predecessor description (MCOR12) could be found in: G.E. Leyh, et. al. "A Multi-Channel Corrector Magnet Controller," PAC 95 and IUPAP, Dallas, Texas, 1-5 May 1995.

3.0 The CANDI Board Description.

The CANDI's input signal (Fig. 3) goes to the instrumentation amplifier through the multiplexer (MUX), then to the operational amplifier, scaling the signal to the input range of the following ADC. All three input channels are identical, except Vmon inputs, having the resistive voltage divider at the input to scale the 70 V signal to 6.9 V. The scaling amplifiers and the ADC1, 2 and 3 share the same reference voltage 2.5 V.

The setpoint output signal (*Vsp*) goes to the MCOR30 input though connector 2 to control the supply's current and to the "Imon2" MUX for the local feedback purposes. The *Vsp* range is +/- 10.2 V.

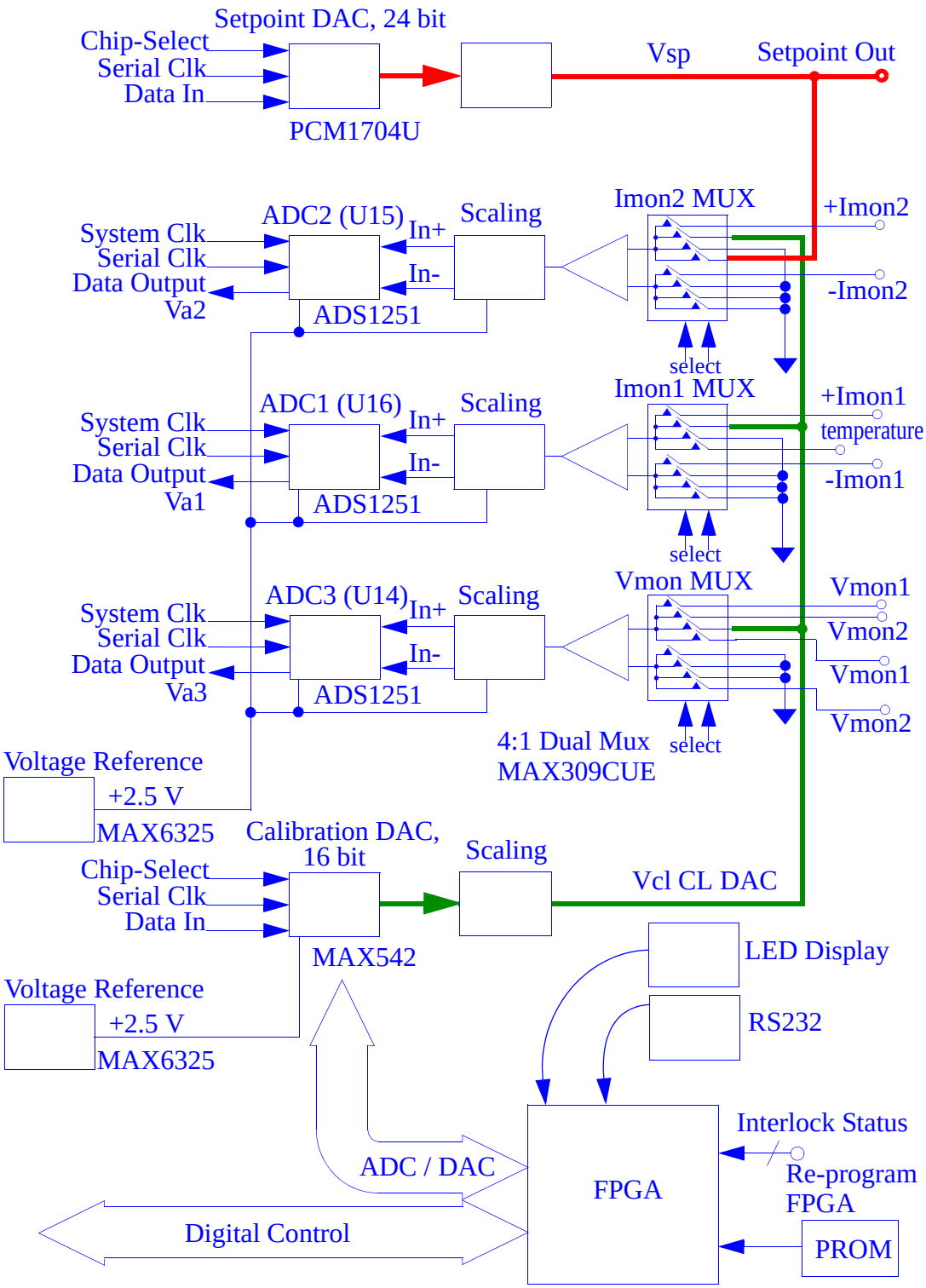

FIGURE 3. CANDI card block diagram.

The scaled Calibration DAC (CL DAC) output signal splits to three multiplexers. By closing the local feedback loop ADC 1,2,3 - CL DAC, and ADC2 - SP DAC, all ADCs and DACs can be calibrated against the CL DAC, or SP DAC, or the external signal.

There is a temperature sensor on the board, it can be read from the ADC1.

The FPGA (Field Programmable Gate Array) executes the processor's commands, reads status, writes and reads three ADCs and two DACs. The FPGA's boot PROM can be re-programmed through the connector, located at the front of the board. The FPGA send the signals indicating the value of the supply's current and the faults status to the 4-digit LED display, also located at the front of the board, next to the RS232 input connector.

The CANDI board size is 6.5" x 3.95", about 0.062" thick (Fig. 4). A shielding box covers the analog signal processing area.

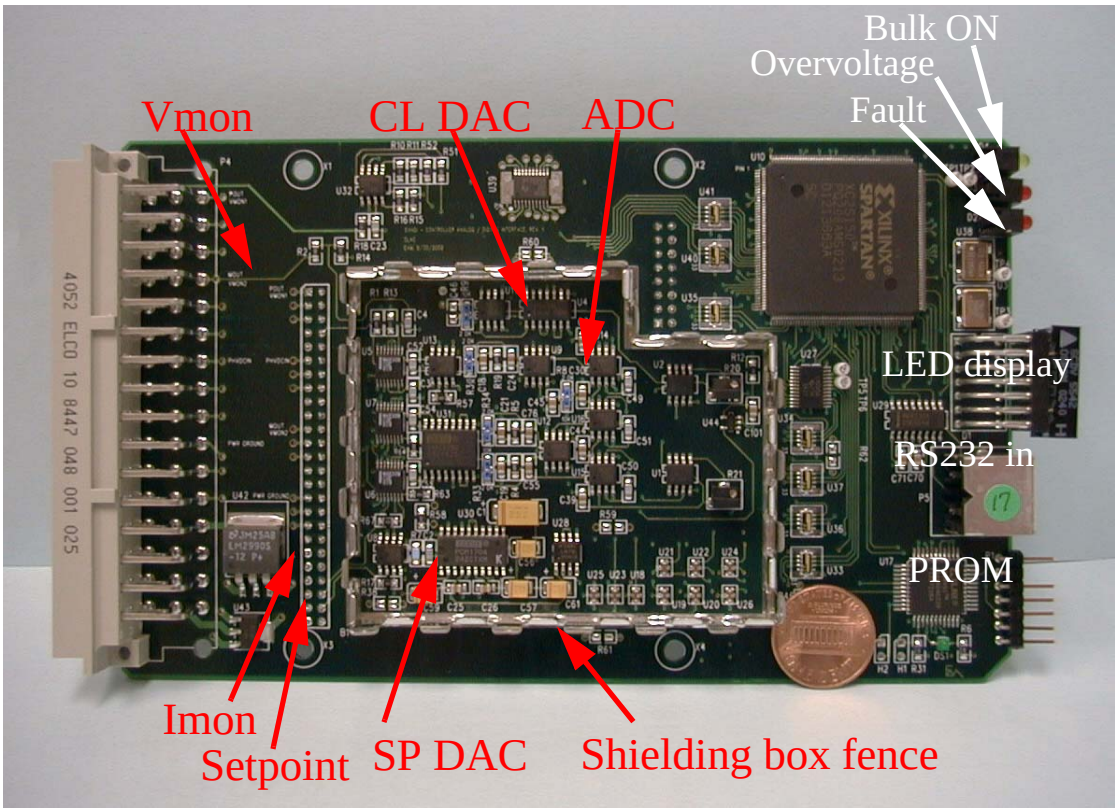

FIGURE 4. The CANDI card, top view.

Three LEDs show the Bulk supply ON / OFF status (yellow), the overvoltage status (red) and the fault detection (red).

4.0 The Input Channel.

4.1 The input signal processing chain.

The Imon1 and Imon2 signals go through connector 2 to the MUX1 and MUX2 (MAX309CUE, Maxim) inputs (Fig. 5). The source output impedance is 470 Ω, the MUX "on" resistor is 60 Ω. The resistors drift in temperature and behave as a voltage divider. In order to make these effects insignificant, the buffering instrumentation amplifier with a high 10^{10} Ω input impedance was chosen for the design (INA128U*). The operational amplifier (OPA227U*) scales and filters the signal which goes then to the ADC input (ADS1251U*).

* Burr-Brown for TI.

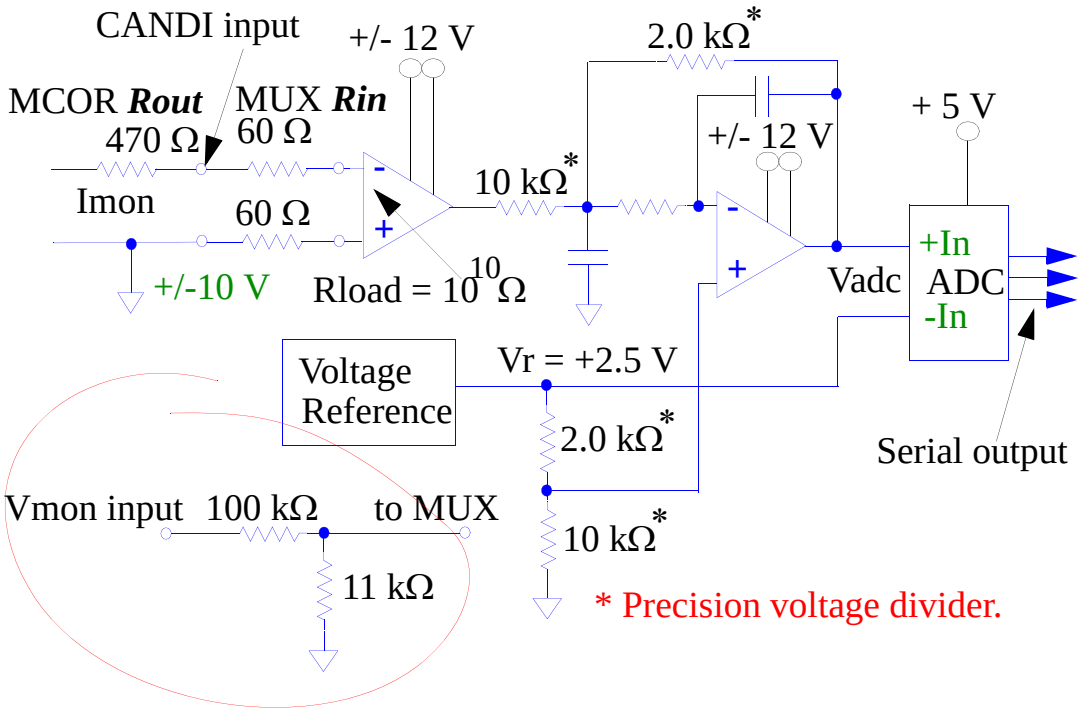

FIGURE 5. The sketch of the input signal processing channel.

The ADC input range is 0 to 5 V +/- 0.3 V. The input is sensitive to overvoltage. The MCOR30 maximum current could be above 30 A. The relation *Vadc(Imon)* is:

•*Vadc(Imon) = Imon*0.2 + Vr*, where *Vr* = 2.5 V.

At Imon = +12.0 V (36 A), the Vadc = + 4.9 V (Tab. 1). To prevent ADC damage at Imon > 12 V, DC voltage regulators are used to supply +/- 12 V power to the instrumentation and the operational amplifiers in order to limit their output voltage swing to the DC supply range. The +/- 12.5 V Imon signal corresponds to the +5 V to 0 V ADC full scale range (*FSR*). Therefore, the CANDI input full scale range (FSR) is 25 V.

The Vmon input could go up to + 70 V, the voltage dividers with the gain 0.099 are installed at the Vmon1 and 2 inputs.

TABLE 1. ADC input versus the Imon (CANDI input).

Imon, V	Vadc, V
+12	+ 4.9
+10	+4.5
0	+2.5
-10	+0.5
-12	+0.1

The FPGA reads the ADC at 4 kHz data rate frequency (*Fdr*).

4.2 ADS1251 characteristics.

The ADS1251 has 24-bit resolution, Δ-Σ architecture, single +5 V supply, maximum *Fdr* = 20.833 MHz, serial interface.

The ADC has an internal digital filter (Fig. 6). The filter averages the Δ-Σ modulator results and present them as a digital output.

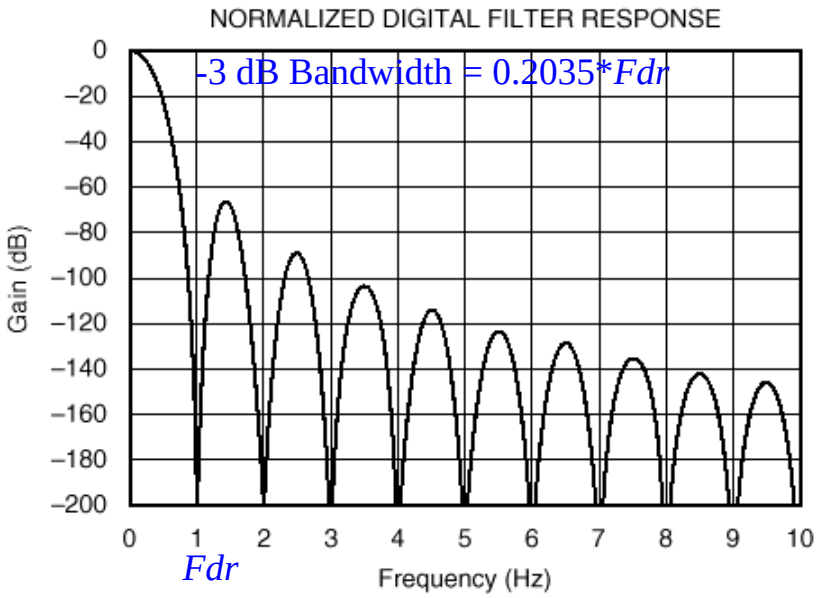

FIGURE 6. The ADS1251 internal digital filter normalized response. Frequency = 1 corresponds to *Fdr*.

FSR signal change at the ADC input requires five or six full conversions to settle.

The nominal system clock frequency is 8 MHz (*Fs*). The Δ-Σ modulator frequency *Fm = Fs / 6*; the modulator oversampling rate is fixed to 64, *Fdr = Fm / 64*. The production CANDI card ADC's *Fdr = 4 kHz*.

The ADS1251 has a very low temperature coefficient (TC). The offset drift TC = 0.07 ppm / °C, the gain drift TC = 0.4 ppm / °C.

TABLE 2. ADC Code, ADC1251U.

Code, hexadecimal	Scale	Analog Input, V
7FFFFF	**+ FS code;** 2^{23} **- 1**	**+ 12.5 - LSB**
1	**mid scale code + 1;**	**0 + LSB**
0	**mid scale code;**	**0**
FFFFFF	**mid scale code - 1;** 2^{24} **- 1**	**0 - LSB**
800000	**- FS code;** 2^{23}	**-12.5**
	least significant bit $FSR/2^n$	$25/2^{24}$

The ADC input voltage (V_{in}) to the digital code (D) relation is:

$$V_{in} = \frac{D \cdot FSR}{2^n}, \qquad \text{(EQ 1)}$$

where *n* - number of bit.

4.3 Precision Voltage Dividers.

The precision 2 kΩ / 10 kΩ resistive voltage dividers have nominal 0.3 ppm / °C ratio tracking and resistance TC = -0.6 ppm / °C. Model VSMD1505, Vishay.

4.4 Voltage reference.

The 2.5 V voltage reference (MAX6325CSA, Maxim) has output range 2.499 V to 2.501 V and TC = 0.5 ppm / °C.

5.0 Setpoint output.

The 24-bit setpoint DAC (SP DAC) has +/- 1.2 mA current output. The current over the 8.35 kΩ precision feedback resistor (Fig. 7) gives +/- 10.2 V at the operational amplifier output. This signal goes to the MCOR30 setpoint input and to the “Imon2” MUX input.

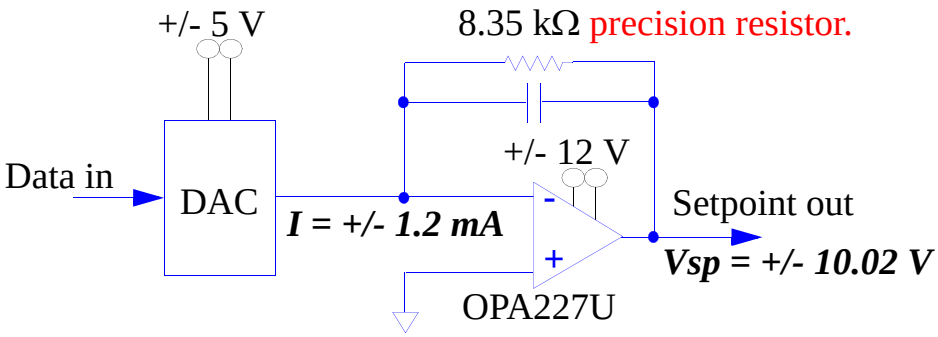

FIGURE 7. The setpoint DAC and the output buffer block diagram.

5.1 SP DAC characteristics.

The PCM1704U-K (Burr-Brown for TI) has 24-bit resolution, sign-magnitude architecture, +/- 5 V supply, 200 ns settling time, serial interface. The offset drift TC = +/-5 ppm / °C, the gain drift TC = +/-25 ppm / °C.

TABLE 3. SP DAC Code. The output +/- 1.2 mA current goes to the 8.5 k resistor to make the output scale +/- 10.2 V.

Code, hexadecimal	Scale	Analog Output, V
7FFFFF	**+ FS code;** 2^{23} **- 1**	**+ 10.02 - LSB**
1	**mid scale code + 1;**	**0 + LSB**
0	**mid scale code;**	**0**
FFFFFF	**mid scale code - 1;** 2^{24} **- 1**	**0 - LSB**
800000	**- FS code;** 2^{23}	**-10.02**
	least significant bit $FSR/2^n$	$20.04/2^{24}$

The SP DAC output voltage (V_{out}) to the digital code relation is the same as the EQ. 1, replace V_{in} with V_{out} in the EQ. 1; SP DAC FSR=20.04 V.

6.0 Calibration Source.

The Calibration DAC (CL DAC) analog output signal goes to the noninverting input of the external operational amplifier (Fig. 8). For the bipolar output swing the CL DAC has the internal matched bipolar offset resistors, connected to the external voltage reference and to the operational amplifier, so the amplifier's output swings for

+/- 2.5 V. The next amplifier with the gain 5 inverts the input signal and supplies the +/- 12 V limited output to the MUX1, 2 and 3 inputs.

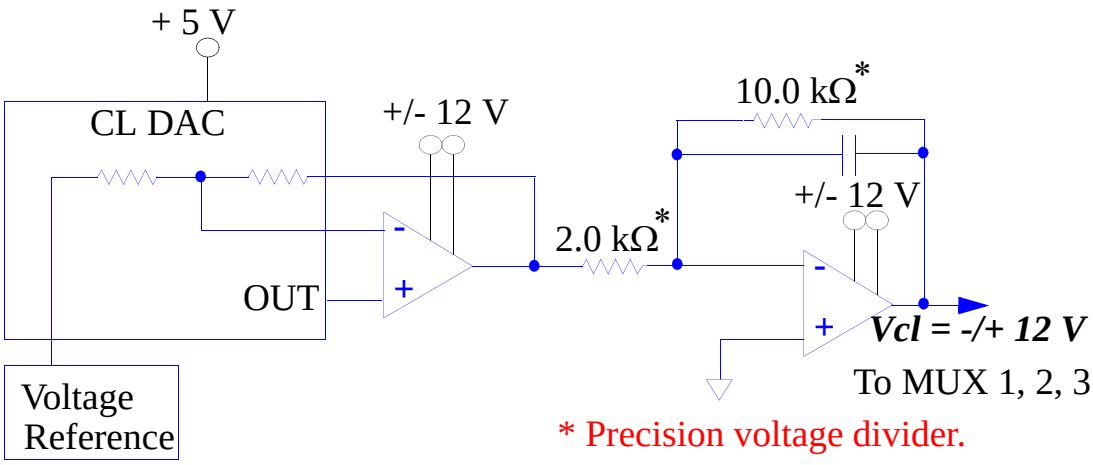

FIGURE 8. Calibration source sketch.

The CL DAC is a precision, low drift independent calibration source.

6.1 CL DAC characteristics.

The CL DAC (MAX542ACSD, Maxim) has 16-bit resolution, single +5 V supply, 1 MHz bandwidth, serial interface. The CL DAC offset drift TC = +/-0.5 ppm / °C, the gain drift TC = +/-0.1 ppm / °C.

TABLE 4. CL DAC and the output amplifier Code Table.

Code, hexadecimal	Scale	Analog Output, V
FFFF	**+ FS code;** 2^{16} **- 1**	**+ 12.5 - LSB**
8001	**mid scale code + 1;** 2^{15} **+ 1**	**0 + LSB**
8000	**mid scale code;** 2^{15}	**0**
7FFF	**mid scale code - 1;** 2^{15} **- 1**	**0 - LSB**
0	**- FS code**	**-12.5**
	least significant bit $FSR/2^n$	$25/2^{16}$

The CL DAC output voltage (V_{out}) to the digital code (D) relation is:

$$- V_{out} = (D - 2^{15})\frac{FSR}{2^n} \qquad \text{(EQ 2)}$$

7.0 Temperature Sensor.

The analog output temperature sensor (MAX6608IUK-T, Maxim) has the output voltage temperature slope of 10 mV / °C and an offset of 500 mV at 0 °C. The typical temperature error is 0.6 °C. The temperature-to-voltage transfer function is:

$$T(°C) = (Vout - 500\ mV) / 10\ mV / °C.$$

8.0 Functionality.

Dual 4-channel differential multiplexers (MUX) are placed in front of the signal processing chain. The different configuration can be made to perform the MCOR30 current controls and the signals monitoring, to make the local, remote, or global feedback.

The multiplexers are normally open. When the inputs 1 to 4 are selected, the corresponding A and B switches are closed. The multiplexers functions and the inputs selection diagram are shown below (Tab. 5 and Tab. 6).

TABLE 5. Multiplexers Functions, AGND - analog ground.

Input Number	Input A Function	Input B Function
Imon1 multiplexer		
1	Imon1 Signal	Imon Ground
2	CL DAC	AGND
3	AGND	AGND
4	Temperature sensor	AGND
Imon2 multiplexer		
1	Imon2 Signal	Imon Ground
2	CL DAC	AGND
3	AGND	AGND
4	SP DAC	AGND
Vmon multiplexer		
1	Vmon1	AGND
2	Vmon2	AGND
3	CL DAC	AGND
4	Vmon1	Vmon2

TABLE 6. Multiplexer Inputs Selection Diagram.

Address 1	Address 0	EN	ON Switch
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

The multiplexer MAX309CUE is TTL-Logic compatible.

9.0 Digital interface.

The digital interfacing, the data accumulation, the commands interpretation and distribution are programmed in the SPARTAN-II (XC2S150PQ208, Xilinx) FPGA. It has two input clocks, 20 MHz for the commands execution and 15.36 MHz to drive the ADC system clock and to get 4 kHz data output rate.

The system clock goes to the ADC digital inputs through the bus transceiver / TTL translator. All digital signals are transmitted via 100 Ω / 100 pF RC networks in order to cut the digital signals sharp edges and to reduce the overall noise.

The RS232 runs with 115.2 Kbd rate.

The FPGA has power (+2.5 V and +3.3 V), supplied by the dual voltage regulator.

The detailed list of the FPGA commands is giving in the “SPEAR3 MCOR30 System.”, written by Jeff Olsen, http://www.slac.stanford.edu/~jjo/sp3mcc/mcor30.pdf.

10.0 Faults Indication.

The MCOR30 generates TTL compatible signals, indicating different faults (Tab. 7). The CANDI board’s FPGA accumulates these signals and sends the fault summary command back to the MCOR30. If faults are detected, this command inhibits the PWM.

TABLE 7. Connector 3, pin numbers, faults signals and faults conditions.

Pin number	Fault	Conditions
1	Current balance out.	When the current from the +Out and the -Out shunts are significantly different.
2	Programming module is missing.	
6	Over current.	When the output current is excessive.
14	Fault summary.	Generated by the FPGA when one or more faults are detected, going to the MCOR30 and inhibits the PWM.
15	Over temperature.	When heat sink temperature is excessive.
16	Filter over current.	Condition from the prolonged excessive load voltage excursion.

In addition to the above mentioned fault signals, the CANDI board has the HVDC monitor to indicate the Bulk Supply status - under voltage, normal operation and overvoltage (fault).

The high voltage bus is wired to the resistive divider, defining the undervoltage and the overvoltage thresholds for the dual comparator. When the Bulk Supply operates in the nominal range +32 V to +65 V, the comparator output indicates the “bulk-on” condition. If the voltage is higher than +65 V, the comparator’s second output indicates the “over voltage” status. Both signals go to the FPGA.

11.0 Terminology and Requirements.

11.1 Terminology.

•ACCURACY - the worst case input to output error of a data converter, as a percent of full scale range (***FSR***).

•RESOLUTION - the smallest change that can be distinguished by an A/D converter or produced by a D/A converter. Usually expressed as the number of bits ***N,*** where the converter has 2^N possible states.

•LEAST SIGNIFICANT BIT (***LSB***) = $\frac{FSR}{2^N}$.

•RMS Quantization Noise in Nyquist Bandwidth, $\sigma = \frac{q}{\sqrt{12}}$, $q = LSB$.

•Effective Number of Bits (***ENOB***) = $log_2\left(\frac{FSR}{\sigma\sqrt{12}}\right)$.

•Signal to noise ratio versus ***ENOB*****:** SNR = 6.02 * ENOB + 1.76, dB.

11.2 Requirements.

•The CANDI card shall read the monitor signals from the MCOR30 and shall supply the reference voltage (setpoint) to the MCOR30.

•Required data update frequency 4 kHz.

•The analog setpoint and the readback requirements are shown below (Tabs. 8, 9).

TABLE 8. The current setpoint requirements.

Analog Setpoint	**Requirements**
Full scale voltage range	+/- 10 V
Bandwidth	DC - 2 kHz
Accuracy	+/- 10 mV
Stability (24 hours, +/- 3.5 °C)	+/- 500 μV
Signal to Noise Ratio, integrated over 10 mHz - 2 kHz	105 dB or 17.2 ENOB

•The temperature coefficient limit is: +/- 14.3 ppm/°C (+/- 500 μV / +/- 3.5 °C, out of 10 V full scale).

TABLE 9. The current and voltage monitors requirements.

Analog Readback, Imon	**Requirements**
Full scale voltage range	+/- 10 V
Bandwidth	DC - 2 kHz
Accuracy	+/- 1 mV
Signal to Noise Ratio integrated over 1 Hz - 200 Hz	101 dB or 16.6 ENOB
Analog Readback, Vmon	
Full scale voltage range	70 V
Accuracy	+/- 10 mV
Signal to Noise Ratio, integrated over 1 Hz - 1 kHz	86 dB or 14 ENOB

12.0 The errors source.

The ADC, DAC, operational and instrumentation amplifiers, resistive voltage dividers have a non-ideal gain and offset, temperature and time drift. The offset moves the transfer function in parallel to the ideal, the gain rotates the transfer function around zero code - all bits off (Fig. 9). This could be critical for the CANDI card accuracy and for the stability in temperature and in time.

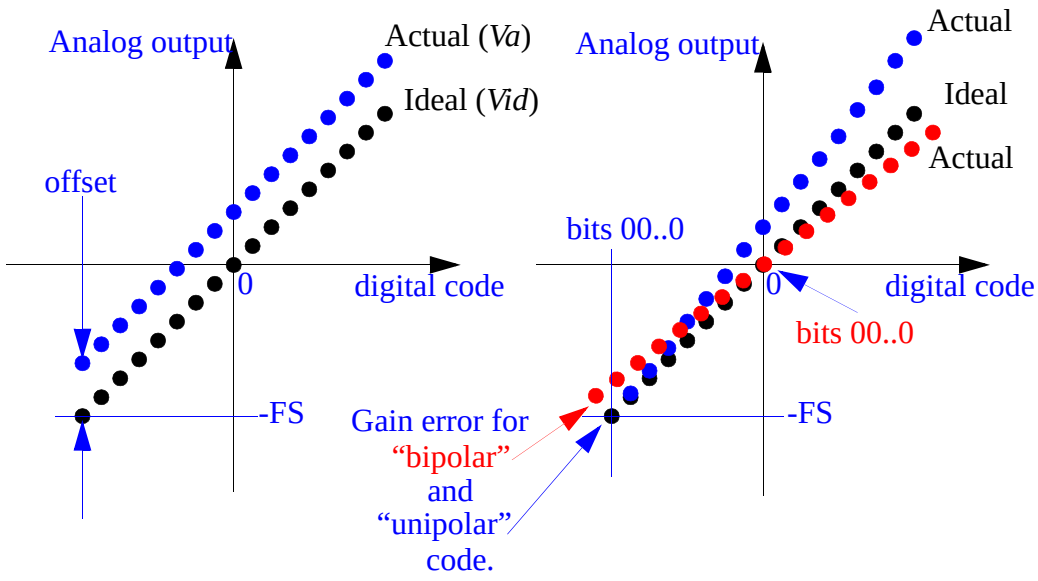

FIGURE 9. The offset error and the unipolar / bipolar gain error.

To reduce the errors, the offset and the gain should be calibrated and compensated.

13.0 CANDI tests results.

13.1 The accuracy measurements and calibration.

The following scheme is used to measure the CANDI card accuracy (Fig. 10).

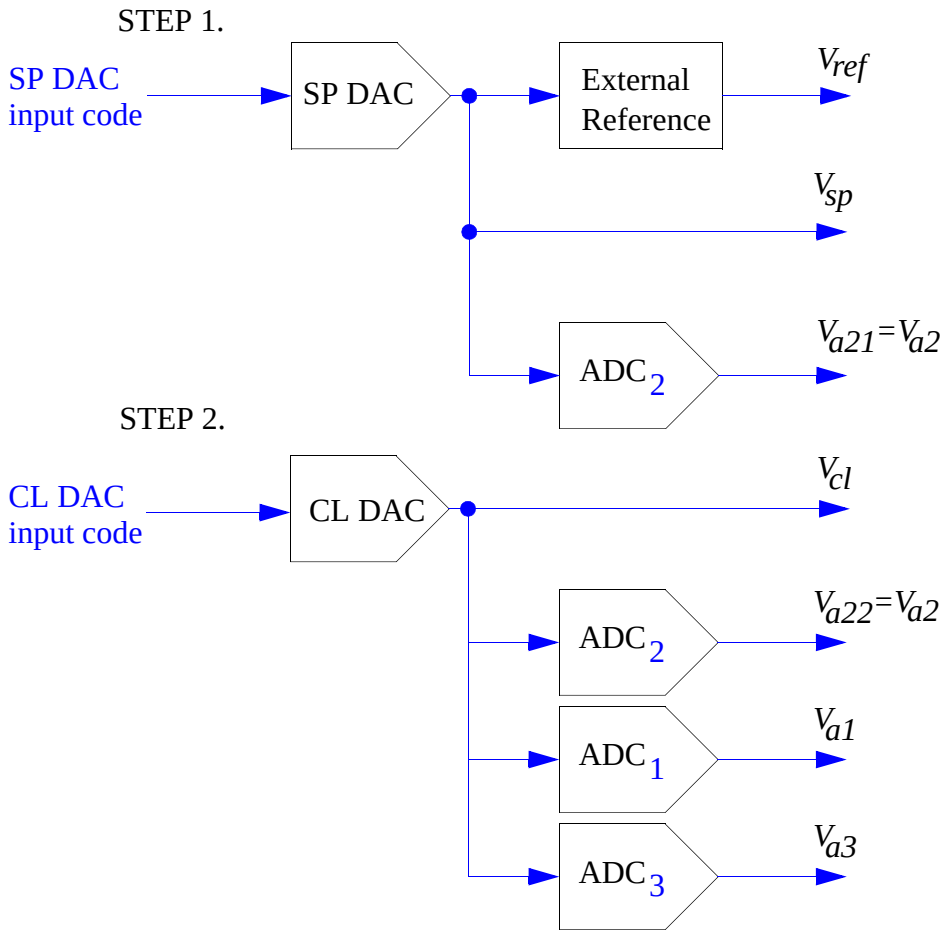

FIGURE 10. Calibration test diagram.

The SP DAC and the CL DAC share the same input code, -10 V to +10 V with 2 V increment. The SP DAC output signal (*Vsp*) goes to the External Reference (*Vref*) and to the ADC2 (*Va21*) via the multiplexer. After reading the ADC2 and the External Reference, the multiplexer connects the ADC2 input to the CL DAC (*Vcl*) output. One cycle of the measurements ends when ADC1 (*Va1*), ADC2 (*Va22*) and ADC3 (*Va3*) are red.

The External Reference is the Agilent 34970A Data Acquisition Switch Unit, at FSR it has +/- 22 µV resolution, 190 µV accuracy over 24 hours, TC = 6 ppm / °C.

The not calibrated SP DAC accuracy *Vref - Vsp; Va21 - Vsp* (Fig. 11) and the CL DAC accuracy *Va1 - Vcl, Va22-Vcl, Va3 - Vcl*:

•-75 mV and -5 mV at +/- FSR respectively (10 mV or less is required);

• -10 mV to + 15 mV at +/- FSR respectively (1 mV or less is required).

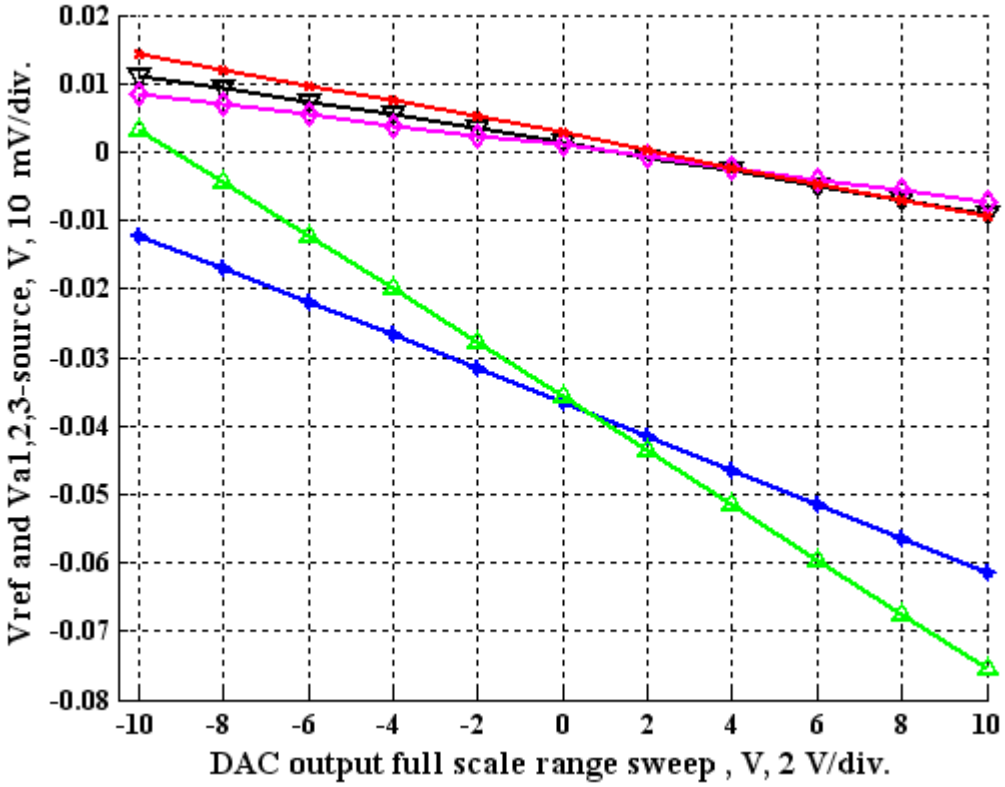

FIGURE 11. SP DAC and CL DAC accuracy, *Vref - Vsp* blue, *Va21 - Vsp* green, *Va1 - Vcl* black, *Va22 - Vcl* magenta, *Va3 - Vcl* red, versus *Vsp*, Volts.

To improve the results, the DACs and ADCs relative gain (m_i) and offset (b_i) should be used in the DACs setting and the ADCs reading.

$$F_1 = V_{ref} \cdot m_1 + b_1 = V_{sp}, \quad \text{(EQ 3)}$$

$$F_2 = V_{a21} \cdot m_2 + b_2 = V_{sp}, \quad \text{(EQ 4)}$$

$$F_3 = V_{a22} \cdot m_3 + b_3 = V_{cl}, \quad \text{(EQ 5)}$$

$$F_4 = V_{a1} \cdot m_4 + b_4 = V_{cl}, \quad \text{(EQ 6)}$$

$$F_5 = V_{a3} \cdot m_5 + b_5 = V_{cl}. \quad \text{(EQ 7)}$$

These functions are shifting and rotating *Vref* and *Vadc* data toward *Vsp* and *Vcl.*

The calibrated SP DAC and CL DAC accuracy is better than required: +/- 300 μV, about 160 μV rms (Fig. 12).

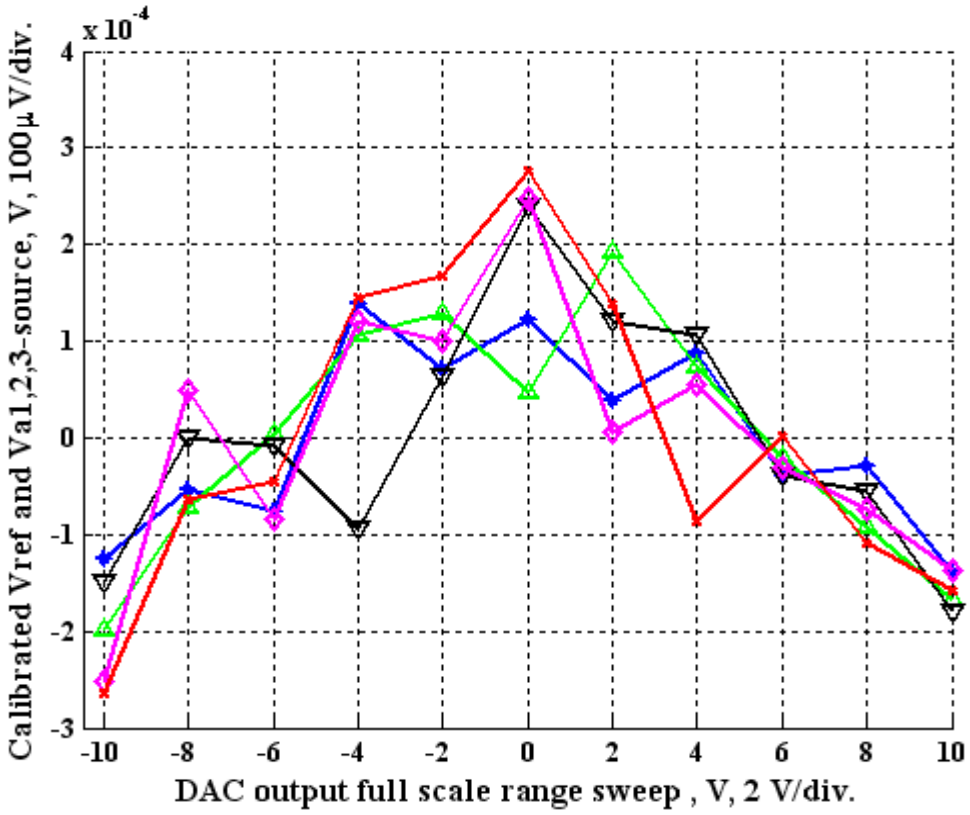

FIGURE 12. . Calibrated SP DAC and CL DAC accuracy, *F1 - Vsp* blue, *F2 - Vsp* green, *F4 - Vcl* black, *F3 - Vcl* magenta, *F5 - Vcl* red, versus *Vsp*, Volts.

The CANDI boards were calibrated and the results were saved to the files “candi_#”, where # - module number:

TABLE 10. The calibration file.

Row Number	Contents
1	*module number*
2	*m1, m2, m3, m4, m5*
3	*b1, b2, b3, b4, b5*
4	*Vrms1, Vrms2, Vrms3, Vrms4, Vrms5*
5	*Vref*
6	*Vsp*
7	*Va21*
8	*Vcl*
9	*Va1*
10	*Va22*
11	*Va3*

The RMS voltage were measured from the following data: *Vrms1*=rms*(F1-Vsp)*, *Vrms2*=rms*(F2-Vsp)*, *Vrms3*=rms*(F3-Vcl)*, *Vrms4*=rms*(F4-Vcl)*, *Vrms5*=rms*(F5-Vcl)*. The rows 3 to 11 are in Volts.

13.2 The noise performance.

The ENOB measurements were performed at 4 kHz data update frequency and 20 kHz ADC readback rate. The SP and CL DAC outputs were set to + full scale. In addition to the ADC 64 oversamplings, the FPGA averages 16 ADC samples. This is equivalent to increasing the ADC oversampling ratio to a factor of 4. The setpoint and the readback ENOB spread is shown below (Tab. 11).

TABLE 11. The set point and the read back ENOB.

Source signal to ADC #	ENOB	
	min	**max**
Setpoint: SP DAC to ADC2	17.3	17.7
Readback: CL DAC to ADC1 & 2	17.5	18.0
Readback: CL DAC to ADC3	17.0	17.9

The production module has no averages, the ADC output rate is 4 kHz, the readback ENOB is reduced by another 1.25 bits.

The SP DAC and ADC noise power spectrum, corresponding to 18 ENOB in the 10 mHz - 2 kHz frequency band, is shown on Figure 13.

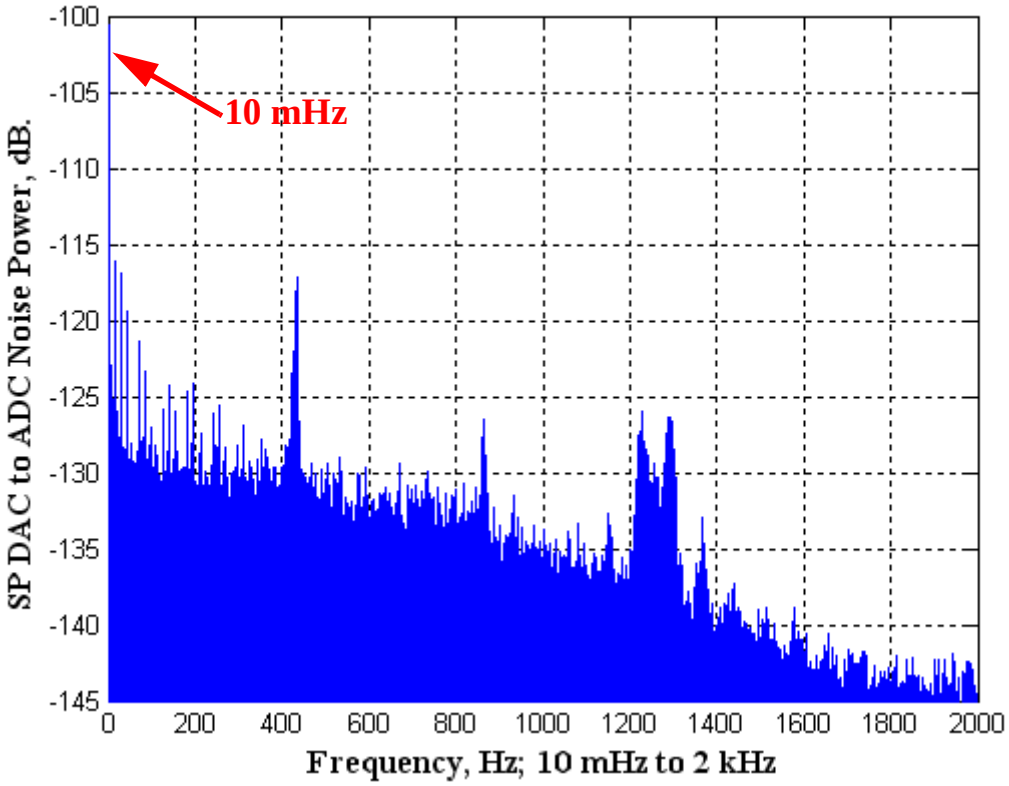

FIGURE 13. SP DAC and ADC noise spectrum.

13.3 Stability measurements.

The SP DAC and the CL DAC + full scale output signals were monitored over two hours. The External Reference and ADC2 were monitored the SP DAC, ADC2 was monitoring the CL DAC. The Figure 14 shows the *Vref* (set point output) varying for about 1.1 mV over a 40 minute interval where ambient temperature drops 2.6 °C. The corresponding temperature coefficient, calculated according the equation:

•TC (ppm / °C) = $\Delta V / \Delta T * 1e6 / 10\ V$,

is 42 ppm / °C at a 10 V full scale. The maximum allowed TC is 14.3 ppm / °C.

The CL DAC output *Va22* shows no significant temperature and time dependency.

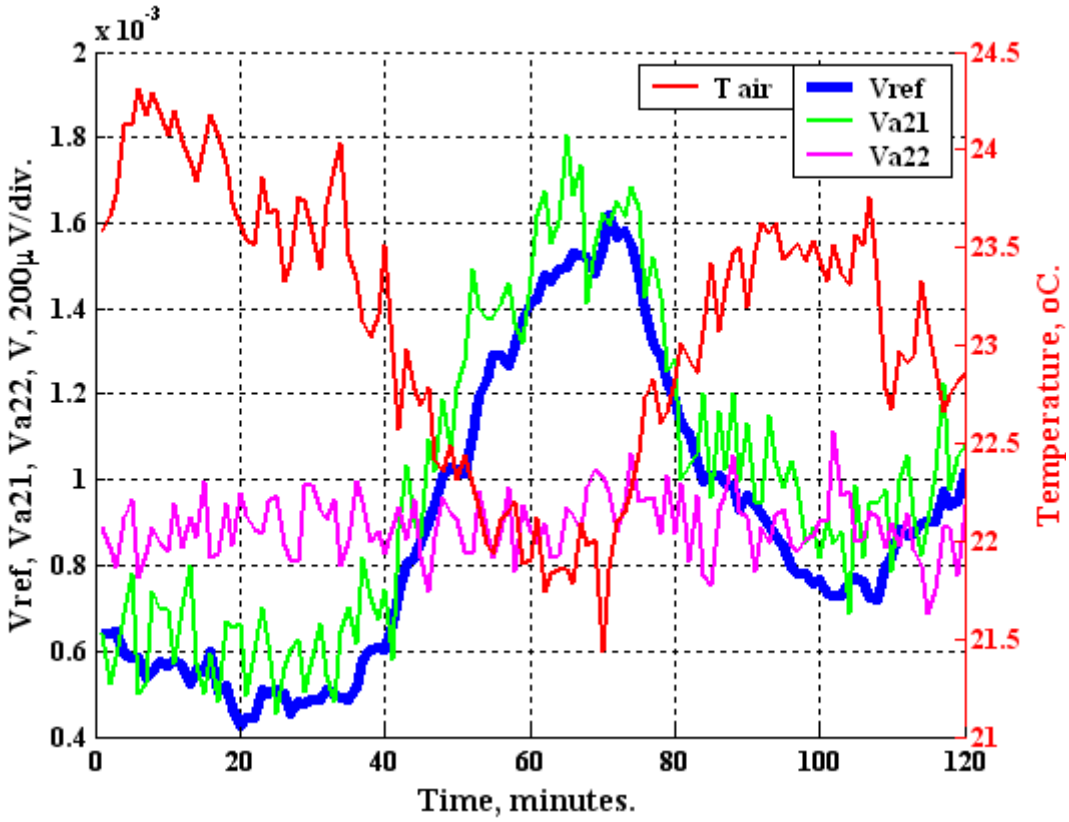

FIGURE 14. SP DAC and CL DAC stability. The signals have removed + full scale DC voltage.

To improve the CANDI module stability results, the successive approximation algorithm feedback is implemented to the test program. The difference of the *Va2* and the SP DAC initial input code, tracks the SP DAC error. The sum of the weighted difference and *Vsp* goes to the SP DAC input. Four loops with the weighting factors 2, 4, 8 and 16 tune the SP DAC precisely to the initial input code (Fig. 15).

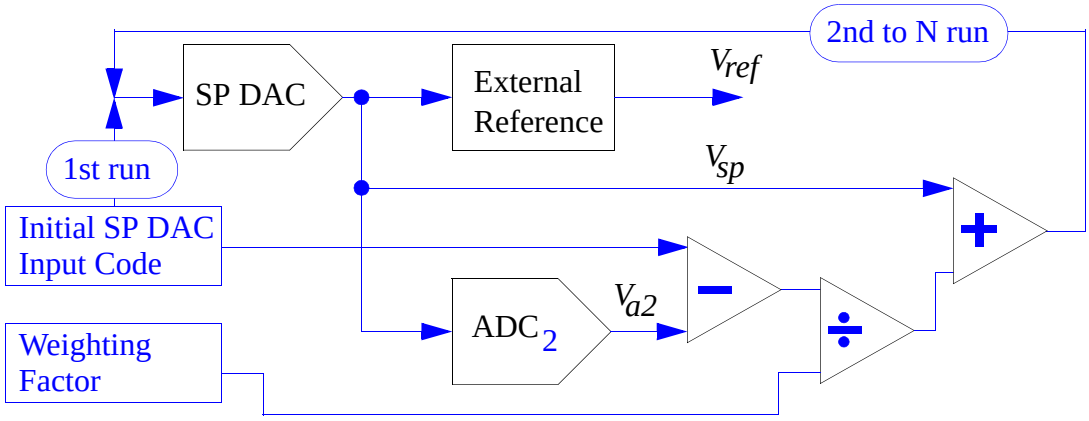

FIGURE 15. The program feedback to tune the SP DAC to the initial input code.

The initial input code was set to + 9 V.

The test program was run for 50 hours. The *Vref*, *Vsp*, *Va21*, air temperature (*Tair*) and the CANDI temperature (*Tc*) were monitored. The *Vref*, *Va21*, *Tc*, and *Tair* are shown on the Figure 16 below.

•The *Vref* variation over 50 hours is about +/- 200 μV.

•The *Va21* variation over 50 hours is about +/- 300 μV.

•Δ*Tair* on the ramp (hours 24 to 36) is about -2.5 °C, Δ*Tc* = -1.8 °C.

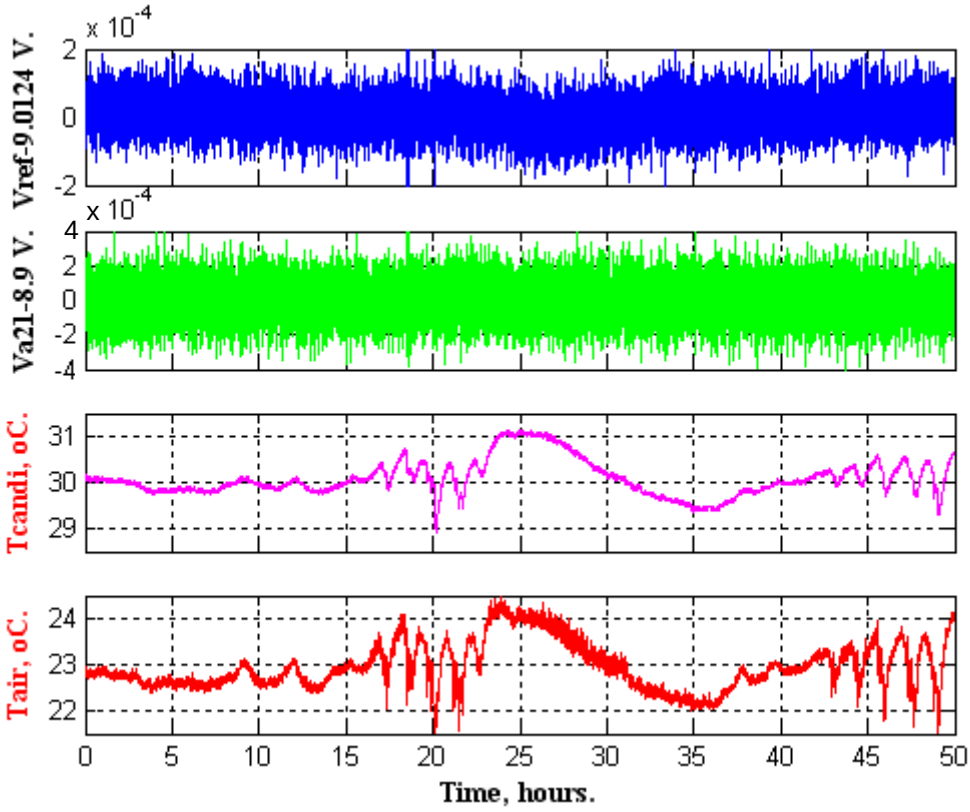

FIGURE 16. The SP DAC stability, 50 hours capture.

To see the *Vref* behaviour in detail, the average of every 100 points was plotted (Fig. 17).

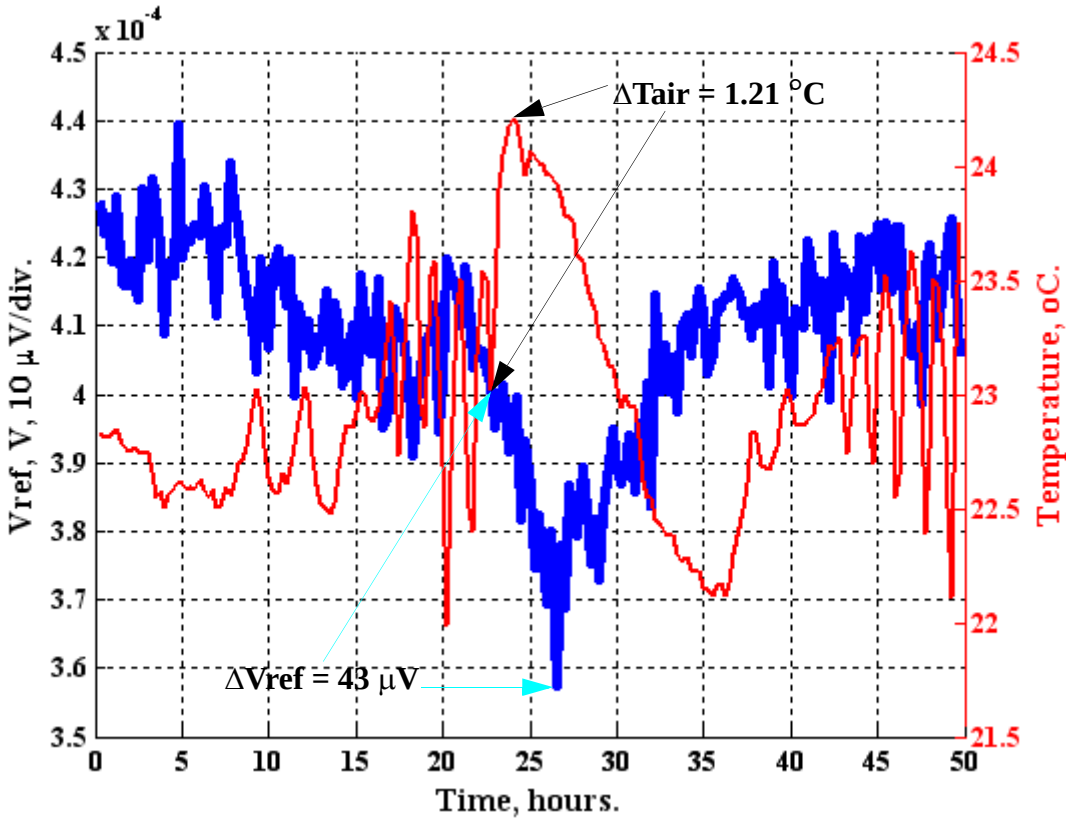

FIGURE 17. *Vref* and *Tair*, one point corresponds to 100 points average from Fig. 16.

When the temperature goes up rapidly (about hour 23), *Vref* (Fig. 17) starts to go down and at about hour 27 hits the minimum. The corresponding *Vref* drift consists 43 μV and the temperature varies for - 1.21 °C (23 °C - 24.21 °C).

•*Vref* drift is 36 μV / °C or 3.6 ppm / °C.

The following slow temperature drop from 24.21 °C to about 22.1 °C (2.11 °C change) forces the *Vref* to rise up for about 58 μV. The drift in this case is:

•*Vref* drift is 28 μV / °C or 2.8 ppm / °C.

The stability results with the feedback loop, closed through the ADC, are better than +/- 500 μV limit over 24 hours from the requirements. Calculated TCs are less than the TC limit of +/- 14.3 ppm / °C from the requirements.

Probably, the temperature drift above is the combination of the input signal processing channel drift and the External Reference drift, specified as 5.4 ppm / °C TC at 9 V scale.

The same test was performed with the CL DAC and ADCs. The *Va3* and *Va22* deviations were +/- 300 μV and +/- 250 μV respectively (Fig. 18).

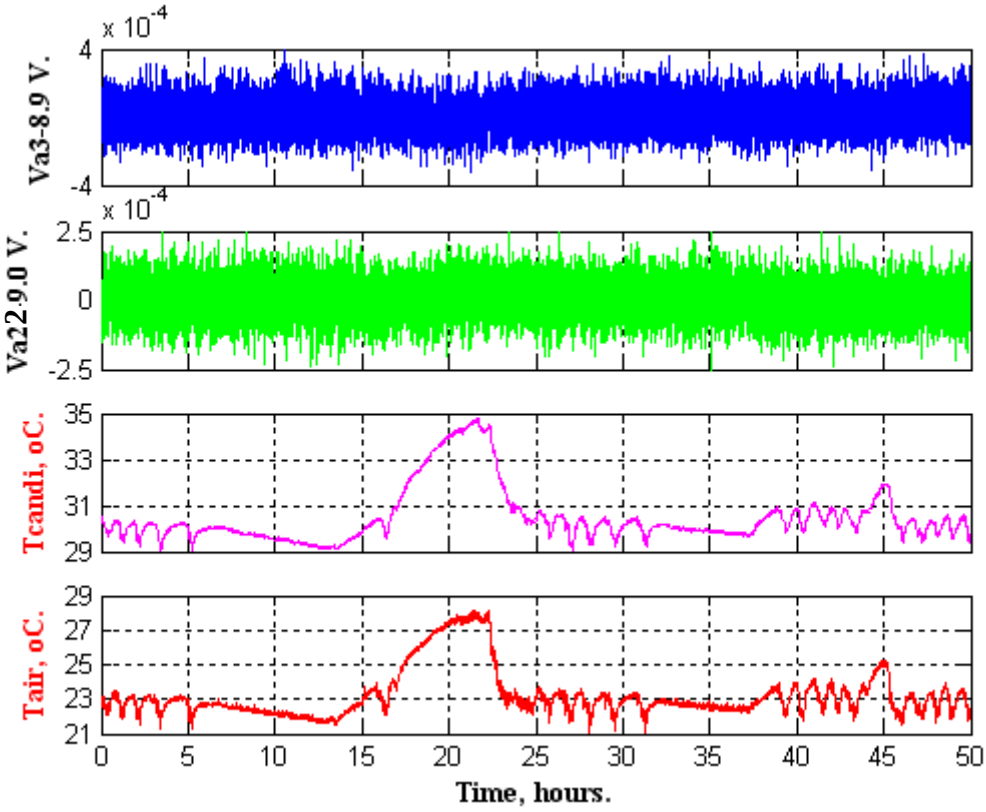

FIGURE 18. The ADC2 and ADC3 stability.

The feedback loop was closed through the ADC2. The feedback signal was bouncing within the CL DAC bit range and after few steps the CL DAC was tuned to the required value and then did not change over 50 hours. So the feedback was not in use most of the time.

The *Va3* and *Va22* average are shown on the Figure 19 below. The *Va3* and *Va22* drifts due to 6 °C temperature rise are 55 μV and 51 μV respectively. When the temperature goes back, the *Va3* was drifted for about 69 μV over 5.3 °C.

- *Va22* TC = 51 μV / 6 °C = 0.9 ppm/°C;
- *Va3* TC = 69 μV / 5.3 °C = 1.3 ppm/°C .
- It provides proof of very good ADC stability and low TC.

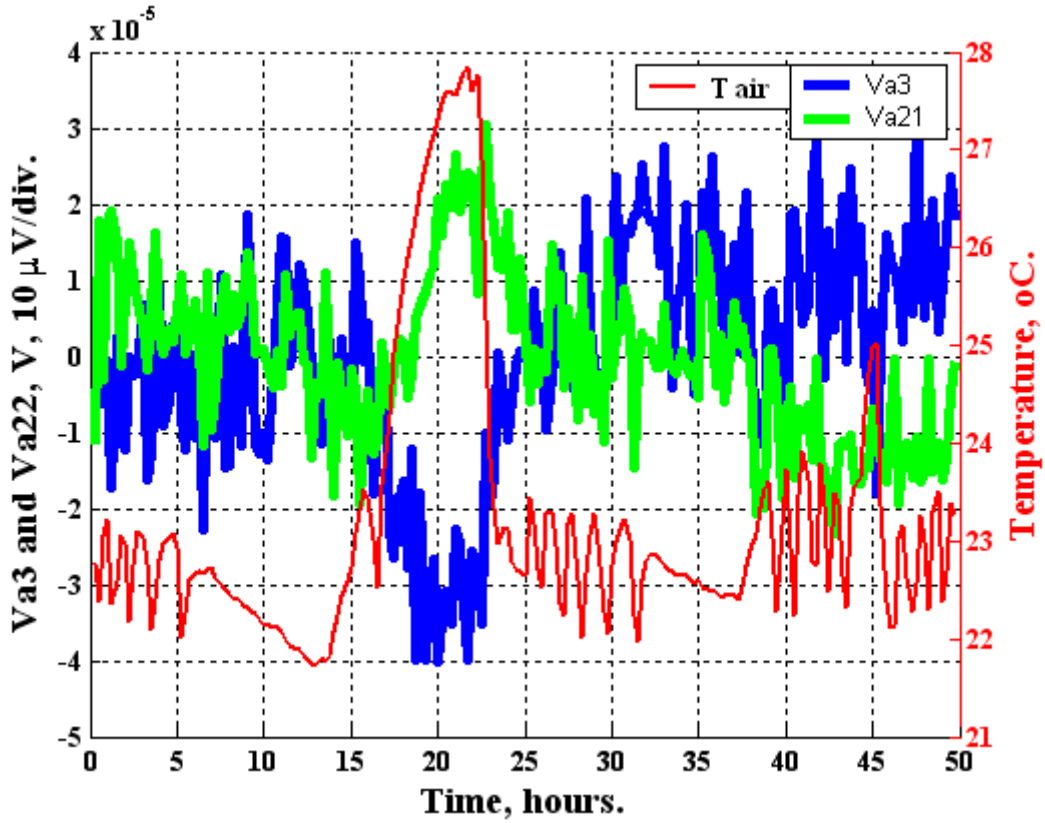

FIGURE 19. ADC3 and ADC2 stability over the time and the temperature.

Since the CL DAC behaviour over the temperature was not clear form this test, the following steps were made to find the CL DAC TC.

13.4 CL DAC temperature drift.

To check the CL DAC temperature drift, the CANDI board was put into an oven, the CL DAC output was connected via a coaxial cable to an external multimeter, located outside the oven. The temperature was changing in the following order: + 25 °C to + 45 °C then to + 65 °C and backward, this cycle was repeated twice. The constant temperature interval duration was 40 min, the ramp - 30 min.

The CL DAC TC was calculated according to the following equation:

$$TC = \frac{\Delta V}{\Delta T} \cdot \frac{1}{10} \cdot 10^6, ppm/^oC,$$

where ΔV is the CL DAC output voltage difference, corresponded to ΔT - the air temperature difference at the initial constant temperature and the next constant

temperature after the ramp; 10 - normalization to the CL DAC 10 V output signal; 10^6 - coefficient to get the answer in parts-per-million units.

The test results are shown on Figure 20 below. The max TC = -1.53 ppm / °C.

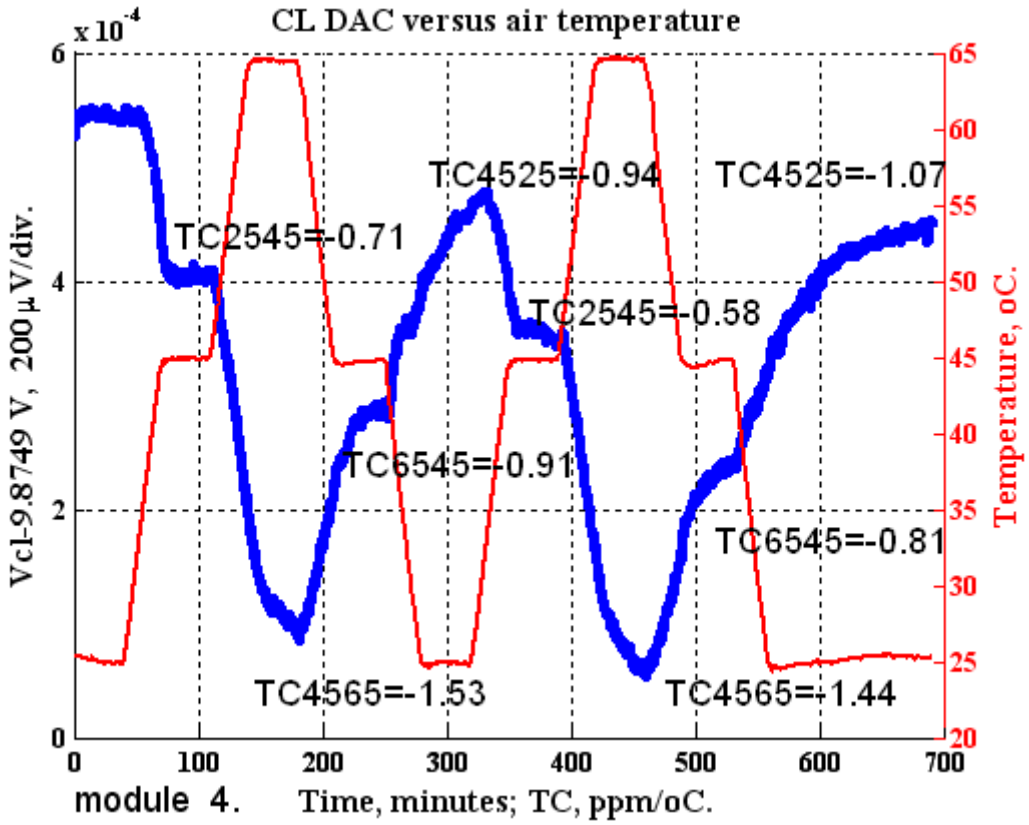

FIGURE 20. CL DAC output signal (blue / fat) at the temperature (red / thin) over 11 and half hours.

Five CANDI boards were tested, the results are shown below (Tab. 12).

TABLE 12. The CL DAC Temperature Coefficient.

Module Number	spare	1	4	15	17
TC, ppm / °C; MAX	1.44	0.86	1.53	1.33	1.23

•The CL DAC Temperature Coefficient varies from 0.9 to 1.53 ppm / °C. The CL DAC TC is much less than the requirements limit of 14 ppm/ °C.

•The CL DAC is stable over time and temperature, and it is a reliable calibration source.

14.0 Test results summary.

The 170 CANDI boards were fabricated and assembled. Their performance was tested and exceeds requirements.

•Accuracy after the calibration is within +/- 300 μV over +/- full scale.

•The setpoint signal to noise ratio varies from 17.7 to 17.3 ENOB. The current readback ranges from 18 to 17.5 ENOB. The production modules ENOB is less by about 1.25 bit due to reducing *Fdr* and decreasing the oversampling ratio by 16 averages.

•The setpoint stability over 50 hours is about +/- 200 μV; TC < 4 ppm / °C. The analog readback stability is +/- 250 μV; TC = 1 ppm / °C.

•The CL DAC TC is between 0.9 ppm / °C and 1.53 ppm / °C.

15.0 CANDI board assembling, special concern.

1. Item 24, connector P4 - top mount. Items 22 and 23, connectors P2 and P3 - bottom mount.

2. Items 27 and 31. Resistive voltage dividers R3, R8, R9, R33, R34 have labels on their cases - 2 K and 10 K. They should be mounted according to the PCB labels - 2.0 K and 10 K (Fig. 21 a).

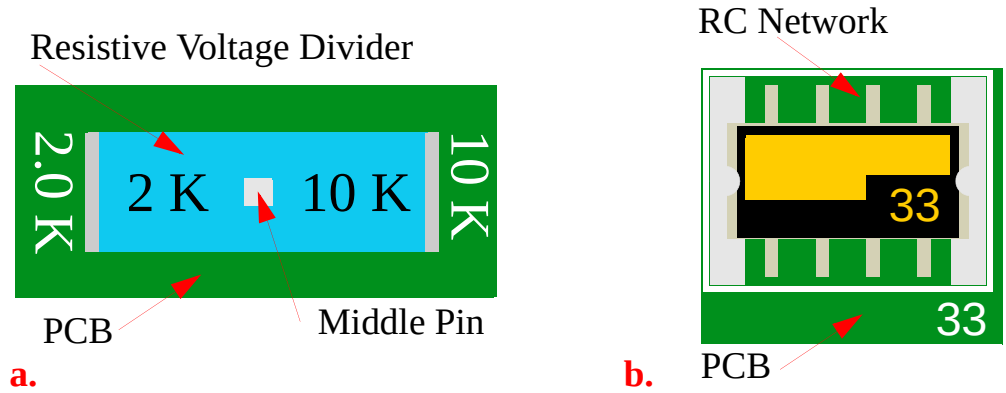

FIGURE 21. Mount the Resistive Voltage Dividers (a.) and RC network (b.) according to the PCB labels.

Please, pay special attention to the Resistive Voltage Dividers solder, all three pins should be properly connected. It is easy to burn!

3. Item 59. RC networks U33, U34, U35, U36, U37, U40, U41 have the label - 33 on their cases. They should be mounted so that the label on the case will be on the side of the PCB label 33 (Fig. 21 b).

4. Item 36. 0 Ω resistors, mount only R17, R67, R35, R46, R58. Don’t load others.

5. Item 1. Shielding Box fence B1 - top mount.

After mounting the fence on the PCB, take out the support bar from the fence's top right corner (Fig. 22 a.) and put on the Shielding Box top cover.

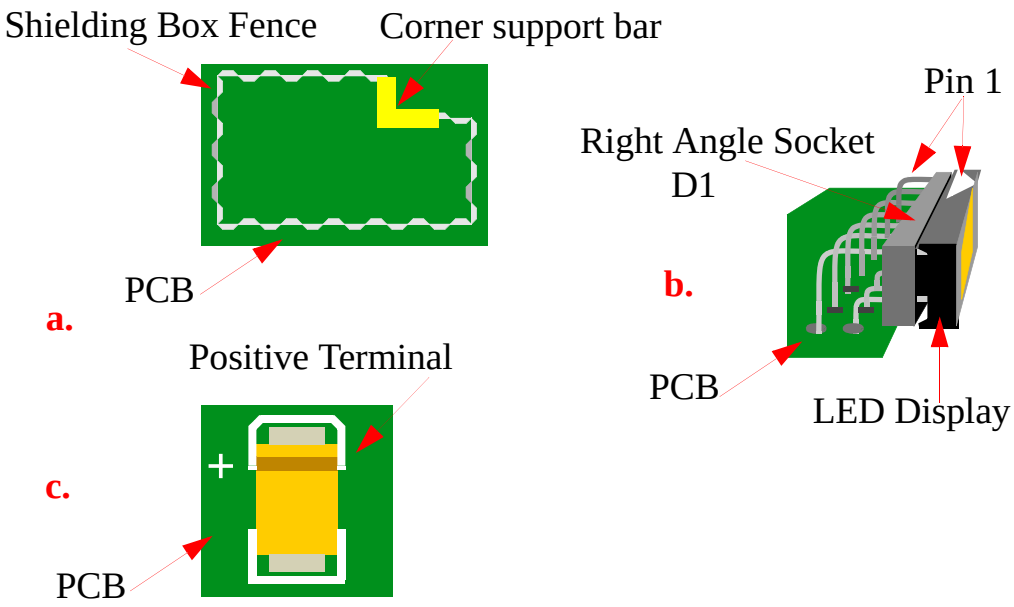

FIGURE 22. The Shielding Box fence and the corner support bar (a.), the LED Display assembling (b.), the polarized capacitor (c.).

6. Item 16. Mount the right angle socket D1 on the PCB top. Insert the LED Display into the socket, pin 1 to pin1 (Fig. 22 b.).

7. All polarized capacitors shall be mount according to the PCB labels. On the side of the capacitor's positive terminal there is a "+" label (Fig. 22 c.).

CC: candi manual.fm

August 28, 2003