MPS Link Node Inputs: 2020-01-02-a

Contents

1 Link Node 10 5
2 Link Node 11 7
3 Link Node 12 10
4 Link Node 13 11
5 Link Node 14 12
6 Link Node 15 13
7 Link Node 16 14
8 Link Node 17 15
9 Link Node 18 16
10 Link Node 19 17
11 Link Node 20 18
12 Link Node 21 19
13 Link Node 22 20
14 Link Node 23 21
15 Link Node 24 22
16 Link Node 25 23
17 Link Node 27 26
18 Link Node 28 27
19 Link Node 29 28
20 Link Node 30 29
21 Link Node 31 31
22 Link Node 32 33

23 Link Node 33 **36**

24 Link Node 34 **39**

25 Link Node 35 **40**

26 Link Node 36 **43**

27 Link Node 37 **46**

28 Link Node 38 **48**

29 Link Node 39 **49**

30 Link Node 40 **51**

31 Link Node 41 **54**

32 Link Node 42 **55**

33 Link Node 43 **58**

34 Link Node 44 **59**

35 Link Node 125 **60**

36 Link Node 127 **61**

37 Link Node 129 **62**

38 Link Node 132 **63**

39 Link Node 134 **64**

40 Link Node 136 **65**

41 Link Node 138 **66**

42 Link Node 139 **67**

43 Link Node 140 **68**

44 Link Node 141 **69**

45 Link Node 143 **70**

46 Link Node 144 **71**

47 Link Node 145 **72**

48 Link Node 195 **73**

49 Link Node 196 **74**

50 Link Node 199 **75**

51 Link Node 202 **76**

52 Link Node 204 **77**

53 Link Node 205 **78**

54 Link Node 206 **79**

55 Link Node 208 **80**

56 Link Node 210 **81**

57 Link Node 213 **82**

58 Link Node 214 **83**

59 Link Node 215 **84**

60 Link Node 216 **85**

1 Link Node 10

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	1	1	COLL:LI20:900:SCRAPER_FS	MPS_SCRAPPER_FLOW_OK_LI20	STATE
□	1	2	VVPG:LI20:1:POSITION	SLOW_VLV_OPEN_LI20	STATE
□	1	3	VVFS:LI20:1:FAST_VLV	FAST_VLV_OPEN_LI20	STATE
□	1	4	MMG:LI20:1:MM_GAUGE	MPS_MM_GAUGE_OK_LI20	STATE
□	1	5	PPS:LI20:72:SECTOR	PPS_SECTOR_OK_SECURE_LI20	STATE
□	1	6	SBST:LI20:1:SBST_OK	MPS_SBST_OK_READY_LI20	STATE
□	1	7	VVS:LI20:1:BREAKER	VVS_BRKR_OK_READY_LI20	STATE
□	1	8	STPR:LI20:1:BASII_POS	BK_BEAM_STPR_LI20	STATE
□	1	9	DUMP:LI20:1:FLOW_SW	DUMP_20_1_FS	STATE
□	1	10	PLIC:LI20:1:SUM	PIC_SUM_LI20	STATE
□	1	11	PICM:LI20:1:HV_PWR	PICM_LI20_1_HV_PWR	STATE
□	2	1	BEND:DMP1:400:BACT_WDOG	BEND_DMP1_400_BACT_WDOG	STATE
□	2	2	MPS:UND1:950:SXRSS_WDOG	MPS_UND1_950_SXRSS_WDOG	STATE
□	2	3	MPS:UND1:950:SX_SS_UND	MPS_UND1_950_SX_SS_UND	STATE
□	2	4	MPS:UND1:950:SX_SASE_X	MPS_UND1_950_SX_SASE_X	STATE
□	2	5	MPS:UND1:950:SX_SS_X	MPS_UND1_950_SX_SS_X	STATE
□	2	6	MPS:UND1:950:SX_HRMNC_X	MPS_UND1_950_SX_HRMNC_X	STATE
□	2	7	MPS:UND1:950:SX_SS_ENERGY	MPS_UND1_950_SX_SS_ENERGY	STATE
□	2	8	MPS:UND1:950:SX_HRMNC_ENERGY	MPS_UND1_950_SX_HRMNC_ENERGY	STATE
□	3	1	MPS:IN20:200:LHSHT1_OUT	MPS_IN20_200_LHSHT1_OUT	FAULT
□	3	2	MPS:IN20:200:LHSHT1_IN	MPS_IN20_200_LHSHT1_IN	FAULT
□	3	3	MPS:IN20:200:LHSHT2_OUT	MPS_IN20_200_LHSHT2_OUT	FAULT
□	3	4	MPS:IN20:200:LHSHT2_IN	MPS_IN20_200_LHSHT2_IN	FAULT
□	3	5	MPS:IN20:200:MSHT1_OUT	MPS_IN20_200_MSHT1_OUT	FAULT
□	3	6	MPS:IN20:200:MSHT1_IN	MPS_IN20_200_MSHT1_IN	FAULT
□	3	7	MPS:IN20:200:MSHT2_OUT	MPS_IN20_200_MSHT2_OUT	FAULT
□	3	8	MPS:IN20:200:MSHT2_IN	MPS_IN20_200_MSHT2_IN	FAULT
□	3	9	MPS:IN20:200:ANDALLACTV	MPS_IN20_200_ANDALLACTV	STATE
□	3	10	MPS:IN20:200:ANDCH1ACTV	MPS_IN20_200_ANDCH1ACTV	STATE
□	3	11	MPS:IN20:200:ANDCH2ACTV	MPS_IN20_200_ANDCH2ACTV	STATE
□	3	12	MPS:IN20:200:ANDCH3ACTV	MPS_IN20_200_ANDCH3ACTV	STATE
□	3	13	MPS:IN20:200:ANDCH4ACTV	MPS_IN20_200_ANDCH4ACTV	STATE
□	3	14	MPS:IN20:200:ANDCH5ACTV	MPS_IN20_200_ANDCH5ACTV	STATE
□	3	15	MPS:IN20:200:ANDCH6ACTV	MPS_IN20_200_ANDCH6ACTV	STATE
□	3	16	MPS:IN20:200:ANDCH7ACTV	MPS_IN20_200_ANDCH7ACTV	STATE
□	4	1	MPS:IN20:200:ANDCH8ACTV	MPS_IN20_200_ANDCH8ACTV	STATE
□	4	2	USEG:UND1:1:ALL_OUT	USEG_UND1_1_ALL_OUT	STATE
□	4	3	XTAL:FEE1:441:PULSEENERGY	XTAL_FEE1_441_PULSEENERGY	THRESHOLD

continued on next page...

. . . continued from previous page

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	4	4	GDET:FEE1:1:CAL_OK	GDET_FEE1_1_CAL_OK	STATE
□	5	1	MPS:IN20:100:ANDALLACTV	MPS_IN20_100_ANDALLACTV	STATE
□	5	2	MPS:IN20:100:ANDCH1ACTV	MPS_IN20_100_ANDCH1ACTV	STATE
□	5	3	MPS:IN20:100:ANDCH2ACTV	MPS_IN20_100_ANDCH2ACTV	STATE
□	5	4	MPS:IN20:100:ANDCH3ACTV	MPS_IN20_100_ANDCH3ACTV	STATE
□	5	5	MPS:IN20:100:ANDCH4ACTV	MPS_IN20_100_ANDCH4ACTV	STATE
□	5	6	MPS:IN20:100:ANDCH5ACTV	MPS_IN20_100_ANDCH5ACTV	STATE
□	5	7	MPS:IN20:100:ANDCH6ACTV	MPS_IN20_100_ANDCH6ACTV	STATE
□	5	8	MPS:IN20:100:ANDCH7ACTV	MPS_IN20_100_ANDCH7ACTV	STATE
□	5	9	MPS:IN20:100:ANDCH8ACTV	MPS_IN20_100_ANDCH8ACTV	STATE

2 Link Node 11

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	1	1	VVPG:IN20:155:POSITION	VV_BL155	STATE
□	1	2	VVPG:IN20:435:POSITION	VV_BL435	STATE
□	1	3	VVPG:IN20:545:POSITION	VV_BL545	STATE
□	1	4	VVPG:IN20:635:POSITION	VV_BL635	STATE
□	1	5	VVPG:IN20:915:POSITION	VV_IS915	STATE
□	1	6	VVMG:IN20:175:POSITION	VV_BL175	STATE
□	1	7	VVMG:LI21:196:POSITION	VV_BL195	STATE
□	1	8	MKSU:LI20:61:WGVACSUM	WGVACGUN	STATE
□	1	9	YAGS:IN20:211:OUT_LMTSW	YAGS_IN20_211_OUT_LMTSW	STATE
□	1	10	YAGS:IN20:211:IN_LMTSW	YAGS_IN20_211_IN_LMTSW	STATE
□	1	11	YAGS:IN20:241:OUT_LMTSW	YAGS_IN20_241_OUT_LMTSW	STATE
□	1	12	YAGS:IN20:241:IN_LMTSW	YAGS_IN20_241_IN_LMTSW	STATE
□	1	13	YAGS:IN20:351:OUT_LMTSW	YAGS_IN20_351_OUT_LMTSW	STATE
□	1	14	YAGS:IN20:351:IN_LMTSW	YAGS_IN20_351_IN_LMTSW	STATE
□	1	15	YAGS:IN20:471:OUT_LMTSW	YAGS_IN20_471_OUT_LMTSW	STATE
□	1	16	YAGS:IN20:471:IN_LMTSW	YAGS_IN20_471_IN_LMTSW	STATE
□	2	1	YAGS:IN20:841:OUT_LMTSW	YAGS_IN20_841_OUT_LMTSW	STATE
□	2	2	YAGS:IN20:841:IN_LMTSW	YAGS_IN20_841_IN_LMTSW	STATE
□	2	3	YAGS:IN20:921:OUT_LMTSW	YAGS_IN20_921_OUT_LMTSW	STATE
□	2	4	YAGS:IN20:921:IN_LMTSW	YAGS_IN20_921_IN_LMTSW	STATE
□	2	5	YAGS:LI21:995:OUT_LMTSW	YAGS_LI21_995_OUT_LMTSW	STATE
□	2	6	YAGS:LI21:995:IN_LMTSW	YAGS_LI21_995_IN_LMTSW	STATE
□	2	7	OTRS:IN20:541:OUT_LMTSW	OTRS_IN20_541_OUT_LMTSW	STATE
□	2	8	OTRS:IN20:541:IN_LMTSW	OTRS_IN20_541_IN_LMTSW	STATE
□	2	9	OTRS:IN20:571:OUT_LMTSW	OTRS_IN20_571_OUT_LMTSW	STATE
□	2	10	OTRS:IN20:571:IN_LMTSW	OTRS_IN20_571_IN_LMTSW	STATE
□	2	11	OTRS:IN20:621:OUT_LMTSW	OTRS_IN20_621_OUT_LMTSW	STATE
□	2	12	OTRS:IN20:621:IN_LMTSW	OTRS_IN20_621_IN_LMTSW	STATE
□	2	13	OTRS:IN20:711:OUT_LMTSW	OTRS_IN20_711_OUT_LMTSW	STATE
□	2	14	OTRS:IN20:711:IN_LMTSW	OTRS_IN20_711_IN_LMTSW	STATE
□	2	15	OTRS:IN20:991:OUT_LMTSW	OTRS_IN20_991_OUT_LMTSW	STATE
□	2	16	OTRS:IN20:991:IN_LMTSW	OTRS_IN20_991_IN_LMTSW	STATE
□	3	1	OTRS:LI21:237:OUT_LMTSW	OTRS_LI21_237_OUT_LMTSW	STATE
□	3	2	OTRS:LI21:237:IN_LMTSW	OTRS_LI21_237_IN_LMTSW	STATE
□	3	3	OTRS:LI21:291:OUT_LMTSW	OTRS_LI21_291_OUT_LMTSW	STATE
□	3	4	OTRS:LI21:291:IN_LMTSW	OTRS_LI21_291_IN_LMTSW	STATE
□	3	5	TORO:IN20:215:CHASIM11	CHASIM11	STATE
□	3	6	TORO:IN20:431:CHASIM12	CHASIM12	STATE

continued on next page. . .

. . . continued from previous page

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	3	7	MIRR:IN20:191:AM1_OUT	MR_BL191	STATE
□	3	8	WKFL:IN20:231:OUT	WL_BL231_OUT	STATE
□	3	9	WKFL:IN20:231:IN	WL_BL231_IN	STATE
□	3	10	TIU:LI20:1:RECEIVER	TIU_2921	STATE
□	3	11	COLL:LI21:235:KLIXON	CE11_KLIXON	STATE
□	3	12	DUMP:LI21:305:FLOW_SW	FS_BL305	STATE
□	3	13	FLTR:IN20:130:FLT1_OUT	LHATTEN_OUT_LIMIT	STATE
□	3	14	FLTR:IN20:130:FLT1_IN	LHATTEN_IN_LIMIT	STATE
□	3	15	FLTR:IN20:450:FLT1_OUT	LHPHD_OUT_LIMIT	STATE
□	3	16	FLTR:IN20:450:FLT1_IN	LHPHD_IN_LIMIT	STATE
□	4	1	STPR:IN20:BL551:POSITION	ST_BL551	STATE
□	4	2	TORO:IN20:BL215:MPS_STATE	TR_BL215	STATE
□	4	3	TORO:IN20:203:TC203L1	TC203L1	STATE
□	4	4	TORO:IN20:203:TC203L2	TC203L2	STATE
□	4	5	TORO:IN20:971:TC2S1L1	TC2S1L1	STATE
□	4	6	TORO:IN20:971:TC2S1L2	TC2S1L2	STATE
□	4	7	TORO:LI21:205:TCBC1L1	TCBC1L1	STATE
□	4	8	TORO:LI21:205:TCBC1L2	TCBC1L2	STATE
□	4	9	DUMP:LI21:305:TD11_OUT	TD11_OUT_LIMIT	STATE
□	4	10	DUMP:LI21:305:TD11_IN	TD11_IN_LIMIT	STATE
□	4	11	STPR:LI20:1:BASII_OUT	BASII_ST_OUT_LIMIT	STATE
□	4	12	STPR:LI20:1:BASII_IN	BASII_ST_IN_LIMIT	STATE
□	4	14	XTAL:UND1:1650:POSITIONSTAT	XTAL_UND1_1650_POSITIONSTAT	STATE
□	4	15	BEND:DMP1:400:INTOL_BRANGE	BEND_DMP1_400_INTOL_BRANGE	STATE
□	4	16	OTRS:IN20:471:IN_LMTSW	OTRH2_IN_LIMIT	STATE
□	5	1	SEPT:LI19:172:HLAM_ENB	HLAM_ENB	STATE
□	5	2	KICK:LI20:7:EKIC_ENB	EKIC_ENB	STATE
□	5	3	JMTR:IN20:1:JOULEMTR	JOULEMTR	STATE
□	5	4	JMTR:IN20:2:JOULEMTR2	JOULEMTR2	STATE
□	5	5	COLL:LI21:235:OUT_LMTSW	CE11_X1_X2_MOTOR	STATE
□	5	6	MOVR:LI21:235:BC1_POS_OK	BC1_CHICANE	STATE
□	5	7	BEND:UND1:1640:INTOL_BMIN	BEND_UND1_1640_INTOL_BMIN	STATE
□	5	8	MBRC:LI20:8:BEAMPERM	BEAM_PERMIT	STATE
□	5	9	OTRS:IN20:465:OUT_LMTSW	OTRH1_OUT_LIMIT	STATE
□	5	10	OTRS:IN20:465:IN_LMTSW	OTRH1_IN_LIMIT	STATE
□	5	11	OTRS:IN20:471:OUT_LMTSW	OTRH2_OUT_LIMIT	STATE
□	5	12	BLEN:LI21:265:BL11_OUT	MIR_BL11_OUT	STATE
□	5	13	BLEN:LI21:265:BL11_IN	MIR_BL11_IN	STATE
□	5	14	MBRC:IN20:1:SS_MODE	SS_MODE	STATE
□	5	15	MBRC:IN20:1:SS_REQST	SS_REQST	STATE
□	5	16	COLL:LI21:235:FLOW_SW	COLL_LI21_235_OPEN	STATE

continued on next page. . .

. . . continued from previous page

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	6	1	SHUT:IN20:1:FAULT	SHFLT	STATE
□	6	2	SHUT:IN20:1:BYPASS	SHFLTBYP	STATE
□	6	3	BEND:IN20:751:STATE_ON	BEND_IN20_751_OK	STATE
□	6	4	BEND:IN20:751:STATE_OFF	BEND_IN20_751_OFF	STATE
□	6	5	BEND:IN20:231:STATE_ON	BEND_IN20_231_OK	STATE
□	6	6	BEND:IN20:231:STATE_OFF	BEND_IN20_231_OFF	STATE
□	6	7	BEND:IN20:931:STATE_ON	BEND_IN20_931_OK	STATE
□	6	8	BEND:IN20:931:STATE_OFF	BEND_IN20_931_OFF	STATE
□	6	9	XTAL:UND1:1650:IN_ENCDR	XTAL_UND1_1650_IN_ENCDR	STATE
□	6	10	MIRR:FEE1:1560:ENERGY	MIRR_FEE1_1560_ENERGY	STATE
□	6	11	IOC:IN20:MP01:HEARTBEATSUM	MN_HEART	STATE
□	6	12	XTAL:FEE1:441:ENERGY	XTAL_FEE1_441_ENERGY	STATE
□	6	15	VVFV:IN20:785:OPEN_LMTSW	VVFV_IN20_785_OPEN_LMTSW	POSITION
□	6	16	KLYS:LI20:61:PEAKPOWER	FLT_20_6_TRP	STATE
□	7	8	PICM:IN20:665:NO_TRIG	PICM_IN20_665_NO_TRIG	MISSED
□	9	1	PICM:IN20:665:LOSSL	PICM_IN20_665_LOSSL	THRESHOLD
□	9	2	PICM:IN20:665:LOSSH	PICM_IN20_665_LOSSH	THRESHOLD
□	10	1	PICM:IN20:775:LOSSL	PICM_IN20_775_LOSSL	THRESHOLD
□	10	2	PICM:IN20:775:LOSSH	PICM_IN20_775_LOSSH	THRESHOLD
□	11	1	PICM:IN20:933:LOSSL	PICM_IN20_933_LOSSL	THRESHOLD
□	11	2	PICM:IN20:933:LOSSH	PICM_IN20_933_LOSSH	THRESHOLD
□	12	1	PICM:IN20:185:LOSSL	PICM_IN20_185_LOSSL	THRESHOLD
□	12	2	PICM:IN20:185:LOSSH	PICM_IN20_185_LOSSH	THRESHOLD
□	13	1	PICM:IN20:232:LOSSL	PICM_IN20_232_LOSSL	THRESHOLD
□	13	2	PICM:IN20:232:LOSSH	PICM_IN20_232_LOSSH	THRESHOLD
□	14	1	PICM:IN20:245:LOSSL	PICM_IN20_245_LOSSL	THRESHOLD
□	14	2	PICM:IN20:245:LOSSH	PICM_IN20_245_LOSSH	THRESHOLD

3 Link Node 12

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	1	2	VVPG:LI21:1:POSITION	SLOW_VLV_OPEN_LI21	STATE
□	1	4	MMG:LI21:1:MM_GAUGE	MPS_MM_GAUGE_OK_LI21	STATE
□	1	5	PPS:LI21:72:SECTOR	PPS_SECTOR_OK_SECURE_LI21	STATE
□	1	6	SBST:LI21:1:SBST_OK	MPS_SBST_OK_READY_LI21	STATE

4 Link Node 13

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	1	1	COLL:LI22:900:SCRAPER_FS	MPS_SCRAPPER_FLOW_OK_LI22	STATE
□	1	2	VVPG:LI22:1:POSITION	SLOW_VLV_OPEN_LI22	STATE
□	1	3	VVFS:LI22:1:FAST_VLV	FAST_VLV_OPEN_LI22	STATE
□	1	4	MMG:LI22:1:MM_GAUGE	MPS_MM_GAUGE_OK_LI22	STATE
□	1	5	PPS:LI22:72:SECTOR	PPS_SECTOR_OK_SECURE_LI22	STATE
□	1	6	SBST:LI22:1:SBST_OK	MPS_SBST_OK_READY_LI22	STATE
□	1	7	VVS:LI22:1:BREAKER	VVS_BRKR_OK_READY_LI22	STATE

5 Link Node 14

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	1	1	COLL:LI23:900:SCRAPER_FS	MPS_SCRAPPER_FLOW_OK_LI23	STATE
□	1	2	VVPG:LI23:1:POSITION	SLOW_VLV_OPEN_LI23	STATE
□	1	3	VVFS:LI23:1:FAST_VLV	FAST_VLV_OPEN_LI23	STATE
□	1	4	MMG:LI23:1:MM_GAUGE	MPS_MM_GAUGE_OK_LI23	STATE
□	1	5	PPS:LI23:72:SECTOR	PPS_SECTOR_OK_SECURE_LI23	STATE
□	1	6	SBST:LI23:1:SBST_OK	MPS_SBST_OK_READY_LI23	STATE

6 Link Node 15

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	1	1	COLL:LI24:900:SCRAPER_FS	MPS_SCRAPPER_FLOW_OK_LI24	STATE
□	1	2	VVPG:LI24:1:POSITION	SLOW_VLV_OPEN_LI24	STATE
□	1	3	VVFS:LI24:1:FAST_VLV	FAST_VLV_OPEN_LI24	STATE
□	1	4	MMG:LI24:1:MM_GAUGE	MPS_MM_GAUGE_OK_LI24	STATE
□	1	5	PPS:LI24:72:SECTOR	PPS_SECTOR_OK_SECURE_LI24	STATE
□	1	6	SBST:LI24:1:SBST_OK	MPS_SBST_OK_READY_LI24	STATE
□	1	7	VVS:LI24:1:BREAKER	VVS_BRKR_OK_READY_LI24	STATE
□	1	11	PICM:LI24:1:HV_PWR	PICM_LI24_1_HV_PWR	STATE
□	1	14	TORO:LI24:707:TCBC2L1	TCBC2L1	STATE
□	1	15	TORO:LI24:707:TCBC2L2	TCBC2L2	STATE
□	1	16	TORO:LI24:1:CHASIMB2	CHASIMB2	STATE

7 Link Node 16

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	1	1	OTRS:LI24:807:OUT_LMTSW	OTRS_LI24_807_OUT_LMTSW	STATE
□	1	2	OTRS:LI24:807:IN_LMTSW	OTRS_LI24_807_IN_LMTSW	STATE
□	1	5	OTRS:LI25:920:OUT_LMTSW	OTR_TCAV_OUT	STATE
□	1	6	OTRS:LI25:920:IN_LMTSW	OTR_TCAV_IN	STATE
□	1	7	CHIC:LI24:790:BC2_LGPS	BC2_LGPS	STATE
□	1	8	PICM:LI24:1:GAS_PRESS	PIC_GAS_PRESS	STATE
□	1	9	BLEN:LI25:886:BL22_OUT	BL22_OUT	STATE
□	1	10	BLEN:LI25:886:BL22_IN	BL22_IN	STATE
□	1	11	COLL:LI24:805:POSITION	COL_805	STATE
□	1	12	COLL:LI24:805:FLOW_SW	COL_805_FLOSW	STATE
□	1	13	VVPG:LI24:710:POSITION	VV21	STATE
□	1	14	VVPG:LI24:896:POSITION	VV22	STATE
□	1	15	CHIC:LI24:805:BC2_POS_OK	BC2_CHICANE	STATE
□	1	16	CHIC:LI24:790:BC2_BEND	BC2_BEND	STATE
□	7	8	PICM:LI24:791:NO_TRIG	PICM_LI24_791_NO_TRIG	MISSED
□	9	1	PICM:LI24:791:LOSSL	PICM_LI24_791_LOSSL	THRESHOLD
□	9	2	PICM:LI24:791:LOSSH	PICM_LI24_791_LOSSH	THRESHOLD
□	10	1	PICM:LI24:811:LOSSL	PICM_LI24_811_LOSSL	THRESHOLD
□	10	2	PICM:LI24:811:LOSSH	PICM_LI24_811_LOSSH	THRESHOLD

8 Link Node 17

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	1	1	COLL:LI25:900:SCRAPER_FS	MPS_SCRAPPER_FLOW_OK_LI25	STATE
□	1	3	VVFS:LI25:1:FAST_VLV	FAST_VLV_OPEN_LI25	STATE
□	1	4	MMG:LI25:1:MM_GAUGE	MPS_MM_GAUGE_OK_LI25	STATE
□	1	5	PPS:LI25:72:SECTOR	PPS_SECTOR_OK_SECURE_LI25	STATE
□	1	6	SBST:LI25:1:SBST_OK	MPS_SBST_OK_READY_LI25	STATE

9 Link Node 18

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	1	1	COLL:LI26:900:SCRAPER_FS	MPS_SCRAPPER_FLOW_OK_LI26	STATE
□	1	2	VVPG:LI26:1:POSITION	SLOW_VLV_OPEN_LI26	STATE
□	1	3	VVFS:LI26:1:FAST_VLV	FAST_VLV_OPEN_LI26	STATE
□	1	4	MMG:LI26:1:MM_GAUGE	MPS_MM_GAUGE_OK_LI26	STATE
□	1	5	PPS:LI26:72:SECTOR	PPS_SECTOR_OK_SECURE_LI26	STATE
□	1	6	SBST:LI26:1:SBST_OK	MPS_SBST_OK_READY_LI26	STATE
□	1	7	VVS:LI26:1:BREAKER	VVS_BRKR_OK_READY_LI26	STATE

10 Link Node 19

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	1	1	COLL:LI27:900:SCRAPER_FS	MPS_SCRAPPER_FLOW_OK_LI27	STATE
□	1	2	VVPG:LI27:1:POSITION	SLOW_VLV_OPEN_LI27	STATE
□	1	3	VVFS:LI27:1:FAST_VLV	FAST_VLV_OPEN_LI27	STATE
□	1	4	MMG:LI27:1:MM_GAUGE	MPS_MM_GAUGE_OK_LI27	STATE
□	1	5	PPS:LI27:72:SECTOR	PPS_SECTOR_OK_SECURE_LI27	STATE
□	1	6	SBST:LI27:1:SBST_OK	MPS_SBST_OK_READY_LI27	STATE

11 Link Node 20

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	1	1	COLL:LI28:900:SCRAPER_FS	MPS_SCRAPPER_FLOW_OK_LI28	STATE
□	1	2	VVPG:LI28:1:POSITION	SLOW_VLV_OPEN_LI28	STATE
□	1	3	VVFS:LI28:1:FAST_VLV	FAST_VLV_OPEN_LI28	STATE
□	1	4	MMG:LI28:1:MM_GAUGE	MPS_MM_GAUGE_OK_LI28	STATE
□	1	5	PPS:LI28:72:SECTOR	PPS_SECTOR_OK_SECURE_LI28	STATE
□	1	6	SBST:LI28:1:SBST_OK	MPS_SBST_OK_READY_LI28	STATE
□	1	7	VVS:LI28:1:BREAKER	VVS_BRKR_OK_READY_LI28	STATE
□	1	9	DUMP:LI28:5879:KLIXON	DUMP_5879_KLIXON_OK	STATE
□	1	10	DUMP:LI28:5879:FLOW_SW	DUMP_5879_FLOW_SW	STATE
□	1	11	STPR:LI28:950:BASII_IN	BASII_STOPPER_IN	STATE
□	1	12	STPR:LI28:950:BASII_OUT	BASII_STOPPER_OUT	STATE

12 Link Node 21

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	1	1	COLL:LI29:900:SCRAPER_FS	MPS_SCRAPPER_FLOW_OK_LI29	STATE
□	1	2	VVPG:LI29:1:POSITION	SLOW_VLV_OPEN_LI29	STATE
□	1	3	VVFS:LI29:1:FAST_VLV	FAST_VLV_OPEN_LI29	STATE
□	1	4	MMG:LI29:1:MM_GAUGE	MPS_MM_GAUGE_OK	STATE
□	1	5	PPS:LI29:72:SECTOR	PPS_SECTOR_OK_SECURE_LI29	STATE
□	1	6	SBST:LI29:1:SBST_OK	MPS_SBST_OK_READY_LI29	STATE
□	1	7	COLL:LI29:96:28_9_FS	FLOW_SW_28_9	STATE
□	1	8	COLL:LI29:146:29_1_FS	FLOW_SW_29_1	STATE
□	1	9	COLL:LI29:446:29_4_FS	FLOW_SW_29_4	STATE
□	1	10	COLL:LI29:546:29_5_FS	FLOW_SW_29_5	STATE
□	1	11	PLIC:LI29:1:SYS_OK	PLIC_SYSTEM_OK	STATE

13 Link Node 22

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	1	1	COLL:LI30:900:SCRAPER_FS	MPS_SCRAPPER_FLOW_OK_LI30	STATE
□	1	2	VVPG:LI30:1:POSITION	SLOW_VLV_OPEN_LI30	STATE
□	1	3	VVFS:LI30:1:FAST_VLV	FAST_VLV_OPEN_LI30	STATE
□	1	4	MMG:LI30:1:MM_GAUGE	MPS_MM_GAUGE_30_5_OK	STATE
□	1	5	PPS:LI30:72:SECTOR	PPS_SECTOR_OK_SECURE_LI30	STATE
□	1	6	SBST:LI30:1:SBST_OK	MPS_SBST_OK_READY_LI30	STATE
□	1	7	VVS:LI30:1:BREAKER	VVS_BRKR_OK_READY_LI30	STATE
□	1	8	VVPG:LI30:43:SLOW_VLV30_9	SLOW_VLV_30_9_OK_OPEN	STATE
□	1	9	MMG:LI30:1:MMG30_9	MPS_MM_GAUGE_30_9_OK	STATE
□	1	13	COLL:LI30:96:29_9_FS	FLOW_SW_29_9	STATE
□	1	14	COLL:LI30:146:30_1_FS	FLOW_SW_30_1	STATE
□	1	15	COLL:LI30:446:30_4_FS	FLOW_SW_30_4	STATE
□	1	16	COLL:LI30:546:30_5_FS	FLOW_SW_30_5	STATE
□	2	1	PICM:LI30:1:HV_PWR	PICM_LI30_1_HV_PWR	STATE
□	7	8	PICM:LI28:916:NO_TRIG	PICM_LI28_916_NO_TRIG	MISSED
□	9	1	PICM:LI28:916:LOSSL	PICM_LI28_916_LOSSL	THRESHOLD
□	9	2	PICM:LI28:916:LOSSH	PICM_LI28_916_LOSSH	THRESHOLD
□	10	1	PICM:LI29:146:LOSSL	PICM_LI29_146_LOSSL	THRESHOLD
□	10	2	PICM:LI29:146:LOSSH	PICM_LI29_146_LOSSH	THRESHOLD
□	11	1	PICM:LI29:446:LOSSL	PICM_LI29_446_LOSSL	THRESHOLD
□	11	2	PICM:LI29:446:LOSSH	PICM_LI29_446_LOSSH	THRESHOLD
□	12	1	PICM:LI29:546:LOSSL	PICM_LI29_546_LOSSL	THRESHOLD
□	12	2	PICM:LI29:546:LOSSH	PICM_LI29_546_LOSSH	THRESHOLD
□	13	1	PICM:LI29:801:LOSSL	PICM_LI29_801_LOSSL	THRESHOLD
□	13	2	PICM:LI29:801:LOSSH	PICM_LI29_801_LOSSH	THRESHOLD
□	17	1	PICM:LI29:956:LOSSL	PICM_LI29_956_LOSSL	THRESHOLD
□	17	2	PICM:LI29:956:LOSSH	PICM_LI29_956_LOSSH	THRESHOLD
□	18	1	PICM:LI30:146:LOSSL	PICM_LI30_146_LOSSL	THRESHOLD
□	18	2	PICM:LI30:146:LOSSH	PICM_LI30_146_LOSSH	THRESHOLD
□	19	1	PICM:LI30:446:LOSSL	PICM_LI30_446_LOSSL	THRESHOLD
□	19	2	PICM:LI30:446:LOSSH	PICM_LI30_446_LOSSH	THRESHOLD
□	20	1	PICM:LI30:546:LOSSL	PICM_LI30_546_LOSSL	THRESHOLD
□	20	2	PICM:LI30:546:LOSSH	PICM_LI30_546_LOSSH	THRESHOLD
□	21	1	PICM:LI30:801:LOSSL	PICM_LI30_801_LOSSL	THRESHOLD
□	21	2	PICM:LI30:801:LOSSH	PICM_LI30_801_LOSSH	THRESHOLD

14 Link Node 23

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	2	1	KICK:BSY0:66:PM1_ON	KICK_BSY0_66_PM1_ON	STATUS
□	2	2	KICK:BSY0:66:PM1_OFF	KICK_BSY0_66_PM1_OFF	STATUS
□	2	3	KICK:BSY0:66:PM1_TRIG_ENB	KICK_BSY0_66_PM1_TRIG_ENB	STATUS
□	2	4	KICK:BSY0:66:PM1_TRIG_LOCK	KICK_BSY0_66_PM1_TRIG_LOCK	STATUS
□	2	5	KICK:BSY0:66:PM2_ON	KICK_BSY0_66_PM2_ON	STATUS
□	2	6	KICK:BSY0:66:PM2_OFF	KICK_BSY0_66_PM2_OFF	STATUS
□	2	7	KICK:BSY0:66:PM2_TRIG_ENB	KICK_BSY0_66_PM2_TRIG_ENB	STATUS
□	2	8	KICK:BSY0:66:PM2_TRIG_LOCK	KICK_BSY0_66_PM2_TRIG_LOCK	STATUS

15 Link Node 24

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	1	1	KICK:LTU1:320:BYKIK	BYKIK	STATUS
□	1	2	KICK:LTU1:320:BYKIKRB	BYKIK_READBACK	STATUS
□	7	1	KICK:LTU0:320:TA120MISS	BYKIK_120HZ_ABRT_TRIG	MISSED
□	7	2	KICK:LTU0:320:TS120MISS	BYKIK_120HZ_STBY_TRIG	MISSED
□	7	3	KICK:LTU0:320:TA30MISS	BYKIK_30HZ_ABRT_TRIG	MISSED
□	7	4	KICK:LTU0:320:TS30MISS	BYKIK_30HZ_STBY_TRIG	MISSED
□	7	6	KICK:LTU0:320:THRSHUNDR	BYKIK_THRESHOLD_UNDER	FAULT
□	7	7	KICK:LTU0:320:THRSHOVER	BYKIK_THRESHOLD_OVER	FAULT
□	7	14	KICK:LTU0:320:ABORTWIN	KICK_LTU0_320_ABORTWIN	FAULT
□	7	15	KICK:LTU0:320:STANDBYWIN	KICK_LTU0_320_STANDBYWIN	FAULT

16 Link Node 25

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	1	6	VGFS:BSY0:2:FSG1_OK	FSG1_VAC_OK	STATE
□	1	7	VGFS:BSY0:2:FSG12_OK	FSG12_VAC_OK	STATE
□	1	8	VGFS:BSY0:2:FSG3_OK	FSG3_VAC_OK	STATE
□	1	9	VGFS:BSY0:2:FSG10_OK	FSG10_VAC_OK	STATE
□	1	10	WATR:BSY0:3:HTEXCH2_FS	HTEXCH2	STATE
□	1	11	WATR:BSY0:3:HX1RCBNR	HYDRECM1	STATE
□	1	12	WATR:BSY0:3:HX2RCBNR	HYDRECM2	STATE
□	2	2	MISC:MCC0:1:EMG_RAD_STOP	EMG_RAD_STOP	STATE
□	2	5	PPS:MCC0:1:BATTP24OVER	PPS_MCC0_1_BATTP24OVER	STATE
□	2	6	PPS:MCC0:1:BATTP24UNDER	PPS_MCC0_1_BATTP24UNDER	STATE
□	2	7	PPS:MCC0:1:BATTN24OVER	PPS_MCC0_1_BATTN24OVER	STATE
□	2	8	PPS:MCC0:1:BATTN24UNDER	PPS_MCC0_1_BATTN24UNDER	STATE
□	2	9	CHAS:MCC0:2:BTM_GAS	CHAS_MCC0_2_BTM_GAS	STATE
□	2	10	CHAS:MCC0:2:BAS2_BTM	CHAS_MCC0_2_BAS2_BTM	STATE
□	2	11	CHAS:MCC0:2:TEMP_SUM	CHAS_MCC0_2_TEMP_SUM	STATE
□	2	12	CHAS:MCC0:2:EPVTANK	CHAS_MCC0_2_EPVTANK	STATE
□	2	13	CHAS:MCC0:2:CCR_BAT	CHAS_MCC0_2_CCR_BAT	STATE
□	3	2	CHAS:MCC0:1:LNW_BSO	CHAS_MCC0_1_LNW_BSO	STATE
□	3	3	CHAS:MCC0:1:PPS30MCC	CHAS_MCC0_1_PPS30MCC	STATE
□	3	4	CHAS:MCC0:1:PPS_2_20	CHAS_MCC0_1_PPS_2_20	STATE
□	3	5	CHAS:MCC0:1:PPS_UND	CHAS_MCC0_1_PPS_UND	STATE
□	3	6	CHAS:MCC0:1:PPS_WE	CHAS_MCC0_1_PPS_WE	STATE
□	3	7	CHAS:MCC0:1:PPS_S2_S29	CHAS_MCC0_1_PPS_S2_S29	STATE
□	3	8	CHAS:MCC0:1:WE_BSOIC	CHAS_MCC0_1_WE_BSOIC	STATE
□	3	9	CHAS:MCC0:1:EE_BSOIC	CHAS_MCC0_1_EE_BSOIC	STATE
□	3	11	CHAS:MCC0:1:LCLSS20BSOIC	CHAS_MCC0_1_LCLSBSOIC	STATE
□	3	12	CHAS:MCC0:1:UNDBSOIC	CHAS_MCC0_1_UNDBSOIC	STATE
□	3	13	CHAS:MCC0:2:BSOIC_ANLG	CHAS_MCC0_2_BSOIC_ANLG	STATE
□	3	14	CHAS:MCC0:2:VAX_TEMP	CHAS_MCC0_2_VAX_TEMP	STATE
□	3	15	CHAS:MCC0:2:SITE_AIR	CHAS_MCC0_2_SITE_AIR	STATE
□	3	16	CHAS:MCC0:2:STPR409_TEMP	CHAS_MCC0_2_STPR409_TEMP	STATE
□	4	2	CHAS:MCC0:1:VDPS_TEMP	CHAS_MCC0_1_VDPS_TEMP	STATE
□	4	3	CHAS:MCC0:1:DR_LCW	CHAS_MCC0_1_DR_LCW	STATE
□	4	5	CHAS:MCC0:1:MCC_PLIC	CHAS_MCC0_1_MCC_PLIC	STATE
□	4	6	CHAS:MCC0:1:MCC_BAT	CHAS_MCC0_1_MCC_BAT	STATE
□	4	9	CHAS:MCC0:1:1200_LEVEL	CHAS_MCC0_1_1200_LEVEL	STATE
□	4	10	CHAS:MCC0:1:1200_PUMP	CHAS_MCC0_1_1200_PUMP	STATE
□	4	11	CHAS:MCC0:1:1201_PUMP	CHAS_MCC0_1_1201_PUMP	STATE

continued on next page...

. . . continued from previous page

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	4	12	CHAS:MCC0:1:1202_PUMP	CHAS_MCC0_1_1202_PUMP	STATE
□	4	15	CHAS:MCC0:1:BDERCBNR	CHAS_MCC0_1_BDERCBNR	STATE
□	5	1	PROF:BSYA:1:OUT_SUM	PROF_BSYA_1_OUT_SUM	STATE
□	5	2	BEND:BSYA:140:B1_2_PS_ON	BEND_BSYA_140_B1_2_PS_ON	STATE
□	5	3	COLL:BSYA:1015:FLOW_SW	COLL_BSYA_1015_FLOW_SW	STATE
□	5	4	VVFS:BSYA:1030:POSITION	VVFS_BSYA_1030_POSITION	STATE
□	5	5	VVPG:BSYA:1018:POSITION	VVPG_BSYA_1018_POSITION	STATE
□	5	6	BEND:BSYA:1100:B11_PS_ON	BEND_BSYA_1100_B11_PS_ON	STATE
□	5	7	BPM:BSYA:1020:FLOW_SW	BPM_BSYA_1020_FLOW_SW	STATE
□	5	8	QUAD:BSYA:1010:Q10_PS_ON	QUAD_BSYA_1010_Q10_PS_ON	STATE
□	5	9	QUAD:BSYA:1090:Q11_PS_ON	QUAD_BSYA_1090_Q11_PS_ON	STATE
□	5	10	BPM:BSYA:1240:FLOW_SW	BPM_BSYA_1240_FLOW_SW	STATE
□	5	11	COLL:BSYA:1230:FLOW_SW	COLL_BSYA_1230_FLOW_SW	STATE
□	5	12	VVPG:BSYA:2635:POSITION	VVPG_BSYA_2635_POSITION	STATE
□	5	13	VVFS:BSYA:2855:POSITION	VVFS_BSYA_2855_POSITION	STATE
□	5	14	VVPG:BSYA:4005:POSITION	VVPG_BSYA_4005_POSITION	STATE
□	5	15	STPR:BSY0:88:IN_LIMIT	STPR_BSY0_88_IN_LIMIT	POSITION
□	5	16	STPR:BSY0:88:OUT_LIMIT	STPR_BSY0_88_OUT_LIMIT	POSITION
□	6	1	PICM:BSY0:1:HV_PWR	PICM_BSY0_1_HV_PWR	STATE
□	6	2	PICM:BSY0:2:HV_PWR	PICM_BSY0_2_HV_PWR	STATE
□	6	3	PICM:BSY0:3:HV_PWR	PICM_BSY0_3_HV_PWR	STATE
□	6	4	PICM:BSY0:4:HV_PWR	PICM_BSY0_4_HV_PWR	STATE
□	6	5	PICM:BSY0:5:HV_PWR	PICM_BSY0_5_HV_PWR	STATE
□	6	6	PICM:BSY0:6:HV_PWR	PICM_BSY0_6_HV_PWR	STATE
□	6	7	BEND:BSYA:140:PS_OFF_A	BEND_BSYA_140_PS_OFF_A	STATE
□	6	8	BEND:BSYA:140:PS_OFF_B	BEND_BSYA_140_PS_OFF_B	STATE
□	6	10	TRGT:BSYA:964:OUT_LIMSW	TRGT_BSYA_964_OUT_LIMSW	POSITION
□	6	11	TRGT:BSYA:964:IN_LIMSW	TRGT_BSYA_964_IN_LIMSW	POSITION
□	7	8	PICM:BSY0:16:NO_TRIG	PICM_BSY0_16_NO_TRIG	MISSED
□	9	1	PICM:BSYH:479:LOSSL	PICM_BSYH_479_LOSSL	THRESHOLD
□	9	2	PICM:BSYH:479:LOSSH	PICM_BSYH_479_LOSSH	THRESHOLD
□	10	1	PICM:BSYH:487:LOSSL	PICM_BSYH_487_LOSSL	THRESHOLD
□	10	2	PICM:BSYH:487:LOSSH	PICM_BSYH_487_LOSSH	THRESHOLD
□	11	1	PICM:BSYH:495:LOSSL	PICM_BSYH_495_LOSSL	THRESHOLD
□	11	2	PICM:BSYH:495:LOSSH	PICM_BSYH_495_LOSSH	THRESHOLD
□	12	1	PICM:BSYH:836:LOSSL	PICM_BSYH_836_LOSSL	THRESHOLD
□	12	2	PICM:BSYH:836:LOSSH	PICM_BSYH_836_LOSSH	THRESHOLD
□	13	1	PICM:BSYH:503:LOSSL	PICM_BSYH_503_LOSSL	THRESHOLD
□	13	2	PICM:BSYH:503:LOSSH	PICM_BSYH_503_LOSSH	THRESHOLD
□	22	1	PICM:BSYA:1016:LOSSL	PICM_BSYA_1016_LOSSL	THRESHOLD
□	22	2	PICM:BSYA:1016:LOSSH	PICM_BSYA_1016_LOSSH	THRESHOLD

continued on next page. . .

. . . continued from previous page

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	23	1	PICM:BSYA:1021:LOSSL	PICM_BSYA_1021_LOSSL	THRESHOLD
□	23	2	PICM:BSYA:1021:LOSSH	PICM_BSYA_1021_LOSSH	THRESHOLD
□	24	1	PICM:BSYA:1120:LOSSL	PICM_BSYA_1120_LOSSL	THRESHOLD
□	24	2	PICM:BSYA:1120:LOSSH	PICM_BSYA_1120_LOSSH	THRESHOLD
□	25	1	PICM:BSYA:1320:LOSSL	PICM_BSYA_1320_LOSSL	THRESHOLD
□	25	2	PICM:BSYA:1320:LOSSH	PICM_BSYA_1320_LOSSH	THRESHOLD
□	26	1	PICM:BSYA:1520:LOSSL	PICM_BSYA_1520_LOSSL	THRESHOLD
□	26	2	PICM:BSYA:1520:LOSSH	PICM_BSYA_1520_LOSSH	THRESHOLD
□	27	1	PICM:BSYA:1980:LOSSL	PICM_BSYA_1980_LOSSL	THRESHOLD
□	27	2	PICM:BSYA:1980:LOSSH	PICM_BSYA_1980_LOSSH	THRESHOLD
□	28	1	PICM:BSYA:1701A:LOSSL	PICM_BSYA_1701A_LOSSL	THRESHOLD
□	28	2	PICM:BSYA:1701A:LOSSH	PICM_BSYA_1701A_LOSSH	THRESHOLD
□	29	1	PICM:BSYA:1701B:LOSSL	PICM_BSYA_1701B_LOSSL	THRESHOLD
□	29	2	PICM:BSYA:1701B:LOSSH	PICM_BSYA_1701B_LOSSH	THRESHOLD
□	30	1	PICM:BSYH:762:LOSSL	PICM_BSYH_762_LOSSL	THRESHOLD
□	30	2	PICM:BSYH:762:LOSSH	PICM_BSYH_762_LOSSH	THRESHOLD

17 Link Node 27

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	1	1	SPLR:LTU1:359:FLOW_SW	SPOILER_FS	STATE
□	1	2	DUMP:LTU1:360:FLOW_SW	TDKIK_FS	STATE
□	1	4	VVPG:CLTH:178:OPEN_LIMSW	VVPG_CLTH_178_OPEN_LIMSW	POSITION
□	1	5	VVPG:CLTH:375:OPEN_LIMSW	VVPG_CLTH_375_OPEN_LIMSW	POSITION
□	1	6	VVPG:BSYH:470:OPEN_LIMSW	VVPG_BSYH_470_OPEN_LIMSW	POSITION
□	1	7	VVPG:BSYH:541:OPEN_LIMSW	VVPG_BSYH_541_OPEN_LIMSW	POSITION
□	1	8	VVPG:LTU0:100:POSITION	VACV_LTU1_100	STATE
□	1	9	VVPG:LTU1:265:POSITION	VACV_LTU1_265	STATE
□	1	10	VVMG:LTU0:174:POSITION	VACV_LTU1_174	STATE
□	1	11	VVMG:LTU1:355:POSITION	VACV_LTU1_355	STATE
□	1	12	VVFS:LTU0:102:OPENSTATUS	VACFS_LTU1_102	STATE
□	1	13	VVPG:BSYA:340:OPEN_LIMSW	VVPG_BSYA_340_OPEN_LIMSW	POSITION
□	1	14	IOC:LTU1:BP01:BEAMKICKED	IOC_LTU1_BP01_BEAMKICKED	STATE
□	1	15	VVFS:CLTH:101:OPEN_LIMSW	VVFS_CLTH_101_OPEN_LIMSW	POSITION
□	1	16	VVPG:BSYH:837:OPEN_LIMSW	VVPG_BSYH_837_OPEN_LIMSW	POSITION

18 Link Node 28

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	1	1	TORO:LTU1:195:IM31_IM36_L1	TORO_LTU1_195_IM31_IM36_L1	STATE
□	1	2	TORO:LTU1:196:IM31_IM36_L2	TORO_LTU1_196_IM31_IM36_L2	STATE
□	1	3	TORO:LTU1:195:CHASIM31_36	TORO_LTU1_195_CHASIM31_36	STATE
□	1	4	COLL:LTU1:252:FLOW_SW	COLL_LTU1_252_FLOW_SW	STATE
□	1	5	COLL:LTU1:452:FLOW_SW	COLL_LTU1_452_FLOW_SW	STATE
□	1	6	OTRS:LTU1:449:OUT_LMTSW	OTRS_LTU1_449_OUT_LMTSW	STATE
□	1	7	OTRS:LTU1:449:IN_LMTSW	OTRS_LTU1_449_IN_LMTSW	STATE
□	1	8	MIRR:LTU1:548:OUT_LIMSW	MIRR_LTU1_548_OUT_LIMSW	POSITION
□	1	9	MIRR:LTU1:548:IN_LIMSW	MIRR_LTU1_548_IN_LIMSW	POSITION
□	1	10	PICM:LTU1:B911:HV_PWR	PICM_LTU1_B911_HV_PWR	STATE
□	1	11	COLL:LTU1:252:STATE_OUT	COLL_LTU1_252_STATE_OUT	STATE
□	1	12	COLL:LTU1:452:STATE_OUT	COLL_LTU1_452_STATE_OUT	STATE
□	1	14	COLL:LTU1:732:STATE_OUT	COLL_LTU1_732_STATE_OUT	STATE
□	1	15	COLL:LTU1:722:STATE_OUT	COLL_LTU1_722_STATE_OUT	STATE
□	2	1	DCHP:LTU1:555:OUT_LIMSW_NEGX	DCHP_LTU1_555_OUT_LIMSW_NEGX	POSITION
□	2	2	DCHP:LTU1:555:OUT_LIMSW_POSX	DCHP_LTU1_555_OUT_LIMSW_POSX	POSITION
□	2	3	DCHP:LTU1:545:OUT_LIMSW_NEGY	DCHP_LTU1_545_OUT_LIMSW_NEGY	POSITION
□	2	4	DCHP:LTU1:545:OUT_LIMSW_POSY	DCHP_LTU1_545_OUT_LIMSW_POSY	POSITION
□	2	5	DCHP:LTU1:555:GAP_LIMSW_NEGZ	DCHP_LTU1_555_GAP_LIMSW_NEGZ	POSITION
□	2	6	DCHP:LTU1:555:GAP_LIMSW_POSZ	DCHP_LTU1_555_GAP_LIMSW_POSZ	POSITION
□	2	7	DCHP:LTU1:545:GAP_LIMSW_NEGZ	DCHP_LTU1_545_GAP_LIMSW_NEGZ	POSITION
□	2	8	DCHP:LTU1:545:GAP_LIMSW_POSZ	DCHP_LTU1_545_GAP_LIMSW_POSZ	POSITION
□	7	8	PICM:LTU1:220:NO_TRIG	PICS_LTU1_220_NO_TRIG	MISSED
□	9	1	PICM:LTU1:220:LOSSL	PICS_LTU1_220_LOSSL	THRESHOLD
□	9	2	PICM:LTU1:220:LOSSH	PICS_LTU1_220_LOSSH	THRESHOLD
□	10	1	PICM:LTU1:252:LOSSL	PICS_LTU1_252_LOSSL	THRESHOLD
□	10	2	PICM:LTU1:252:LOSSH	PICS_LTU1_252_LOSSH	THRESHOLD
□	11	1	PICM:LTU1:280:LOSSL	PICS_LTU1_280_LOSSL	THRESHOLD
□	11	2	PICM:LTU1:280:LOSSH	PICS_LTU1_280_LOSSH	THRESHOLD
□	12	1	PICM:LTU1:420:LOSSL	PICS_LTU1_420_LOSSL	THRESHOLD
□	12	2	PICM:LTU1:420:LOSSH	PICS_LTU1_420_LOSSH	THRESHOLD
□	13	1	PICM:LTU1:450:LOSSL	PICS_LTU1_450_LOSSL	THRESHOLD
□	13	2	PICM:LTU1:450:LOSSH	PICS_LTU1_450_LOSSH	THRESHOLD

19 Link Node 29

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	1	1	YAGS:LTU1:743:OUT_LIMIT	YAGS_LTU1_743_OUT_LIMIT	POSITION
□	1	2	PICM:LTU1:B912:HV_PWR	PICM_LTU1_B912_HV_PWR	STATE
□	1	3	VVMG:LTU1:505:POSITION	VVPG_0505	STATE
□	1	4	COLL:LTU1:722:FLOW_SW	CX31_FS	STATE
□	1	5	COLL:LTU1:732:FLOW_SW	CX32_FS	STATE
□	1	6	OTRS:LTU1:745:OUT_LMTSW	OTR33_0745_OUT	STATE
□	1	7	OTRS:LTU1:745:IN_LMTSW	OTR33_0745_IN	STATE
□	1	8	VVPG:LTU1:435:POSITION	VVPG_0435	STATE
□	1	9	VVPG:LTU1:580:POSITION	VVPG_0580	STATE
□	1	10	VVPG:LTU1:725:POSITION	VVPG_0725	STATE
□	1	11	VVPG:LTU1:757:POSITION	VVPG_0757	STATE
□	1	12	VVPG:LTU1:999:POSITION	VVPG_0999	STATE
□	1	13	YAGS:LTU1:743:IN_LIMIT	YAGS_LTU1_743_IN_LIMIT	POSITION
□	1	14	VVMG:LTU1:670:POSITION	VVPG_0670	STATE
□	1	15	VVMG:LTU1:742:POSITION	VVPG_0742	STATE
□	1	16	VVMG:LTU1:774:POSITION	VVPG_0774	STATE
□	7	8	PICM:LTU1:480:NO_TRIG	PICS_LTU1_480_NO_TRIG	MISSED
□	9	1	PICM:LTU1:722:LOSSL	PICS_LTU1_722_LOSSL	THRESHOLD
□	9	2	PICM:LTU1:722:LOSSH	PICS_LTU1_722_LOSSH	THRESHOLD
□	10	1	PICM:LTU1:732:LOSSL	PICM_LTU1_732_LOSSL	THRESHOLD
□	10	2	PICM:LTU1:732:LOSSH	PICM_LTU1_732_LOSSH	THRESHOLD
□	11	1	PICM:LTU1:480:LOSSL	PICS_LTU1_480_LOSSL	THRESHOLD
□	11	2	PICM:LTU1:480:LOSSH	PICS_LTU1_480_LOSSH	THRESHOLD

20 Link Node 30

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	7	8	BLM:LTU1:722:NO_TRIG	BLM_LTU1_722_NO_TRIG	MISSED
□	9	1	BLM:LTU1:722:LOSS_L	BLM_LTU1_722_LOSS_L	THRESHOLD
□	9	2	BLM:LTU1:722:LOSS_H	BLM_LTU1_722_LOSS_H	THRESHOLD
□	9	11	BLM:LTU1:722:TIMING_L	BLM_LTU1_722_TEST_L	THRESHOLD
□	9	12	BLM:LTU1:722:TIMING_H	BLM_LTU1_722_TEST_H	THRESHOLD
□	9	15	BLM:LTU1:722:PED_L	BLM_LTU1_722_PED_L	THRESHOLD
□	9	16	BLM:LTU1:722:PED_H	BLM_LTU1_722_PED_H	THRESHOLD
□	10	1	BLM:LTU1:732:LOSS_L	BLM_LTU1_732_LOSS_L	THRESHOLD
□	10	2	BLM:LTU1:732:LOSS_H	BLM_LTU1_732_LOSS_H	THRESHOLD
□	10	11	BLM:LTU1:732:TEST_L	BLM_LTU1_732_TEST_L	THRESHOLD
□	10	12	BLM:LTU1:732:TEST_H	BLM_LTU1_732_TEST_H	THRESHOLD
□	10	15	BLM:LTU1:732:PED_L	BLM_LTU1_732_PED_L	THRESHOLD
□	10	16	BLM:LTU1:732:PED_H	BLM_LTU1_732_PED_H	THRESHOLD
□	11	1	BLM:LTU1:BLF545:LOSS_L	BLM_LTU1_BLF545_LOSS_L	THRESHOLD
□	11	2	BLM:LTU1:BLF545:LOSS_H	BLM_LTU1_BLF545_LOSS_H	THRESHOLD
□	11	11	BLM:LTU1:BLF545:TEST_L	BLM_LTU1_BLF545_TEST_L	THRESHOLD
□	11	12	BLM:LTU1:BLF545:TEST_H	BLM_LTU1_BLF545_TEST_H	THRESHOLD
□	11	15	BLM:LTU1:BLF545:PED_L	BLM_LTU1_BLF545_PED_L	THRESHOLD
□	11	16	BLM:LTU1:BLF545:PED_H	BLM_LTU1_BLF545_PED_H	THRESHOLD
□	12	1	BLM:LTU1:BLF859:LOSS_L	BLM_LTU1_BLF859_LOSS_L	THRESHOLD
□	12	2	BLM:LTU1:BLF859:LOSS_H	BLM_LTU1_BLF859_LOSS_H	THRESHOLD
□	12	11	BLM:LTU1:BLF859:TEST_L	BLM_LTU1_BLF859_TEST_L	THRESHOLD
□	12	12	BLM:LTU1:BLF859:TEST_H	BLM_LTU1_BLF859_TEST_H	THRESHOLD
□	12	15	BLM:LTU1:BLF859:PED_L	BLM_LTU1_BLF859_PED_L	THRESHOLD
□	12	16	BLM:LTU1:BLF859:PED_H	BLM_LTU1_BLF859_PED_H	THRESHOLD
□	13	1	BLM:UND1:121:LOSS_L	BLM_UND1_121_LOSS_L	THRESHOLD
□	13	2	BLM:UND1:121:LOSS_H	BLM_UND1_121_LOSS_H	THRESHOLD
□	13	11	BLM:UND1:121:TEST_L	BLM_UND1_121_TEST_L	THRESHOLD
□	13	12	BLM:UND1:121:TEST_H	BLM_UND1_121_TEST_H	THRESHOLD
□	13	15	BLM:UND1:121:PED_L	BLM_UND1_121_PED_L	THRESHOLD
□	13	16	BLM:UND1:121:PED_H	BLM_UND1_121_PED_H	THRESHOLD
□	14	1	BLM:UND1:921:LOSS_L	BLM_UND1_921_LOSS_L	THRESHOLD
□	14	2	BLM:UND1:921:LOSS_H	BLM_UND1_921_LOSS_H	THRESHOLD
□	14	11	BLM:UND1:921:TEST_L	BLM_UND1_921_TEST_L	THRESHOLD
□	14	12	BLM:UND1:921:TEST_H	BLM_UND1_921_TEST_H	THRESHOLD
□	14	15	BLM:UND1:921:PED_L	BLM_UND1_921_PED_L	THRESHOLD
□	14	16	BLM:UND1:921:PED_H	BLM_UND1_921_PED_H	THRESHOLD
□	15	1	BLM:UND1:BLF1:LOSS_L	BLM_UND1_BLF1_LOSS_L	THRESHOLD

continued on next page...

. . . continued from previous page

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	15	2	BLM:UND1:BLF1:LOSS_H	BLM_UND1_BLF1_LOSS_H	THRESHOLD
□	15	11	BLM:UND1:BLF1:TEST_L	BLM_UND1_BLF1_TEST_L	THRESHOLD
□	15	12	BLM:UND1:BLF1:TEST_H	BLM_UND1_BLF1_TEST_H	THRESHOLD
□	15	15	BLM:UND1:BLF1:PED_L	BLM_UND1_BLF1_PED_L	THRESHOLD
□	15	16	BLM:UND1:BLF1:PED_H	BLM_UND1_BLF1_PED_H	THRESHOLD
□	16	1	BLM:UND1:BLF17:LOSS_L	BLM_UND1_BLF17_LOSS_L	THRESHOLD
□	16	2	BLM:UND1:BLF17:LOSS_H	BLM_UND1_BLF17_LOSS_H	THRESHOLD
□	16	11	BLM:UND1:BLF17:TEST_L	BLM_UND1_BLF17_TEST_L	THRESHOLD
□	16	12	BLM:UND1:BLF17:TEST_H	BLM_UND1_BLF17_TEST_H	THRESHOLD
□	16	15	BLM:UND1:BLF17:PED_L	BLM_UND1_BLF17_PED_L	THRESHOLD
□	16	16	BLM:UND1:BLF17:PED_H	BLM_UND1_BLF17_PED_H	THRESHOLD
□	17	1	HVPS:LTU1:722:LOW	HVPS_LTU1_722_LOW	FAULT
□	17	2	HVPS:LTU1:722:HIGH	HVPS_LTU1_722_HIGH	FAULT
□	17	3	HVPS:LTU1:732:LOW	HVPS_LTU1_732_LOW	FAULT
□	17	4	HVPS:LTU1:732:HIGH	HVPS_LTU1_732_HIGH	FAULT
□	17	5	HVPS:LTU1:SP1:LOW	HVPS_LTU1_SP1_LOW	FAULT
□	17	6	HVPS:LTU1:SP1:HIGH	HVPS_LTU1_SP1_HIGH	FAULT
□	17	7	HVPS:LTU1:SP2:LOW	HVPS_LTU1_SP2_LOW	FAULT
□	17	8	HVPS:LTU1:SP2:HIGH	HVPS_LTU1_SP2_HIGH	FAULT
□	17	9	HVPS:UND1:121:LOW	HVPS_UND1_121_LOW	FAULT
□	17	10	HVPS:UND1:121:HIGH	HVPS_UND1_121_HIGH	FAULT
□	17	11	HVPS:UND1:921:LOW	HVPS_UND1_921_LOW	FAULT
□	17	12	HVPS:UND1:921:HIGH	HVPS_UND1_921_HIGH	FAULT
□	17	13	HVPS:UND1:BLF1:LOW	HVPS_UND1_BLF1_LOW	FAULT
□	17	14	HVPS:UND1:BLF1:HIGH	HVPS_UND1_BLF1_HIGH	FAULT
□	17	15	HVPS:UND1:BLF17:LOW	HVPS_UND1_BLF17_LOW	FAULT
□	17	16	HVPS:UND1:BLF17:HIGH	HVPS_UND1_BLF17_HIGH	FAULT

21 Link Node 31

Verified	Card	Channel	PV Prefix	Device Name	Fault Nam
□	1	1	THZR:LTU1:741:OUT_LIMSW	THZR_LTU1_741_OUT_LIMSW	POSITION
□	1	2	COLL:LTU1:762:FLOW_SW	CX35_FS	STATE
□	1	3	COLL:LTU1:772:FLOW_SW	CY36_FS	STATE
□	1	6	DUMP:LTU1:970:TDUND_OUT	DUMP_LTU1_970_TDUND_OUT	POSITION
□	1	7	DUMP:LTU1:970:TDUND_IN	DUMP_LTU1_970_TDUND_IN	POSITION
□	1	8	VVPG:UND1:1000:POSITION	VACV_LTU0_1000_OPEN	STATE
□	1	9	THZR:LTU1:741:IN_LIMSW	THZR_LTU1_741_IN_LIMSW	POSITION
□	1	10	PICM:LTU1:B913:HV_PWR	PICM_LTU1_B913_HV_PWR	STATE
□	1	11	IOC:UND1:BP01:MPSSTAT	IOC_UND1_BP01_MPSSTAT	STATE
□	1	12	IOC:UND1:BP02:MPSSTAT	IOC_UND1_BP02_MPSSTAT	STATE
□	1	14	COLL:LTU1:772:STATE_OUT	COLL_CY36	STATE
□	1	15	COLL:LTU1:762:STATE_OUT	COLL_CX35	STATE
□	2	1	VVMG:UND1:1645:OPEN_LMTSW	VVMG_UND1_1645_OPEN_LMTSW	STATE
□	2	2	VVMG:UND1:1655:OPEN_LMTSW	VVMG_UND1_1655_OPEN_LMTSW	STATE
□	2	3	BMLN:UND1:1650:IN_LMTSW	BMLN_UND1_1650_IN_LMTSW	STATE
□	2	4	BMLN:UND1:1650:OUT_LMTSW	BMLN_UND1_1650_OUT_LMTSW	STATE
□	2	5	MIRR:LTU1:829:APERTURE_3MM	MIRR_LTU1_829_APERTURE_3MM	POSITION
□	2	6	XTAL:UND1:1650:OUT_LMTSW	XTAL_UND1_1650_OUT_LMTSW	STATE
□	2	7	BEND:UND1:1640:OFF	BEND_UND1_1640_OFF	STATE
□	2	8	BEND:UND1:1640:ON	BEND_UND1_1640_ON	STATE
□	2	9	XTAL:UND1:1651:OUT_LMTSW	XTAL_UND1_1651_OUT_LMTSW	STATE
□	2	10	XTAL:UND1:1652:OUT_LMTSW	XTAL_UND1_1652_OUT_LMTSW	STATE
□	2	11	SPLR:DMP1:765:IN_LIMSW	SPLR_DMP1_765_IN_LIMSW	POSITION
□	2	12	SPLR:DMP1:765:OUT_LIMSW	SPLR_DMP1_765_OUT_LIMSW	POSITION
□	2	13	MIRR:LTU1:829:OUT_LIMSW	MIRR_LTU1_829_OUT_LIMSW	POSITION
□	2	14	MIRR:LTU1:829:APERTURE_5MM	MIRR_LTU1_829_APERTURE_5MM	POSITION
□	2	15	YAGS:LTU1:844:OUT_LIMSW	YAGS_LTU1_844_OUT_LIMSW	POSITION
□	2	16	YAGS:LTU1:844:IN_LIMSW	YAGS_LTU1_844_IN_LIMSW	POSITION
□	3	1	GRAT:UND1:934:IN_LIMIT	GRAT_UND1_934_IN_LIMIT	POSITION
□	3	2	GRAT:UND1:934:OUT_LIMIT	GRAT_UND1_934_OUT_LIMIT	POSITION
□	3	3	MIRR:UND1:964:IN_LIMIT	MIRR_UND1_964_IN_LIMIT	POSITION
□	3	4	MIRR:UND1:964:OUT_LIMIT	MIRR_UND1_964_OUT_LIMIT	POSITION
□	3	5	MIRR:UND1:966:IN_LIMIT	MIRR_UND1_966_IN_LIMIT	POSITION
□	3	6	MIRR:UND1:966:OUT_LIMIT	MIRR_UND1_966_OUT_LIMIT	POSITION
□	3	7	SLIT:UND1:962:IN_LIMIT	SLIT_UND1_962_IN_LIMIT	POSITION
□	3	8	SLIT:UND1:962:OUT_LIMIT	SLIT_UND1_962_OUT_LIMIT	POSITION
□	3	9	BEND:UND1:940:ON	BEND_UND1_940_ON	STATE
□	3	10	BOD:UND1:1005:IN_LIMIT	BOD_UND1_1005_IN_LIMIT	POSITION

continued on next page. . .

. . . continued from previous page

Verified	Card	Channel	PV Prefix	Device Name	Fault Nam
□	3	11	BOD:UND1:1005:OUT_LIMIT	BOD_UND1_1005_OUT_LIMIT	POSITION
□	3	12	BOD:UND1:1305:IN_LIMIT	BOD_UND1_1305_IN_LIMIT	POSITION
□	3	13	BOD:UND1:1305:OUT_LIMIT	BOD_UND1_1305_OUT_LIMIT	POSITION
□	3	14	VVMG:UND1:932:OUT_LIMIT	VVMG_UND1_932_OUT_LIMIT	POSITION
□	3	15	VVMG:UND1:968:OUT_LIMIT	VVMG_UND1_968_OUT_LIMIT	POSITION
□	4	1	WIGG:LTU1:849:GAP_LIMSW_POSZ_TOP	WIGG_LTU1_849_GAP_LIMSW_POSZ_TOP	POSITION
□	4	2	WIGG:LTU1:849:GAP_LIMSW_POSZ_BOT	WIGG_LTU1_849_GAP_LIMSW_POSZ_BOT	POSITION
□	4	3	WIGG:LTU1:849:GAP_LIMSW_NEGZ_TOP	WIGG_LTU1_849_GAP_LIMSW_NEGZ_TOP	POSITION
□	4	4	WIGG:LTU1:849:GAP_LIMSW_NEGZ_BOT	WIGG_LTU1_849_GAP_LIMSW_NEGZ_BOT	POSITION
□	7	8	PICM:LTU1:762:NO_TRIG	PICS_LTU1_762_NO_TRIG	MISSED
□	9	1	PICM:LTU1:762:LOSSL	PICS_LTU1_762_LOSSL	THRESHOLD
□	9	2	PICM:LTU1:762:LOSSH	PICS_LTU1_762_LOSSH	THRESHOLD
□	10	1	PICM:LTU1:772:LOSSL	PICS_LTU1_772_LOSSL	THRESHOLD
□	10	2	PICM:LTU1:772:LOSSH	PICS_LTU1_772_LOSSH	THRESHOLD

22 Link Node 32

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	1	1	BFW:UND1:110:OUT	BFW_UND1_110_OUT	STATE
□	1	3	BFW:UND1:210:OUT	BFW_UND1_210_OUT	STATE
□	1	4	BFW:UND1:310:OUT	BFW_UND1_310_OUT	STATE
□	1	5	BFW:UND1:410:OUT	BFW_UND1_410_OUT	STATE
□	1	6	BFW:UND1:510:OUT	BFW_UND1_510_OUT	STATE
□	1	7	BFW:UND1:110:IN	BFW_UND1_110_IN	STATE
□	1	8	BFW:UND1:210:IN	BFW_UND1_210_IN	STATE
□	1	9	BFW:UND1:310:IN	BFW_UND1_310_IN	STATE
□	1	10	BFW:UND1:410:IN	BFW_UND1_410_IN	STATE
□	1	11	BFW:UND1:510:IN	BFW_UND1_510_IN	STATE
□	1	12	BFW:UND1:1010:IN	BFW_UND1_1010_IN	STATE
□	1	13	YAGS:LTU1:853:OUT_LIMSW	YAGS_LTU1_853_OUT_LIMSW	POSITION
□	1	14	YAGS:LTU1:853:IN_LIMSW	YAGS_LTU1_853_IN_LIMSW	POSITION
□	1	15	OTRS:LTU1:858:OUT_LIMSW	OTRS_LTU1_858_OUT_LIMSW	POSITION
□	1	16	OTRS:LTU1:858:IN_LIMSW	OTRS_LTU1_858_IN_LIMSW	POSITION
□	7	8	BLM:LTU1:762:NO_TRIG	BLM_LTU1_762_NO_TRIG	MISSED
□	9	1	BLM:LTU1:762:LOSS_L	BLM_LTU1_762_LOSS_L	THRESHOLD
□	9	2	BLM:LTU1:762:LOSS_H	BLM_LTU1_762_LOSS_H	THRESHOLD
□	9	11	BLM:LTU1:762:TIMING_L	BLM_LTU1_762_TEST_L	THRESHOLD
□	9	12	BLM:LTU1:762:TIMING_H	BLM_LTU1_762_TEST_H	THRESHOLD
□	9	15	BLM:LTU1:762:PED_L	BLM_LTU1_762_PED_L	THRESHOLD
□	9	16	BLM:LTU1:762:PED_H	BLM_LTU1_762_PED_H	THRESHOLD
□	10	1	BLM:LTU1:772:LOSS_L	BLM_LTU1_772_LOSS_L	THRESHOLD
□	10	2	BLM:LTU1:772:LOSS_H	BLM_LTU1_772_LOSS_H	THRESHOLD
□	10	11	BLM:LTU1:772:TEST_L	BLM_LTU1_772_TEST_L	THRESHOLD
□	10	12	BLM:LTU1:772:TEST_H	BLM_LTU1_772_TEST_H	THRESHOLD
□	10	15	BLM:LTU1:772:PED_L	BLM_LTU1_772_PED_L	THRESHOLD
□	10	16	BLM:LTU1:772:PED_H	BLM_LTU1_772_PED_H	THRESHOLD
□	11	1	BLM:LTU1:980:LOSS_L	BLM_LTU1_980_LOSS_L	THRESHOLD
□	11	2	BLM:LTU1:980:LOSS_H	BLM_LTU1_980_LOSS_H	THRESHOLD
□	11	11	BLM:LTU1:980:TEST_L	BLM_LTU1_980_TEST_L	THRESHOLD
□	11	12	BLM:LTU1:980:TEST_H	BLM_LTU1_980_TEST_H	THRESHOLD
□	11	15	BLM:LTU1:980:PED_L	BLM_LTU1_980_PED_L	THRESHOLD
□	11	16	BLM:LTU1:980:PED_H	BLM_LTU1_980_PED_H	THRESHOLD
□	12	1	BLM:UND1:120:LOSS_L	BLM_UND1_120_LOSS_L	THRESHOLD
□	12	2	BLM:UND1:120:LOSS_H	BLM_UND1_120_LOSS_H	THRESHOLD
□	12	11	BLM:UND1:120:HRTBT_L	BLM_UND1_120_TEST_L	THRESHOLD
□	12	12	BLM:UND1:120:HRTBT_H	BLM_UND1_120_TEST_H	THRESHOLD

continued on next page. . .

. . . continued from previous page

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	12	15	BLM:UND1:120:PED_L	BLM_UND1_120_PED_L	THRESHOLD
□	12	16	BLM:UND1:120:PED_H	BLM_UND1_120_PED_H	THRESHOLD
□	13	1	BLM:UND1:221:LOSS_L	BLM_UND1_221_LOSS_L	THRESHOLD
□	13	2	BLM:UND1:221:LOSS_H	BLM_UND1_221_LOSS_H	THRESHOLD
□	13	11	BLM:UND1:221:TEST_L	BLM_UND1_221_TEST_L	THRESHOLD
□	13	12	BLM:UND1:221:TEST_H	BLM_UND1_221_TEST_H	THRESHOLD
□	13	15	BLM:UND1:221:PED_L	BLM_UND1_221_PED_L	THRESHOLD
□	13	16	BLM:UND1:221:PED_H	BLM_UND1_221_PED_H	THRESHOLD
□	14	1	BLM:UND1:321:LOSS_L	BLM_UND1_321_LOSS_L	THRESHOLD
□	14	2	BLM:UND1:321:LOSS_H	BLM_UND1_321_LOSS_H	THRESHOLD
□	14	11	BLM:UND1:321:TEST_L	BLM_UND1_321_TEST_L	THRESHOLD
□	14	12	BLM:UND1:321:TEST_H	BLM_UND1_321_TEST_H	THRESHOLD
□	14	15	BLM:UND1:321:PED_L	BLM_UND1_321_PED_L	THRESHOLD
□	14	16	BLM:UND1:321:PED_H	BLM_UND1_321_PED_H	THRESHOLD
□	15	1	BLM:UND1:421:LOSS_L	BLM_UND1_421_LOSS_L	THRESHOLD
□	15	2	BLM:UND1:421:LOSS_H	BLM_UND1_421_LOSS_H	THRESHOLD
□	15	11	BLM:UND1:421:TEST_L	BLM_UND1_421_TEST_L	THRESHOLD
□	15	12	BLM:UND1:421:TEST_H	BLM_UND1_421_TEST_H	THRESHOLD
□	15	15	BLM:UND1:421:PED_L	BLM_UND1_421_PED_L	THRESHOLD
□	15	16	BLM:UND1:421:PED_H	BLM_UND1_421_PED_H	THRESHOLD
□	16	1	BLM:UND1:521:LOSS_L	BLM_UND1_521_LOSS_L	THRESHOLD
□	16	2	BLM:UND1:521:LOSS_H	BLM_UND1_521_LOSS_H	THRESHOLD
□	16	11	BLM:UND1:521:TEST_L	BLM_UND1_521_TEST_L	THRESHOLD
□	16	12	BLM:UND1:521:TEST_H	BLM_UND1_521_TEST_H	THRESHOLD
□	16	15	BLM:UND1:521:PED_L	BLM_UND1_521_PED_L	THRESHOLD
□	16	16	BLM:UND1:521:PED_H	BLM_UND1_521_PED_H	THRESHOLD
□	17	1	HVPS:LTU1:762:LOW	HVPS_LTU1_762_LOW	FAULT
□	17	2	HVPS:LTU1:762:HIGH	HVPS_LTU1_762_HIGH	FAULT
□	17	3	HVPS:LTU1:772:LOW	HVPS_LTU1_772_LOW	FAULT
□	17	4	HVPS:LTU1:772:HIGH	HVPS_LTU1_772_HIGH	FAULT
□	17	5	HVPS:LTU1:980:LOW	HVPS_LTU1_980_LOW	FAULT
□	17	6	HVPS:LTU1:980:HIGH	HVPS_LTU1_980_HIGH	FAULT
□	17	7	HVPS:UND1:120:LOW	HVPS_UND1_120_LOW	FAULT
□	17	8	HVPS:UND1:120:HIGH	HVPS_UND1_120_HIGH	FAULT
□	17	9	HVPS:UND1:221:LOW	HVPS_UND1_221_LOW	FAULT
□	17	10	HVPS:UND1:221:HIGH	HVPS_UND1_221_HIGH	FAULT
□	17	11	HVPS:UND1:321:LOW	HVPS_UND1_321_LOW	FAULT
□	17	12	HVPS:UND1:321:HIGH	HVPS_UND1_321_HIGH	FAULT
□	17	13	HVPS:UND1:421:LOW	HVPS_UND1_421_LOW	FAULT
□	17	14	HVPS:UND1:421:HIGH	HVPS_UND1_421_HIGH	FAULT
□	17	15	HVPS:UND1:521:LOW	HVPS_UND1_521_LOW	FAULT

continued on next page. . .

. . . continued from previous page

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	17	16	HVPS:UND1:521:HIGH	HVPS_UND1_521_HIGH	FAULT

23 Link Node 33

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	1	1	BFW:UND1:610:OUT	BFW_UND1_610_OUT	STATE
□	1	2	BFW:UND1:710:OUT	BFW_UND1_710_OUT	STATE
□	1	3	BFW:UND1:810:OUT	BFW_UND1_810_OUT	STATE
□	1	4	BFW:UND1:910:OUT	BFW_UND1_910_OUT	STATE
□	1	5	BFW:UND1:1010:OUT	BFW_UND1_1010_OUT	STATE
□	1	6	BFW:UND1:1110:OUT	BFW_UND1_1110_OUT	STATE
□	1	7	BFW:UND1:1210:OUT	BFW_UND1_1210_OUT	STATE
□	1	8	BFW:UND1:1310:OUT	BFW_UND1_1310_OUT	STATE
□	1	9	BFW:UND1:610:IN	BFW_UND1_610_IN	STATE
□	1	10	BFW:UND1:710:IN	BFW_UND1_710_IN	STATE
□	1	11	BFW:UND1:810:IN	BFW_UND1_810_IN	STATE
□	1	12	BFW:UND1:910:IN	BFW_UND1_910_IN	STATE
□	1	14	BFW:UND1:1110:IN	BFW_UND1_1110_IN	STATE
□	1	15	BFW:UND1:1210:IN	BFW_UND1_1210_IN	STATE
□	1	16	BFW:UND1:1310:IN	BFW_UND1_1310_IN	STATE
□	7	8	BLM:UND1:6:NO_TRIG	BLM_UND1_6_NO_TRIG	MISSED
□	9	1	BLM:UND1:621:LOSS_L	BLM_UND1_621_LOSS_L	THRESHOLD
□	9	2	BLM:UND1:621:LOSS_H	BLM_UND1_621_LOSS_H	THRESHOLD
□	9	11	BLM:UND1:621:TIMING_L	BLM_UND1_621_TEST_L	THRESHOLD
□	9	12	BLM:UND1:621:TIMING_H	BLM_UND1_621_TEST_H	THRESHOLD
□	9	15	BLM:UND1:621:PED_L	BLM_UND1_621_PED_L	THRESHOLD
□	9	16	BLM:UND1:621:PED_H	BLM_UND1_621_PED_H	THRESHOLD
□	10	1	BLM:UND1:721:LOSS_L	BLM_UND1_721_LOSS_L	THRESHOLD
□	10	2	BLM:UND1:721:LOSS_H	BLM_UND1_721_LOSS_H	THRESHOLD
□	10	11	BLM:UND1:721:TEST_L	BLM_UND1_721_TEST_L	THRESHOLD
□	10	12	BLM:UND1:721:TEST_H	BLM_UND1_721_TEST_H	THRESHOLD
□	10	15	BLM:UND1:721:PED_L	BLM_UND1_721_PED_L	THRESHOLD
□	10	16	BLM:UND1:721:PED_H	BLM_UND1_721_PED_H	THRESHOLD
□	11	1	BLM:UND1:821:LOSS_L	BLM_UND1_821_LOSS_L	THRESHOLD
□	11	2	BLM:UND1:821:LOSS_H	BLM_UND1_821_LOSS_H	THRESHOLD
□	11	11	BLM:UND1:821:TEST_L	BLM_UND1_821_TEST_L	THRESHOLD
□	11	12	BLM:UND1:821:TEST_H	BLM_UND1_821_TEST_H	THRESHOLD
□	11	15	BLM:UND1:821:PED_L	BLM_UND1_821_PED_L	THRESHOLD
□	11	16	BLM:UND1:821:PED_H	BLM_UND1_821_PED_H	THRESHOLD
□	12	1	BLM:UND1:920:LOSS_L	BLM_UND1_920_LOSS_L	THRESHOLD
□	12	2	BLM:UND1:920:LOSS_H	BLM_UND1_920_LOSS_H	THRESHOLD
□	12	11	BLM:UND1:920:HRTBT_L	BLM_UND1_920_TEST_L	THRESHOLD
□	12	12	BLM:UND1:920:HRTBT_H	BLM_UND1_920_TEST_H	THRESHOLD

continued on next page...

. . . continued from previous page

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	12	15	BLM:UND1:920:PED_L	BLM_UND1_920_PED_L	THRESHOLD
□	12	16	BLM:UND1:920:PED_H	BLM_UND1_920_PED_H	THRESHOLD
□	13	1	BLM:UND1:1021:LOSS_L	BLM_UND1_1021_LOSS_L	THRESHOLD
□	13	2	BLM:UND1:1021:LOSS_H	BLM_UND1_1021_LOSS_H	THRESHOLD
□	13	11	BLM:UND1:1021:TEST_L	BLM_UND1_1021_TEST_L	THRESHOLD
□	13	12	BLM:UND1:1021:TEST_H	BLM_UND1_1021_TEST_H	THRESHOLD
□	13	15	BLM:UND1:1021:PED_L	BLM_UND1_1021_PED_L	THRESHOLD
□	13	16	BLM:UND1:1021:PED_H	BLM_UND1_1021_PED_H	THRESHOLD
□	14	1	BLM:UND1:1121:LOSS_L	BLM_UND1_1121_LOSS_L	THRESHOLD
□	14	2	BLM:UND1:1121:LOSS_H	BLM_UND1_1121_LOSS_H	THRESHOLD
□	14	11	BLM:UND1:1121:TEST_L	BLM_UND1_1121_TEST_L	THRESHOLD
□	14	12	BLM:UND1:1121:TEST_H	BLM_UND1_1121_TEST_H	THRESHOLD
□	14	15	BLM:UND1:1121:PED_L	BLM_UND1_1121_PED_L	THRESHOLD
□	14	16	BLM:UND1:1121:PED_H	BLM_UND1_1121_PED_H	THRESHOLD
□	15	1	BLM:UND1:1221:LOSS_L	BLM_UND1_1221_LOSS_L	THRESHOLD
□	15	2	BLM:UND1:1221:LOSS_H	BLM_UND1_1221_LOSS_H	THRESHOLD
□	15	11	BLM:UND1:1221:TEST_L	BLM_UND1_1221_TEST_L	THRESHOLD
□	15	12	BLM:UND1:1221:TEST_H	BLM_UND1_1221_TEST_H	THRESHOLD
□	15	15	BLM:UND1:1221:PED_L	BLM_UND1_1221_PED_L	THRESHOLD
□	15	16	BLM:UND1:1221:PED_H	BLM_UND1_1221_PED_H	THRESHOLD
□	16	1	BLM:UND1:1321:LOSS_L	BLM_UND1_1321_LOSS_L	THRESHOLD
□	16	2	BLM:UND1:1321:LOSS_H	BLM_UND1_1321_LOSS_H	THRESHOLD
□	16	11	BLM:UND1:1321:TEST_L	BLM_UND1_1321_TEST_L	THRESHOLD
□	16	12	BLM:UND1:1321:TEST_H	BLM_UND1_1321_TEST_H	THRESHOLD
□	16	15	BLM:UND1:1321:PED_L	BLM_UND1_1321_PED_L	THRESHOLD
□	16	16	BLM:UND1:1321:PED_H	BLM_UND1_1321_PED_H	THRESHOLD
□	17	1	HVPS:UND1:621:LOW	HVPS_UND1_621_LOW	FAULT
□	17	2	HVPS:UND1:621:HIGH	HVPS_UND1_621_HIGH	FAULT
□	17	3	HVPS:UND1:721:LOW	HVPS_UND1_721_LOW	FAULT
□	17	4	HVPS:UND1:721:HIGH	HVPS_UND1_721_HIGH	FAULT
□	17	5	HVPS:UND1:821:LOW	HVPS_UND1_821_LOW	FAULT
□	17	6	HVPS:UND1:821:HIGH	HVPS_UND1_821_HIGH	FAULT
□	17	7	HVPS:UND1:920:LOW	HVPS_UND1_920_LOW	FAULT
□	17	8	HVPS:UND1:920:HIGH	HVPS_UND1_920_HIGH	FAULT
□	17	9	HVPS:UND1:1021:LOW	HVPS_UND1_1021_LOW	FAULT
□	17	10	HVPS:UND1:1021:HIGH	HVPS_UND1_1021_HIGH	FAULT
□	17	11	HVPS:UND1:1121:LOW	HVPS_UND1_1121_LOW	FAULT
□	17	12	HVPS:UND1:1121:HIGH	HVPS_UND1_1121_HIGH	FAULT
□	17	13	HVPS:UND1:1221:LOW	HVPS_UND1_1221_LOW	FAULT
□	17	14	HVPS:UND1:1221:HIGH	HVPS_UND1_1221_HIGH	FAULT
□	17	15	HVPS:UND1:1321:LOW	HVPS_UND1_1321_LOW	FAULT

continued on next page. . .

. . . continued from previous page

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	17	16	HVPS:UND1:1321:HIGH	HVPS_UND1_1321_HIGH	FAULT

24 Link Node 34

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	1	1	TORO:LTU1:920:IMUNDI_L1	IMUNDI_COMP_L1	STATE
□	1	2	TORO:LTU1:920:IMUNDI_L2	IMUNDI_COMP_L2	STATE
□	1	3	TORO:DMP1:198:IMUNDO_L1	IMUNDO_COMP_L1	STATE
□	1	4	TORO:DMP1:198:IMUNDO_L2	IMUNDO_COMP_L2	STATE
□	1	5	TORO:B921:198:CHASIMUND	COMP_STAT_ON	STATE
□	1	6	OTRS:DMP1:695:OUT_LMTSW	PROF_DMP1_OTR_0695_OUT	STATE
□	1	7	OTRS:DMP1:695:IN_LMTSW	PROF_DMP1_OTR_0695_IN	STATE
□	1	8	DUMP:LTU1:970:TDUND_FS	TDUND_FS	STATE
□	1	9	DUMP:DMP1:699:FLOW_SW	DMPFC_FS	STATE
□	1	10	PICM:DMP1:B921:HV_PWR	PICM_DMP1_B921_HV_PWR	STATE
□	1	11	COLL:DMP1:310:FLOW_SW	COLL_PCPM0_FS	STATE
□	1	12	COLL:DMP1:710:FLOW_SW	COLL_PCPM1_FS	STATE
□	1	14	STPR:DMP1:991:FLOW_SW	ST2_FS	STATE
□	1	15	IOC:UND1:BP03:MPSSTAT	IOC_UND1_BP03_MPSSTAT	STATE
□	1	16	IOC:UND1:BP04:MPSSTAT	IOC_UND1_BP04_MPSSTAT	STATE
□	2	1	VVPG:UND1:2500:POSITION	VACV_UND_2500	STATE
□	2	2	VVPG:DMP1:100:POSITION	VACV_DMP_100	STATE
□	2	3	VVPG:DMP1:395:POSITION	VACV_DMP_395	STATE
□	2	4	VVPG:DMP1:700:POSITION	VACV_DMP_700	STATE
□	2	7	VVPG:DMP1:355:OPENSTATUS	VVPG_DMP1_355_OPENSTATUS	STATE
□	2	8	VVPG:DMP1:355:CLOSEDSTATUS	VVPG_DMP1_355_CLOSEDSTATUS	STATE
□	2	9	COLL:DMP1:800:FLOW_SW	COLL_PCPM2_FS	STATE
□	2	10	VVMG:DMP1:743:POSITION	VVMG_DMP1_743_POSITION	STATE
□	2	11	VVFS:DMP1:107:OPEN_LMTSW	VVFS_DMP1_107_OPEN_LMTSW	STATE
□	7	8	PICM:DMP1:698:NO_TRIG	PICS_DMP1_100_NO_TRIG	MISSED
□	9	1	PICM:DMP1:698:LOSSL	PICS_DMP1_100_LOSSL	THRESHOLD
□	9	2	PICM:DMP1:698:LOSSH	PICS_DMP1_100_LOSSH	THRESHOLD
□	10	1	PICM:DMP1:699:LOSSL	PICS_DMP2_200_LOSSL	THRESHOLD
□	10	2	PICM:DMP1:699:LOSSH	PICS_DMP2_200_LOSSH	THRESHOLD

25 Link Node 35

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	1	1	BFW:UND1:1410:OUT	BFW_UND1_1410_OUT	STATE
□	1	2	BFW:UND1:1510:OUT	BFW_UND1_1510_OUT	STATE
□	1	3	BFW:UND1:1610:OUT	BFW_UND1_1610_OUT	STATE
□	1	4	BFW:UND1:1710:OUT	BFW_UND1_1710_OUT	STATE
□	1	5	BFW:UND1:1810:OUT	BFW_UND1_1810_OUT	STATE
□	1	6	BFW:UND1:1910:OUT	BFW_UND1_1910_OUT	STATE
□	1	7	BFW:UND1:2010:OUT	BFW_UND1_2010_OUT	STATE
□	1	8	BFW:UND1:2110:OUT	BFW_UND1_2110_OUT	STATE
□	1	9	BFW:UND1:1410:IN	BFW_UND1_1410_IN	STATE
□	1	10	BFW:UND1:1510:IN	BFW_UND1_1510_IN	STATE
□	1	11	BFW:UND1:1610:IN	BFW_UND1_1610_IN	STATE
□	1	12	BFW:UND1:1710:IN	BFW_UND1_1710_IN	STATE
□	1	14	BFW:UND1:1910:IN	BFW_UND1_1910_IN	STATE
□	1	15	BFW:UND1:2010:IN	BFW_UND1_2010_IN	STATE
□	1	16	BFW:UND1:2110:IN	BFW_UND1_2110_IN	STATE
□	7	8	BLM:UND1:14:NO_TRIG	BLM_UND1_14_NO_TRIG	MISSED
□	9	1	BLM:UND1:1421:LOSS_L	BLM_UND1_1421_LOSS_L	THRESHOLD
□	9	2	BLM:UND1:1421:LOSS_H	BLM_UND1_1421_LOSS_H	THRESHOLD
□	9	11	BLM:UND1:1421:TIMING_L	BLM_UND1_1421_TEST_L	THRESHOLD
□	9	12	BLM:UND1:1421:TIMING_H	BLM_UND1_1421_TEST_H	THRESHOLD
□	9	15	BLM:UND1:1421:PED_L	BLM_UND1_1421_PED_L	THRESHOLD
□	9	16	BLM:UND1:1421:PED_H	BLM_UND1_1421_PED_H	THRESHOLD
□	10	1	BLM:UND1:1521:LOSS_L	BLM_UND1_1521_LOSS_L	THRESHOLD
□	10	2	BLM:UND1:1521:LOSS_H	BLM_UND1_1521_LOSS_H	THRESHOLD
□	10	11	BLM:UND1:1521:TEST_L	BLM_UND1_1521_TEST_L	THRESHOLD
□	10	12	BLM:UND1:1521:TEST_H	BLM_UND1_1521_TEST_H	THRESHOLD
□	10	15	BLM:UND1:1521:PED_L	BLM_UND1_1521_PED_L	THRESHOLD
□	10	16	BLM:UND1:1521:PED_H	BLM_UND1_1521_PED_H	THRESHOLD
□	11	1	BLM:UND1:1621:LOSS_L	BLM_UND1_1621_LOSS_L	THRESHOLD
□	11	2	BLM:UND1:1621:LOSS_H	BLM_UND1_1621_LOSS_H	THRESHOLD
□	11	11	BLM:UND1:1621:TEST_L	BLM_UND1_1621_TEST_L	THRESHOLD
□	11	12	BLM:UND1:1621:TEST_H	BLM_UND1_1621_TEST_H	THRESHOLD
□	11	15	BLM:UND1:1621:PED_L	BLM_UND1_1621_PED_L	THRESHOLD
□	11	16	BLM:UND1:1621:PED_H	BLM_UND1_1621_PED_H	THRESHOLD
□	12	1	BLM:UND1:1720:LOSS_L	BLM_UND1_1720_LOSS_L	THRESHOLD
□	12	2	BLM:UND1:1720:LOSS_H	BLM_UND1_1720_LOSS_H	THRESHOLD
□	12	11	BLM:UND1:1720:HRTBT_L	BLM_UND1_1720_TEST_L	THRESHOLD
□	12	12	BLM:UND1:1720:HRTBT_H	BLM_UND1_1720_TEST_H	THRESHOLD

continued on next page...

. . . continued from previous page

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	12	15	BLM:UND1:1720:PED_L	BLM_UND1_1720_PED_L	THRESHOLD
□	12	16	BLM:UND1:1720:PED_H	BLM_UND1_1720_PED_H	THRESHOLD
□	13	1	BLM:UND1:1821:LOSS_L	BLM_UND1_1821_LOSS_L	THRESHOLD
□	13	2	BLM:UND1:1821:LOSS_H	BLM_UND1_1821_LOSS_H	THRESHOLD
□	13	11	BLM:UND1:1821:TEST_L	BLM_UND1_1821_TEST_L	THRESHOLD
□	13	12	BLM:UND1:1821:TEST_H	BLM_UND1_1821_TEST_H	THRESHOLD
□	13	15	BLM:UND1:1821:PED_L	BLM_UND1_1821_PED_L	THRESHOLD
□	13	16	BLM:UND1:1821:PED_H	BLM_UND1_1821_PED_H	THRESHOLD
□	14	1	BLM:UND1:1921:LOSS_L	BLM_UND1_1921_LOSS_L	THRESHOLD
□	14	2	BLM:UND1:1921:LOSS_H	BLM_UND1_1921_LOSS_H	THRESHOLD
□	14	11	BLM:UND1:1921:TEST_L	BLM_UND1_1921_TEST_L	THRESHOLD
□	14	12	BLM:UND1:1921:TEST_H	BLM_UND1_1921_TEST_H	THRESHOLD
□	14	15	BLM:UND1:1921:PED_L	BLM_UND1_1921_PED_L	THRESHOLD
□	14	16	BLM:UND1:1921:PED_H	BLM_UND1_1921_PED_H	THRESHOLD
□	15	1	BLM:UND1:2021:LOSS_L	BLM_UND1_2021_LOSS_L	THRESHOLD
□	15	2	BLM:UND1:2021:LOSS_H	BLM_UND1_2021_LOSS_H	THRESHOLD
□	15	11	BLM:UND1:2021:TEST_L	BLM_UND1_2021_TEST_L	THRESHOLD
□	15	12	BLM:UND1:2021:TEST_H	BLM_UND1_2021_TEST_H	THRESHOLD
□	15	15	BLM:UND1:2021:PED_L	BLM_UND1_2021_PED_L	THRESHOLD
□	15	16	BLM:UND1:2021:PED_H	BLM_UND1_2021_PED_H	THRESHOLD
□	16	1	BLM:UND1:2121:LOSS_L	BLM_UND1_2121_LOSS_L	THRESHOLD
□	16	2	BLM:UND1:2121:LOSS_H	BLM_UND1_2121_LOSS_H	THRESHOLD
□	16	11	BLM:UND1:2121:TEST_L	BLM_UND1_2121_TEST_L	THRESHOLD
□	16	12	BLM:UND1:2121:TEST_H	BLM_UND1_2121_TEST_H	THRESHOLD
□	16	15	BLM:UND1:2121:PED_L	BLM_UND1_2121_PED_L	THRESHOLD
□	16	16	BLM:UND1:2121:PED_H	BLM_UND1_2121_PED_H	THRESHOLD
□	17	1	HVPS:UND1:1421:LOW	HVPS_UND1_1421_LOW	FAULT
□	17	2	HVPS:UND1:1421:HIGH	HVPS_UND1_1421_HIGH	FAULT
□	17	3	HVPS:UND1:1521:LOW	HVPS_UND1_1521_LOW	FAULT
□	17	4	HVPS:UND1:1521:HIGH	HVPS_UND1_1521_HIGH	FAULT
□	17	5	HVPS:UND1:1621:LOW	HVPS_UND1_1621_LOW	FAULT
□	17	6	HVPS:UND1:1621:HIGH	HVPS_UND1_1621_HIGH	FAULT
□	17	7	HVPS:UND1:1720:LOW	HVPS_UND1_1720_LOW	FAULT
□	17	8	HVPS:UND1:1720:HIGH	HVPS_UND1_1720_HIGH	FAULT
□	17	9	HVPS:UND1:1821:LOW	HVPS_UND1_1821_LOW	FAULT
□	17	10	HVPS:UND1:1821:HIGH	HVPS_UND1_1821_HIGH	FAULT
□	17	11	HVPS:UND1:1921:LOW	HVPS_UND1_1921_LOW	FAULT
□	17	12	HVPS:UND1:1921:HIGH	HVPS_UND1_1921_HIGH	FAULT
□	17	13	HVPS:UND1:2021:LOW	HVPS_UND1_2021_LOW	FAULT
□	17	14	HVPS:UND1:2021:HIGH	HVPS_UND1_2021_HIGH	FAULT
□	17	15	HVPS:UND1:2121:LOW	HVPS_UND1_2121_LOW	FAULT

continued on next page. . .

. . . continued from previous page

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	17	16	HVPS:UND1:2121:HIGH	HVPS_UND1_2121_HIGH	FAULT

26 Link Node 36

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	1	1	BFW:UND1:2210:OUT	BFW_UND1_2210_OUT	STATE
□	1	2	BFW:UND1:2310:OUT	BFW_UND1_2310_OUT	STATE
□	1	3	BFW:UND1:2410:OUT	BFW_UND1_2410_OUT	STATE
□	1	4	BFW:UND1:2510:OUT	BFW_UND1_2510_OUT	STATE
□	1	5	BFW:UND1:2610:OUT	BFW_UND1_2610_OUT	STATE
□	1	6	BFW:UND1:2710:OUT	BFW_UND1_2710_OUT	STATE
□	1	7	BFW:UND1:2810:OUT	BFW_UND1_2810_OUT	STATE
□	1	8	BFW:UND1:2910:OUT	BFW_UND1_2910_OUT	STATE
□	1	9	BFW:UND1:2210:IN	BFW_UND1_2210_IN	STATE
□	1	10	BFW:UND1:2310:IN	BFW_UND1_2310_IN	STATE
□	1	11	BFW:UND1:2410:IN	BFW_UND1_2410_IN	STATE
□	1	12	BFW:UND1:2510:IN	BFW_UND1_2510_IN	STATE
□	1	14	BFW:UND1:2710:IN	BFW_UND1_2710_IN	STATE
□	1	15	BFW:UND1:2810:IN	BFW_UND1_2810_IN	STATE
□	1	16	BFW:UND1:2910:IN	BFW_UND1_2910_IN	STATE
□	7	8	BLM:UND1:22:NOTRIG	BLM_TRIG	MISSED
□	9	1	BLM:UND1:2221:LOSS_L	BLM_2220_QBL	THRESHOLD
□	9	2	BLM:UND1:2221:LOSS_H	BLM_2220_QBH	THRESHOLD
□	9	11	BLM:UND1:2221:TIMING_L	BLM_2220_QTL	THRESHOLD
□	9	12	BLM:UND1:2221:TIMING_H	BLM_2220_QTH	THRESHOLD
□	9	13	BLM:UND1:2221:TIMING_1_L	BLM_2220_T1L	THRESHOLD
□	9	14	BLM:UND1:2221:TIMING_1_H	BLM_2220_T1H	THRESHOLD
□	9	15	BLM:UND1:2221:PED_L	BLM_2220_QBLL	THRESHOLD
□	9	16	BLM:UND1:2221:PED_H	BLM_2220_QBLH	THRESHOLD
□	10	1	BLM:UND1:2321:LOSS_L	BLM_2320_QBL	THRESHOLD
□	10	2	BLM:UND1:2321:LOSS_H	BLM_2320_QBH	THRESHOLD
□	10	11	BLM:UND1:2321:TEST_L	BLM_2320_QTL	THRESHOLD
□	10	12	BLM:UND1:2321:TEST_H	BLM_2320_QTH	THRESHOLD
□	10	13	BLM:UND1:2321:TEST_1_L	BLM_2320_T1L	THRESHOLD
□	10	14	BLM:UND1:2321:TEST_1_H	BLM_2320_T1H	THRESHOLD
□	10	15	BLM:UND1:2321:PED_L	BLM_2320_QBLL	THRESHOLD
□	10	16	BLM:UND1:2321:PED_H	BLM_2320_QBLH	THRESHOLD
□	11	1	BLM:UND1:2421:LOSS_L	BLM_2420_QBL	THRESHOLD
□	11	2	BLM:UND1:2421:LOSS_H	BLM_2420_QBH	THRESHOLD
□	11	11	BLM:UND1:2421:TEST_L	BLM_2420_QTL	THRESHOLD
□	11	12	BLM:UND1:2421:TEST_H	BLM_2420_QTH	THRESHOLD
□	11	13	BLM:UND1:2421:TEST_1_L	BLM_2420_T1L	THRESHOLD
□	11	14	BLM:UND1:2421:TEST_1_H	BLM_2420_T1H	THRESHOLD

continued on next page...

. . . continued from previous page

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	11	15	BLM:UND1:2421:PED_L	BLM_2420_QBLL	THRESHOLD
□	11	16	BLM:UND1:2421:PED_H	BLM_2420_QBLH	THRESHOLD
□	12	1	BLM:UND1:2520:LOSS_L	BLM_2520_QBL	THRESHOLD
□	12	2	BLM:UND1:2520:LOSS_H	BLM_2520_QBH	THRESHOLD
□	12	11	BLM:UND1:2520:HRTBT_L	BLM_2520_QTL	THRESHOLD
□	12	12	BLM:UND1:2520:HRTBT_H	BLM_2520_QTH	THRESHOLD
□	12	13	BLM:UND1:2520:HRTBT_1_L	BLM_2520_T1L	THRESHOLD
□	12	14	BLM:UND1:2520:HRTBT_1_H	BLM_2520_T1H	THRESHOLD
□	12	15	BLM:UND1:2520:PED_L	BLM_2520_QBLL	THRESHOLD
□	12	16	BLM:UND1:2520:PED_H	BLM_2520_QBLH	THRESHOLD
□	13	1	BLM:UND1:2621:LOSS_L	BLM_2620_QBL	THRESHOLD
□	13	2	BLM:UND1:2621:LOSS_H	BLM_2620_QBH	THRESHOLD
□	13	11	BLM:UND1:2621:TEST_L	BLM_2620_QTL	THRESHOLD
□	13	12	BLM:UND1:2621:TEST_H	BLM_2620_QTH	THRESHOLD
□	13	13	BLM:UND1:2621:TEST_1_L	BLM_2620_T1L	THRESHOLD
□	13	14	BLM:UND1:2621:TEST_1_H	BLM_2620_T1H	THRESHOLD
□	13	15	BLM:UND1:2621:PED_L	BLM_2620_QBLL	THRESHOLD
□	13	16	BLM:UND1:2621:PED_H	BLM_2620_QBLH	THRESHOLD
□	14	1	BLM:UND1:2721:LOSS_L	BLM_2720_QBL	THRESHOLD
□	14	2	BLM:UND1:2721:LOSS_H	BLM_2720_QBH	THRESHOLD
□	14	11	BLM:UND1:2721:TEST_L	BLM_2720_QTL	THRESHOLD
□	14	12	BLM:UND1:2721:TEST_H	BLM_2720_QTH	THRESHOLD
□	14	13	BLM:UND1:2721:TEST_1_L	BLM_2720_T1L	THRESHOLD
□	14	14	BLM:UND1:2721:TEST_1_H	BLM_2720_T1H	THRESHOLD
□	14	15	BLM:UND1:2721:PED_L	BLM_2720_QBLL	THRESHOLD
□	14	16	BLM:UND1:2721:PED_H	BLM_2720_QBLH	THRESHOLD
□	15	1	BLM:UND1:2821:LOSS_L	BLM_2820_QBL	THRESHOLD
□	15	2	BLM:UND1:2821:LOSS_H	BLM_2820_QBH	THRESHOLD
□	15	11	BLM:UND1:2821:TEST_L	BLM_2820_QTL	THRESHOLD
□	15	12	BLM:UND1:2821:TEST_H	BLM_2820_QTH	THRESHOLD
□	15	13	BLM:UND1:2821:TEST_1_L	BLM_2820_T1L	THRESHOLD
□	15	14	BLM:UND1:2821:TEST_1_H	BLM_2820_T1H	THRESHOLD
□	15	15	BLM:UND1:2821:PED_L	BLM_2820_QBLL	THRESHOLD
□	15	16	BLM:UND1:2821:PED_H	BLM_2820_QBLH	THRESHOLD
□	16	1	BLM:UND1:2921:LOSS_L	BLM_2920_QBL	THRESHOLD
□	16	2	BLM:UND1:2921:LOSS_H	BLM_2920_QBH	THRESHOLD
□	16	11	BLM:UND1:2921:TEST_L	BLM_2920_QTL	THRESHOLD
□	16	12	BLM:UND1:2921:TEST_H	BLM_2920_QTH	THRESHOLD
□	16	13	BLM:UND1:2921:TEST_1_L	BLM_2920_T1L	THRESHOLD
□	16	14	BLM:UND1:2921:TEST_1_H	BLM_2920_T1H	THRESHOLD
□	16	15	BLM:UND1:2921:PED_L	BLM_2920_QBLL	THRESHOLD

continued on next page. . .

. . . continued from previous page

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	16	16	BLM:UND1:2921:PED_H	BLM_2920_QBLH	THRESHOLD
□	17	1	HVPS:UND1:2221:LOW	HVPS_UND1_2221_LOW	FAULT
□	17	2	HVPS:UND1:2221:HIGH	HVPS_UND1_2221_HIGH	FAULT
□	17	3	HVPS:UND1:2321:LOW	HVPS_UND1_2321_LOW	FAULT
□	17	4	HVPS:UND1:2321:HIGH	HVPS_UND1_2321_HIGH	FAULT
□	17	5	HVPS:UND1:2421:LOW	HVPS_UND1_2421_LOW	FAULT
□	17	6	HVPS:UND1:2421:HIGH	HVPS_UND1_2421_HIGH	FAULT
□	17	7	HVPS:UND1:2520:LOW	HVPS_UND1_2520_LOW	FAULT
□	17	8	HVPS:UND1:2520:HIGH	HVPS_UND1_2520_HIGH	FAULT
□	17	9	HVPS:UND1:2621:LOW	HVPS_UND1_2621_LOW	FAULT
□	17	10	HVPS:UND1:2621:HIGH	HVPS_UND1_2621_HIGH	FAULT
□	17	11	HVPS:UND1:2721:LOW	HVPS_UND1_2721_LOW	FAULT
□	17	12	HVPS:UND1:2721:HIGH	HVPS_UND1_2721_HIGH	FAULT
□	17	13	HVPS:UND1:2821:LOW	HVPS_UND1_2821_LOW	FAULT
□	17	14	HVPS:UND1:2821:HIGH	HVPS_UND1_2821_HIGH	FAULT
□	17	15	HVPS:UND1:2921:LOW	HVPS_UND1_2921_LOW	FAULT
□	17	16	HVPS:UND1:2921:HIGH	HVPS_UND1_2921_HIGH	FAULT

27 Link Node 37

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	1	1	BFW:UND1:3010:OUT	BFW_UND1_3010_OUT	STATE
□	1	2	BFW:UND1:3110:OUT	BFW_UND1_3110_OUT	STATE
□	1	3	BFW:UND1:3210:OUT	BFW_UND1_3210_OUT	STATE
□	1	4	BFW:UND1:3310:OUT	BFW_UND1_3310_OUT	STATE
□	1	5	BFW:UND1:3010:IN	BFW_UND1_3010_IN	STATE
□	1	6	BFW:UND1:3110:IN	BFW_UND1_3110_IN	STATE
□	1	7	BFW:UND1:3210:IN	BFW_UND1_3210_IN	STATE
□	1	8	BFW:UND1:3310:IN	BFW_UND1_3310_IN	STATE
□	1	9	BFW:UND1:1810:IN	BFW_UND1_1810_IN	STATE
□	1	10	BFW:UND1:2610:IN	BFW_UND1_2610_IN	STATE
□	7	8	BLM:UND1:30:NO_TRIG	BLM_UND1_30_NO_TRIG	MISSED
□	9	1	BLM:UND1:3021:LOSS_L	BLM_UND1_3021_LOSS_L	THRESHOLD
□	9	2	BLM:UND1:3021:LOSS_H	BLM_UND1_3021_LOSS_H	THRESHOLD
□	9	11	BLM:UND1:3021:TIMING_L	BLM_UND1_3021_TEST_L	THRESHOLD
□	9	12	BLM:UND1:3021:TIMING_H	BLM_UND1_3021_TEST_H	THRESHOLD
□	9	15	BLM:UND1:3021:PED_L	BLM_UND1_3021_PED_L	THRESHOLD
□	9	16	BLM:UND1:3021:PED_H	BLM_UND1_3021_PED_H	THRESHOLD
□	10	1	BLM:UND1:3121:LOSS_L	BLM_UND1_3121_LOSS_L	THRESHOLD
□	10	2	BLM:UND1:3121:LOSS_H	BLM_UND1_3121_LOSS_H	THRESHOLD
□	10	11	BLM:UND1:3121:TEST_L	BLM_UND1_3121_TEST_L	THRESHOLD
□	10	12	BLM:UND1:3121:TEST_H	BLM_UND1_3121_TEST_H	THRESHOLD
□	10	15	BLM:UND1:3121:PED_L	BLM_UND1_3121_PED_L	THRESHOLD
□	10	16	BLM:UND1:3121:PED_H	BLM_UND1_3121_PED_H	THRESHOLD
□	11	1	BLM:UND1:3221:LOSS_L	BLM_UND1_3221_LOSS_L	THRESHOLD
□	11	2	BLM:UND1:3221:LOSS_H	BLM_UND1_3221_LOSS_H	THRESHOLD
□	11	11	BLM:UND1:3221:TEST_L	BLM_UND1_3221_TEST_L	THRESHOLD
□	11	12	BLM:UND1:3221:TEST_H	BLM_UND1_3221_TEST_H	THRESHOLD
□	11	15	BLM:UND1:3221:PED_L	BLM_UND1_3221_PED_L	THRESHOLD
□	11	16	BLM:UND1:3221:PED_H	BLM_UND1_3221_PED_H	THRESHOLD
□	12	1	BLM:UND1:3320:LOSS_L	BLM_UND1_3320_LOSS_L	THRESHOLD
□	12	2	BLM:UND1:3320:LOSS_H	BLM_UND1_3320_LOSS_H	THRESHOLD
□	12	11	BLM:UND1:3320:HRTBT_L	BLM_UND1_3320_TEST_L	THRESHOLD
□	12	12	BLM:UND1:3320:HRTBT_H	BLM_UND1_3320_TEST_H	THRESHOLD
□	12	15	BLM:UND1:3320:PED_L	BLM_UND1_3320_PED_L	THRESHOLD
□	12	16	BLM:UND1:3320:PED_H	BLM_UND1_3320_PED_H	THRESHOLD
□	13	1	BLM:UND1:1721:LOSS_L	BLM_UND1_1721_LOSS_L	THRESHOLD
□	13	2	BLM:UND1:1721:LOSS_H	BLM_UND1_1721_LOSS_H	THRESHOLD
□	13	11	BLM:UND1:1721:TEST_L	BLM_UND1_1721_TEST_L	THRESHOLD

continued on next page...

. . . continued from previous page

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	13	12	BLM:UND1:1721:TEST_H	BLM_UND1_1721_TEST_H	THRESHOLD
□	13	15	BLM:UND1:1721:PED_L	BLM_UND1_1721_PED_L	THRESHOLD
□	13	16	BLM:UND1:1721:PED_H	BLM_UND1_1721_PED_H	THRESHOLD
□	14	1	BLM:UND1:2521:LOSS_L	BLM_UND1_2521_LOSS_L	THRESHOLD
□	14	2	BLM:UND1:2521:LOSS_H	BLM_UND1_2521_LOSS_H	THRESHOLD
□	14	11	BLM:UND1:2521:TEST_L	BLM_UND1_2521_TEST_L	THRESHOLD
□	14	12	BLM:UND1:2521:TEST_H	BLM_UND1_2521_TEST_H	THRESHOLD
□	14	15	BLM:UND1:2521:PED_L	BLM_UND1_2521_PED_L	THRESHOLD
□	14	16	BLM:UND1:2521:PED_H	BLM_UND1_2521_PED_H	THRESHOLD
□	15	1	BLM:UND1:3321:LOSS_L	BLM_UND1_3321_LOSS_L	THRESHOLD
□	15	2	BLM:UND1:3321:LOSS_H	BLM_UND1_3321_LOSS_H	THRESHOLD
□	15	11	BLM:UND1:3321:TEST_L	BLM_UND1_3321_TEST_L	THRESHOLD
□	15	12	BLM:UND1:3321:TEST_H	BLM_UND1_3321_TEST_H	THRESHOLD
□	15	15	BLM:UND1:3321:PED_L	BLM_UND1_3321_PED_L	THRESHOLD
□	15	16	BLM:UND1:3321:PED_H	BLM_UND1_3321_PED_H	THRESHOLD
□	17	1	HVPS:UND1:3021:LOW	HVPS_UND1_3021_LOW	FAULT
□	17	2	HVPS:UND1:3021:HIGH	HVPS_UND1_3021_HIGH	FAULT
□	17	3	HVPS:UND1:3121:LOW	HVPS_UND1_3121_LOW	FAULT
□	17	4	HVPS:UND1:3121:HIGH	HVPS_UND1_3121_HIGH	FAULT
□	17	5	HVPS:UND1:3221:LOW	HVPS_UND1_3221_LOW	FAULT
□	17	6	HVPS:UND1:3221:HIGH	HVPS_UND1_3221_HIGH	FAULT
□	17	7	HVPS:UND1:3320:LOW	HVPS_UND1_3320_LOW	FAULT
□	17	8	HVPS:UND1:3320:HIGH	HVPS_UND1_3320_HIGH	FAULT
□	17	9	HVPS:UND1:1721:LOW	HVPS_UND1_1721_LOW	FAULT
□	17	10	HVPS:UND1:1721:HIGH	HVPS_UND1_1721_HIGH	FAULT
□	17	11	HVPS:UND1:2521:LOW	HVPS_UND1_2521_LOW	FAULT
□	17	12	HVPS:UND1:2521:HIGH	HVPS_UND1_2521_HIGH	FAULT
□	17	13	HVPS:UND1:3321:LOW	HVPS_UND1_3321_LOW	FAULT
□	17	14	HVPS:UND1:3321:HIGH	HVPS_UND1_3321_HIGH	FAULT
□	17	15	HVPS:UND1:SP3:LOW	HVPS_UND1_SP3_LOW	FAULT
□	17	16	HVPS:UND1:SP3:HIGH	HVPS_UND1_SP3_HIGH	FAULT

28 Link Node 38

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	1	1	VMPS:FEE1:HXTD:SUM	VMPS_FEE1_HXTD_SUM	FAULT
□	1	2	VMPS:FEE1:GAS:SUM	VMPS_FEE1_GAS_SUM	FAULT
□	1	3	VMPS:NEH1:HXTD:SUM	VMPS_NEH1_HXTD_SUM	FAULT
□	1	4	CAMR:FEE1:852:STATUS	CAMR_FEE1_852_STATUS	FAULT
□	1	5	CAMR:FEE1:913:STATUS	CAMR_FEE1_913_STATUS	FAULT
□	1	6	VMPS:FEE1:703:ISOL_S1	VMPS_FEE1_703_ISOL_S1	FAULT
□	1	7	VMPS:FEE1:703:ISOL_S2	VMPS_FEE1_703_ISOL_S2	FAULT
□	1	8	MIRR:FEE1:1560:OUT_LIMIT1	MIRR_FEE1_1560_OUT_LIMIT1	POSITION
□	1	9	MIRR:FEE1:1560:OUT_LIMIT2	MIRR_FEE1_1560_OUT_LIMIT2	POSITION
□	1	10	XTAL:FEE1:441:OUT_LIMSW	XTAL_FEE1_441_OUT_LIMSW	POSITION
□	4	3	STPR:FEE1:1:S1IN	STPR_FEE1_1_S1IN	POSITION
□	4	4	STPR:FEE1:1:S2IN	STPR_FEE1_1_S2IN	STATE
□	4	5	STPR:FEE1:1:S2BIN	STPR_FEE1_1_S2BIN	STATE
□	4	6	STPR:FEE1:1:SH1IN	STPR_FEE1_1_SH1IN	STATE
□	4	8	XPP:SH3:STP:OPN_DI	XPP_SH3_STP_OPN_DI	POSITION
□	4	9	XPP:SH3:STP:CLS_DI	XPP_SH3_STP_CLS_DI	POSITION
□	5	1	CAMR:FEE1:1561:IN	CAMR_FEE1_1561_IN	STATE
□	5	2	CAMR:FEE1:1561:OUT	CAMR_FEE1_1561_OUT	STATE
□	5	7	CAMR:FEE1:1692:IN	CAMR_FEE1_1692_IN	STATE
□	5	8	CAMR:FEE1:1692:OUT	CAMR_FEE1_1692_OUT	STATE
□	5	9	CAMR:FEE1:1953:IN	CAMR_FEE1_1953_IN	STATE
□	5	10	CAMR:FEE1:1953:OUT	CAMR_FEE1_1953_OUT	STATE
□	5	11	CAMR:FEE1:2953:IN	CAMR_FEE1_2953_IN	STATE
□	5	12	CAMR:FEE1:2953:OUT	CAMR_FEE1_2953_OUT	STATE
□	6	1	VMPS:NEH:703:ISOL_H	VMPS_NEH_703_ISOL_H	STATE
□	6	2	VMPS:NEH:703:ISOL_S1	VMPS_NEH_703_ISOL_S1	STATE
□	6	3	VMPS:NEH:703:ISOL_S2	VMPS_NEH_703_ISOL_S2	STATE
□	6	5	AMO:EXP:MPS:01	AMO_EXP_MPS_01	STATE
□	6	7	CAMR:NEH1:124:IN	CAMR_NEH1_124_IN	STATE
□	6	8	CAMR:NEH1:124:OUT	CAMR_NEH1_124_OUT	STATE
□	6	9	CAMR:NEH1:195:IN	CAMR_NEH1_195_IN	STATE
□	6	10	CAMR:NEH1:195:OUT	CAMR_NEH1_195_OUT	STATE
□	6	11	CAMR:NEH1:1124:IN	CAMR_NEH1_1124_IN	STATE
□	6	12	CAMR:NEH1:1124:OUT	CAMR_NEH1_1124_OUT	STATE
□	6	13	CAMR:NEH1:2124:IN	CAMR_NEH1_2124_IN	STATE
□	6	14	CAMR:NEH1:2124:OUT	CAMR_NEH1_2124_OUT	STATE

29 Link Node 39

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	1	1	SAS:MMM:01:A	SAS_MMM_01_A	POSITION
□	1	2	SAS:MMM:01:B	SAS_MMM_01_B	POSITION
□	1	5	AMO:MPS:VAC:OK_SUM	AMO_MPS_VAC_OK_SUM	STATE
□	1	7	AMO:KBO:VGC:02B	AMO_KBO_VGC_02B	POSITION
□	1	8	AMO:KBO:VGC:02A	AMO_KBO_VGC_02A	POSITION
□	1	9	AMO:LMP:VGC_30:OPN_DI	AMO_LMP_VGC_30_OPN_DI	POSITION
□	1	10	AMO:LMP:VGC_30:CLS_DI	AMO_LMP_VGC_30_CLS_DI	POSITION
□	2	1	SXR:TSS:VGC_01:CLS_DI	SXR_TSS_VGC_01_CLS_DI	STATE
□	2	2	SXR:TSS:VGC_01:OPN_DI	SXR_TSS_VGC_01_OPN_DI	STATE
□	2	3	SXR:MON:VGC_01:CLS_DI	SXR_MON_VGC_01_CLS_DI	STATE
□	2	4	SXR:MON:VGC_01:OPN_DI	SXR_MON_VGC_01_OPN_DI	STATE
□	2	5	SXR:MON:MMS_06:B	SXR_MON_MMS_06_B	STATE
□	2	6	SXR:COL:VGC_01:CLS_DI	SXR_COL_VGC_01_CLS_DI	STATE
□	2	7	SXR:COL:VGC_01:OPN_DI	SXR_COL_VGC_01_OPN_DI	STATE
□	2	8	SXR:EXS:VGC_01:CLS_DI	SXR_EXS_VGC_01_CLS_DI	STATE
□	2	9	SXR:EXS:VGC_01:OPN_DI	SXR_EXS_VGC_01_OPN_DI	STATE
□	2	10	SXR:EXS:MMS_01:B	SXR_EXS_MMS_01_B	STATE
□	2	11	SXR:PST:VGC_01:CLS_DI	SXR_PST_VGC_01_CLS_DI	STATE
□	2	12	SXR:PST:VGC_01:OPN_DI	SXR_PST_VGC_01_OPN_DI	STATE
□	2	13	SXR:FLX:VGC_01:CLS_DI	SXR_FLX_VGC_01_CLS_DI	STATE
□	2	14	SXR:FLX:VGC_01:OPN_DI	SXR_FLX_VGC_01_OPN_DI	STATE
□	2	15	SXR:KBO:VGC_01:CLS_DI	SXR_KBO_VGC_01_CLS_DI	STATE
□	2	16	SXR:KBO:VGC_01:OPN_DI	SXR_KBO_VGC_01_OPN_DI	STATE
□	3	1	SXR:DFP:VGC_01:CLS_DI	SXR_DFP_VGC_01_CLS_DI	STATE
□	3	2	SXR:DFP:VGC_01:OPN_DI	SXR_DFP_VGC_01_OPN_DI	STATE
□	3	3	SXR:LIN:VGC_01:CLS_DI	SXR_LIN_VGC_01_CLS_DI	STATE
□	3	4	SXR:LIN:VGC_01:OPN_DI	SXR_LIN_VGC_01_OPN_DI	STATE
□	3	5	SXR:EXP:MPS:01	SXR_EXP_MPS_01	STATE
□	3	6	HX2:SB1:VGC_01:CLS_DI	HX2_SB1_VGC_01_CLS_DI	STATE
□	3	7	HX2:SB1:VGC_01:OPN_DI	HX2_SB1_VGC_01_OPN_DI	STATE
□	3	8	HX2:DVD:VGC_01:CLS_DI	HX2_DVD_VGC_01_CLS_DI	STATE
□	3	9	HX2:DVD:VGC_01:OPN_DI	HX2_DVD_VGC_01_OPN_DI	STATE
□	3	10	XPP:NH3:POS_00:IN	XPP_NH3_POS_00_IN	STATE
□	3	11	HX3:UVD:VGC_01:CLS_DI	HX3_UVD_VGC_01_CLS_DI	STATE
□	3	12	HX3:UVD:VGC_01:OPN_DI	HX3_UVD_VGC_01_OPN_DI	STATE
□	3	13	HX3:DVD:VGC_01:CLS_DI	HX3_DVD_VGC_01_CLS_DI	STATE
□	3	14	HX3:DVD:VGC_01:OPN_DI	HX3_DVD_VGC_01_OPN_DI	STATE
□	3	15	HX3:MON:VGC_01:CLS_DI	HX3_MON_VGC_01_CLS_DI	POSITION

continued on next page...

. . . continued from previous page

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	3	16	HX3:MON:VGC_01:OPN_DI	HX3_MON_VGC_01_OPN_DI	POSITION
□	4	1	XPP:SB2:VGC_01:CLS_DI	XPP_SB2_VGC_01_CLS_DI	POSITION
□	4	2	XPP:SB2:VGC_01:OPN_DI	XPP_SB2_VGC_01_OPN_DI	POSITION
□	4	3	XPP:NH3:POS_00:OUT	XPP_NH3_POS_00_OUT	STATUS
□	4	4	XPP:DET:01:MPSFAULT	XPP_DET_01_MPSFAULT	STATUS
□	4	5	XPP:MPS:PLC_01:OK	XPP_MPS_PLC_01_OK	STATUS
□	4	6	AMO:MPS:PLC_01:OK	AMO_MPS_PLC_01_OK	STATUS
□	4	7	SXR:MPS:PLC_01:OK	SXR_MPS_PLC_01_OK	STATUS
□	4	8	SXR:GMD:VGC_01:OPN_DI	SXR_GMD_VGC_01_OPN_DI	POSITION
□	4	9	SXR:GMD:VGC_01:CLS_DI	SXR_GMD_VGC_01_CLS_DI	POSITION
□	4	10	XPP:SB2:VGC_02:OPN_DI	XPP_SB2_VGC_02_OPN_DI	POSITION
□	4	11	XPP:SB2:VGC_03:OPN_DI	XPP_SB2_VGC_03_OPN_DI	POSITION

30 Link Node 40

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	1	1	HXX:UM6:CVP_01:A	HXX_UM6_CVP_01_A	STATE
□	1	2	HXX:UM6:CVP_01:B	HXX_UM6_CVP_01_B	STATE
□	1	3	HXX:UM6:VGC_01:CLS_DI	HXX_UM6_VGC_01_CLS_DI	STATE
□	1	4	HXX:UM6:VGC_01:OPN_DI	HXX_UM6_VGC_01_OPN_DI	STATE
□	1	5	HXX:MXT:VGC_03:CLS_DI	HXX_MXT_VGC_03_CLS_DI	POSITION
□	1	6	HXX:MXT:VGC_03:OPN_DI	HXX_MXT_VGC_03_OPN_DI	POSITION
□	1	7	XRT:DIA:MMS_01:B	XRT_DIA_MMS_01_B	POSITION
□	1	8	CXI:DG1:MMS_03:A	CXI_DG1_MMS_03_A	POSITION
□	1	9	CXI:DG1:MMS_08:B	CXI_DG1_MMS_08_B	POSITION
□	1	12	CXI:DG2:MMS_06:B	CXI_DG2_MMS_06_B	POSITION
□	1	13	CXI:DG2:MMS_08:B	CXI_DG2_MMS_08_B	POSITION
□	1	14	CXI:DG2:MMS_09:B	CXI_DG2_MMS_09_B	POSITION
□	1	15	CXI:DG2:MMS_10:B	CXI_DG2_MMS_10_B	POSITION
□	1	16	CXI:SC3:VGC_01:OPN_DI	CXI_SC3_VGC_01_OPN_DI	POSITION
□	2	1	CXI:MPS:CFG:1	CXI_MPS_CFG_1	CONFID
□	2	2	CXI:MPS:CFG:2	CXI_MPS_CFG_2	CONFID
□	2	3	CXI:MPS:CFG:3	CXI_MPS_CFG_3	CONFID
□	2	4	CXI:MPS:CFG:4	CXI_MPS_CFG_4	CONFID
□	2	5	CXI:MPS:CFG:5	CXI_MPS_CFG_5	CONFID
□	2	6	CXI:MPS:CFG:6	CXI_MPS_CFG_6	CONFID
□	2	7	CXI:MPS:CFG:7	CXI_MPS_CFG_7	CONFID
□	2	8	CXI:MPS:PLC_01:OK	CXI_MPS_PLC_01_OK	STATUS
□	2	12	CXI:DG4:MMS_05:B	CXI_DG4_MMS_05_B	POSITION
□	2	13	CXI:DG4:MMS_03:B	CXI_DG4_MMS_03_B	POSITION
□	2	14	CXI:DIA:ATTEN:OK	CXI_DIA_ATTEN_OK	POSITION
□	2	15	HFA:SND:VGC_01:OPN_DI	HFA_SND_VGC_01_OPN_DI	POSITION
□	2	16	HF4:LAM:VGC_01:OPN_DI	HF4_LAM_VGC_01_OPN_DI	POSITION
□	3	1	HXX:LOM:VGC_01:CLS_DI	HXX_LOM_VGC_01_CLS_DI	STATE
□	3	2	HXX:LOM:VGC_01:OPN_DI	HXX_LOM_VGC_01_OPN_DI	STATE
□	3	3	HXX:DIA:VGC_01:CLS_DI	HXX_DIA_VGC_01_CLS_DI	STATE
□	3	4	HXX:DIA:VGC_01:OPN_DI	HXX_DIA_VGC_01_OPN_DI	STATE
□	3	5	HFX:DIA:VGC_02:OPN_DI	HFX_DIA_VGC_02_OPN_DI	POSITION
□	3	6	CXI:DG1:VGC_01:OPN_DI	CXI_DG1_VGC_01_OPN_DI	POSITION
□	3	7	CXI:DG1:VGC_02:OPN_DI	CXI_DG1_VGC_02_OPN_DI	POSITION
□	3	8	CXI:KB1:VGC_01:OPN_DI	CXI_KB1_VGC_01_OPN_DI	POSITION
□	3	9	CXI:KB1:VGC_02:OPN_DI	CXI_KB1_VGC_02_OPN_DI	POSITION
□	3	10	CXI:KB2:VGC_01:OPN_DI	CXI_KB2_VGC_01_OPN_DI	POSITION
□	3	12	CXI:DG2:VGC_01:OPN_DI	CXI_DG2_VGC_01_OPN_DI	POSITION

continued on next page...

. . . continued from previous page

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	3	13	CXI:DG2:VGC_02:OPN_DI	CXI_DG2_VGC_02_OPN_DI	POSITION
□	3	14	CXI:SC1:VGC_01:OPN_DI	CXI_SC1_VGC_01_OPN_DI	POSITION
□	3	15	CXI:SC1:VGC_02:OPN_DI	CXI_SC1_VGC_02_OPN_DI	POSITION
□	3	16	CXI:DSC:VGC_01:OPN_DI	CXI_DSC_VGC_01_OPN_DI	POSITION
□	4	1	CXI:SC2:VGC_02:OPN_DI	CXI_SC2_VGC_02_OPN_DI	POSITION
□	4	2	CXI:SC1:VGC_01:CLS_DI	CXI_SC1_VGC_01_CLS_DI	POSITION
□	4	3	CXI:DSC:VGC_01:CLS_DI	CXI_DSC_VGC_01_CLS_DI	POSITION
□	4	4	CXI:DET:01:MPSFAULT	CXI_DET_01_MPSFAULT	STATUS
□	4	5	CXI:DET:02:MPSFAULT	CXI_DET_02_MPSFAULT	STATUS
□	4	6	CXI:USR:01:MPSFAULT	CXI_USR_01_MPSFAULT	STATUS
□	4	7	CXI:USR:02:MPSFAULT	CXI_USR_02_MPSFAULT	STATUS
□	4	8	CXI:DG2:VGC_01:CLS_DI	CXI_DG2_VGC_01_CLS_DI	POSITION
□	4	9	CXI:DG2:VCG_02:CLS_DI	CXI_DG2_VCG_02_CLS_DI	POSITION
□	4	10	HXX:MXT:VGC_01:OPN_DI	HXX_MXT_VGC_01_OPN_DI	POSITION
□	4	11	HXX:MXT:VGC_02:OPN_DI	HXX_MXT_VGC_02_OPN_DI	POSITION
□	4	12	HXX:MXT:VGC_05:OPN_DI	HXX_MXT_VGC_05_OPN_DI	POSITION
□	4	13	CXI:KB2:VGC_02:OPN_DI	CXI_KB2_VGC_02_OPN_DI	POSITION
□	4	14	MEC:HXM:MMS_04:B	MEC_HXM_MMS_04_B	POSITION
□	4	15	HXX:HXM:MMS_01:B	HXX_HXM_MMS_01_B	POSITION
□	4	16	XCS:MPS:PLC_01:OK	XCS_MPS_PLC_01_OK	STATUS
□	5	1	STPR:XRT1:1:SH2OUT	STPR_XRT1_1_SH2OUT	STATE
□	5	2	STPR:XRT1:1:SH2IN	STPR_XRT1_1_SH2IN	STATE
□	5	3	STPR:XRT1:1:S5IN	STPR_XRT1_1_S5IN	POSITION
□	5	4	STPR:XRT1:1:S5OUT	STPR_XRT1_1_S5OUT	POSITION
□	5	5	STPR:FEH1:5:S5BIN	STPR_FEH1_5_S5BIN	POSITION
□	5	6	STPR:FEH1:5:S5BOUT	STPR_FEH1_5_S5BOUT	POSITION
□	5	7	STPR:XRT1:1:S4IN	STPR_XRT1_1_S4IN	POSITION
□	5	8	STPR:XRT1:1:S4OUT	STPR_XRT1_1_S4OUT	POSITION
□	5	9	HFX:UM6:STP_01:IN_DI	HFX_UM6_STP_01_IN_DI	POSITION
□	5	10	HFX:UM6:STP_01:OUT_DI	HFX_UM6_STP_01_OUT_DI	POSITION
□	5	11	HFX:DG2:STP_01:IN_DI	HFX_DG2_STP_01_IN_DI	POSITION
□	5	12	HFX:DG2:STP_01:OUT_DI	HFX_DG2_STP_01_OUT_DI	POSITION
□	5	13	HFX:DG2:VGC_01:OPN_DI	HFX_DG2_VGC_01_OPN_DI	POSITION
□	5	14	HFX:MON:VGC_01:OPN_DI	HFX_MON_VGC_01_OPN_DI	POSITION
□	5	15	MEC:MPS:PLC_01:OK	MEC_MPS_PLC_01_OK	STATUS
□	5	16	HFX:MON:VGC_02:OPN_DI	HFX_MON_VGC_02_OPN_DI	POSITION
□	6	1	CXI:KB2:VGC_02:CLS_DI	CXI_KB2_VGC_02_CLS_DI	POSITION
□	6	2	CXI:DSU:MMS_07:B	CXI_DSU_MMS_07_B	POSITION
□	6	3	HXX:HXM:MMS_01:INBEAM	HXX_HXM_MMS_01_INBEAM	POSITION
□	6	4	XCS:SB1:VGC_01:OPN_DI	XCS_SB1_VGC_01_OPN_DI	POSITION
□	6	5	XCS:SB1:VGC_01:CLS_DI	XCS_SB1_VGC_01_CLS_DI	POSITION

continued on next page. . .

. . . continued from previous page

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	6	6	XCS:SB1:VGC_02:OPN_DI	XCS_SB1_VGC_02_OPN_DI	POSITION
□	6	7	XCS:SB1:VGC_02:CLS_DI	XCS_SB1_VGC_02_CLS_DI	POSITION
□	6	8	XCS:SB2:VGC_01:OPN_DI	XCS_SB2_VGC_01_OPN_DI	POSITION
□	6	9	XCS:SB2:VGC_01:CLS_DI	XCS_SB2_VGC_01_CLS_DI	POSITION
□	6	10	XCS:SB:POS:MONO	XCS_SB_POS_MONO	POSITION
□	6	11	XCS:SB:POS:HARD	XCS_SB_POS_HARD	POSITION
□	6	12	XCS:SB1:STP_01:OPN_DI	XCS_SB1_STP_01_OPN_DI	POSITION
□	6	13	XCS:SB1:STP_01:CLS_DI	XCS_SB1_STP_01_CLS_DI	POSITION
□	6	14	XCS:USR:01:MPSFAULT	XCS_USR_01_MPSFAULT	STATUS
□	6	15	STPR:XRT1:1:S6IN	STPR_XRT1_1_S6IN	POSITION
□	6	16	STPR:XRT1:1:S6OUT	STPR_XRT1_1_S6OUT	POSITION

31 Link Node 41

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	1	1	MEC:DV5:VGC_01:OPN_DI	MEC_DV5_VGC_01_OPN_DI	POSITION
□	1	2	MEC:XT1:VGC_01:OPN_DI	MEC_XT1_VGC_01_OPN_DI	POSITION
□	1	3	MEC:XT1:MMS_01:B	MEC_XT1_MMS_01_B	POSITION
□	1	4	MEC:XT2:VGC_02:OPN_DI	MEC_XT2_VGC_02_OPN_DI	POSITION
□	1	5	MEC:XT2:VGC_03:OPN_DI	MEC_XT2_VGC_03_OPN_DI	POSITION
□	1	6	MEC:XT2:VGC_04:OPN_DI	MEC_XT2_VGC_04_OPN_DI	POSITION
□	1	7	MEC:XT2:VGC_05:OPN_DI	MEC_XT2_VGC_05_OPN_DI	POSITION
□	1	8	MEC:XT2:VGC_05:CLS_DI	MEC_XT2_VGC_05_CLS_DI	POSITION
□	1	9	MEC:XT2:VGC_06:OPN_DI	MEC_XT2_VGC_06_OPN_DI	POSITION
□	1	10	MEC:HXM:VGC_01:OPN_DI	MEC_HXM_VGC_01_OPN_DI	POSITION
□	1	11	CXI:DG4:VGC_01:OPN_DI	CXI_DG4_VGC_01_OPN_DI	POSITION
□	1	12	CXI:DG4:VGC_01:CLS_DI	CXI_DG4_VGC_01_CLS_DI	POSITION
□	1	13	MFX:MPS:PLC_VAC:OK	MFX_MPS_PLC_VAC_OK	STATUS
□	1	14	MEC:DV4:VGC_01:OPN_DI	MEC_DV4_VGC_01_OPN_DI	POSITION
□	1	15	MEC:BXL:VGC_01:OPN_DI	MEC_BXL_VGC_01_OPN_DI	POSITION
□	2	1	MFX:XRT:VGC:OUT_SUM	MFX_XRT_VGC_OUT_SUM	STATE
□	2	2	STPR:XRT:1:S45IN	STPR_XRT_1_S45IN	STATE
□	2	3	STPR:XRT:1:S45OUT	STPR_XRT_1_S45OUT	STATE
□	2	4	MFX:MPS:1:SUM	MFX_MPS_1_SUM	STATE
□	2	6	XCS:PBT:VGC:OUT_SUM	XCS_PBT_VGC_OUT_SUM	STATE

32 Link Node 42

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	1	7	COLL:BSYH:479:PCAPM_FLOW_SW	COLL_BSYH_479_PCAPM_FLOW_SW	STATE
□	1	9	EXPT:ESA0:1:EPS_STAT	EXPT_ESA0_1_EPS_STAT	STATE
□	1	11	BEND:BSY0:40:40B1_FLOW_SW	BEND_BSY0_40_40B1_FLOW_SW	STATE
□	1	13	PICM:ESA0:1:HV_PWR	PICM_ESA0_1_HV_PWR	STATE
□	2	1	COLL:BSYA:1490:FLOW_SW	COLL_BSYA_1490_FLOW_SW	STATE
□	2	2	COLL:BSYA:1700:FLOW_SW	COLL_BSYA_1700_FLOW_SW	STATE
□	2	3	SLIT:BSYA:1980:SL19_FLOW_SW	SLIT_BSYA_1980_SL19_FLOW_SW	STATE
□	2	5	VGFS:BSYA:1410:FSG22_OK	VGFS_BSYA_1410_FSG22_OK	STATE
□	2	8	QUAD:BSYA:1950:Q19_PS_ON	QUAD_BSYA_1950_Q19_PS_ON	STATE
□	2	9	COLL:BSYA:2470:V_FLOW_SW	COLL_BSYA_2470_V_FLOW_SW	STATE
□	2	10	COLL:BSYA:2470:H_FLOW_SW	COLL_BSYA_2470_H_FLOW_SW	STATE
□	2	11	COLL:BSYA:2410:FLOW_SW	COLL_BSYA_2410_FLOW_SW	STATE
□	2	12	COLL:BSYA:2060:FLOW_SW	COLL_BSYA_2060_FLOW_SW	STATE
□	2	13	COLL:BSYA:2600:FLOW_SW	COLL_BSYA_2600_FLOW_SW	STATE
□	2	14	COLL:BSYA:2990:FLOW_SW	COLL_BSYA_2990_FLOW_SW	STATE
□	2	15	COLL:BSYA:3710:FLOW_SW	COLL_BSYA_3710_FLOW_SW	STATE
□	2	16	BPMS:BSYA:2420:FLOW_SW	BPMS_BSYA_2420_FLOW_SW	STATE
□	3	1	BPMS:BSYA:2860:FLOW_SW	BPMS_BSYA_2860_FLOW_SW	STATE
□	3	2	BPMS:BSYA:3115:FLOW_SW	BPMS_BSYA_3115_FLOW_SW	STATE
□	3	3	COLL:ESA0:4120:FLOW_SW	COLL_ESA0_4120_FLOW_SW	STATE
□	3	4	VVPG:ESA0:4195:POSITION	VVPG_ESA0_4195_POSITION	STATE
□	3	5	VGFS:BSYA:3320:FSG29_OK	VGFS_BSYA_3320_FSG29_OK	STATE
□	3	6	PICM:ESA0:1:GAS_OK	PICM_ESA0_1_GAS_OK	STATE
□	3	7	MPS:ESA0:1:SEM_HV	MPS_ESA0_1_SEM_HV	STATE
□	3	9	QUAD:BSYA:2750:Q27_PS_ON	QUAD_BSYA_2750_Q27_PS_ON	STATE
□	3	10	QUAD:BSYA:2850:Q28_PS_ON	QUAD_BSYA_2850_Q28_PS_ON	STATE
□	3	11	QUAD:BSYA:2050:Q20_PS_ON	QUAD_BSYA_2050_Q20_PS_ON	STATE
□	3	12	XCOR:BSYA:2890:A28_PS_ON	XCOR_BSYA_2890_A28_PS_ON	STATE
□	3	13	YCOR:BSYA:2911:A29_PS_ON	YCOR_BSYA_2911_A29_PS_ON	STATE
□	3	14	XCOR:BSYA:3212:A32_PS_ON	XCOR_BSYA_3212_A32_PS_ON	STATE
□	3	15	YCOR:BSYA:3313:A33_PS_ON	YCOR_BSYA_3313_A33_PS_ON	STATE
□	4	1	KICK:BSY0:66:PM1_5_OFF	KICK_BSY0_66_PM1_5_OFF	STATE
□	4	2	BEND:BSYA:140:B1_2_PS_OFF	BEND_BSYA_140_B1_2_PS_OFF	STATE
□	4	3	STPR:BSYA:2275:ST22_IN_LIM	STPR_BSYA_2275_ST22_IN_LIM	STATE
□	4	4	STPR:BSYA:2930:ST29_IN_LIM	STPR_BSYA_2930_ST29_IN_LIM	STATE
□	4	5	STPR:BSYA:2275:ST22_OUT_LIM	STPR_BSYA_2275_ST22_OUT_LIM	STATE
□	4	6	STPR:BSYA:2930:ST29_OUT_LIM	STPR_BSYA_2930_ST29_OUT_LIM	STATE
□	4	7	SLIT:BSYA:2010:SL10_FT_IN	SLIT_BSYA_2010_SL10_FT_IN	STATE

continued on next page...

. . . continued from previous page

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	4	8	SLIT:BSYA:2010:SL10_FB_IN	SLIT_BSYA_2010_SL10_FB_IN	STATE
□	4	9	SLIT:BSYA:2010:SL10_RT_IN	SLIT_BSYA_2010_SL10_RT_IN	STATE
□	4	10	SLIT:BSYA:2010:SL10_RB_IN	SLIT_BSYA_2010_SL10_RB_IN	STATE
□	5	1	STPR:BSY0:89:IN_LIMSW_A	STPR_BSY0_89_IN_LIMSW_A	POSITION
□	5	2	STPR:BSY0:89:IN_LIMSW_B	STPR_BSY0_89_IN_LIMSW_B	POSITION
□	5	3	STPR:BSY0:89:OUT_LIMSW_A	STPR_BSY0_89_OUT_LIMSW_A	POSITION
□	5	4	STPR:BSY0:89:OUT_LIMSW_B	STPR_BSY0_89_OUT_LIMSW_B	POSITION
□	5	5	STPR:BSY0:90:IN_LIMSW_A	STPR_BSY0_90_IN_LIMSW_A	POSITION
□	5	6	STPR:BSY0:90:IN_LIMSW_B	STPR_BSY0_90_IN_LIMSW_B	POSITION
□	5	7	STPR:BSY0:90:OUT_LIMSW_A	STPR_BSY0_90_OUT_LIMSW_A	POSITION
□	5	8	STPR:BSY0:90:OUT_LIMSW_B	STPR_BSY0_90_OUT_LIMSW_B	POSITION
□	5	9	STPR:BSY0:88:IN_LIMSW_A	STPR_BSY0_88_IN_LIMSW_A	POSITION
□	5	10	STPR:BSY0:88:IN_LIMSW_B	STPR_BSY0_88_IN_LIMSW_B	POSITION
□	5	11	STPR:BSY0:88:OUT_LIMSW_A	STPR_BSY0_88_OUT_LIMSW_A	POSITION
□	5	12	BTM:BSY0:89:IN_LIMSW_A	BTM_BSY0_89_IN_LIMSW_A	POSITION
□	5	13	BTM:BSY0:89:IN_LIMSW_B	BTM_BSY0_89_IN_LIMSW_B	POSITION
□	5	14	BTM:BSY0:89:OUT_LIMSW_A	BTM_BSY0_89_OUT_LIMSW_A	POSITION
□	5	15	BTM:BSY0:89:OUT_CNTRL_A	BTM_BSY0_89_OUT_CNTRL_A	PPS_CNTRL
□	5	16	BTM:BSY0:89:OUT_CNTRL_B	BTM_BSY0_89_OUT_CNTRL_B	PPS_CNTRL
□	7	8	PICM:BSYA:2061:NO_TRIG	PICM_BSYA_2061_NO_TRIG	MISSED
□	9	1	PICM:BSYA:2061:LOSSL	PICM_BSYA_2061_LOSSL	THRESHOLD
□	9	2	PICM:BSYA:2061:LOSSH	PICM_BSYA_2061_LOSSH	THRESHOLD
□	10	1	PICM:BSYA:2120:LOSSL	PICM_BSYA_2120_LOSSL	THRESHOLD
□	10	2	PICM:BSYA:2120:LOSSH	PICM_BSYA_2120_LOSSH	THRESHOLD
□	11	1	PICM:BSYA:2220:LOSSL	PICM_BSYA_2220_LOSSL	THRESHOLD
□	11	2	PICM:BSYA:2220:LOSSH	PICM_BSYA_2220_LOSSH	THRESHOLD
□	12	1	PICM:BSYA:2321:LOSSL	PICM_BSYA_2321_LOSSL	THRESHOLD
□	12	2	PICM:BSYA:2321:LOSSH	PICM_BSYA_2321_LOSSH	THRESHOLD
□	13	1	PICM:BSYA:2411:LOSSL	PICM_BSYA_2411_LOSSL	THRESHOLD
□	13	2	PICM:BSYA:2411:LOSSH	PICM_BSYA_2411_LOSSH	THRESHOLD
□	14	1	PICM:BSYA:2472:LOSSL	PICM_BSYA_2472_LOSSL	THRESHOLD
□	14	2	PICM:BSYA:2472:LOSSH	PICM_BSYA_2472_LOSSH	THRESHOLD
□	15	1	PICM:BSYA:2473:LOSSL	PICM_BSYA_2473_LOSSL	THRESHOLD
□	15	2	PICM:BSYA:2473:LOSSH	PICM_BSYA_2473_LOSSH	THRESHOLD
□	16	1	PICM:BSYA:2474:LOSSL	PICM_BSYA_2474_LOSSL	THRESHOLD
□	16	2	PICM:BSYA:2474:LOSSH	PICM_BSYA_2474_LOSSH	THRESHOLD
□	17	1	PICM:BSYA:2475:LOSSL	PICM_BSYA_2475_LOSSL	THRESHOLD
□	17	2	PICM:BSYA:2475:LOSSH	PICM_BSYA_2475_LOSSH	THRESHOLD
□	18	1	PICM:BSYA:2520:LOSSL	PICM_BSYA_2520_LOSSL	THRESHOLD
□	18	2	PICM:BSYA:2520:LOSSH	PICM_BSYA_2520_LOSSH	THRESHOLD
□	19	1	PICM:BSYA:2601:LOSSL	PICM_BSYA_2601_LOSSL	THRESHOLD

continued on next page. . .

. . . continued from previous page

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	19	2	PICM:BSYA:2601:LOSSH	PICM_BSYA_2601_LOSSH	THRESHOLD
□	20	1	PICM:BSYA:2861:LOSSL	PICM_BSYA_2861_LOSSL	THRESHOLD
□	20	2	PICM:BSYA:2861:LOSSH	PICM_BSYA_2861_LOSSH	THRESHOLD
□	21	1	PICM:BSYA:2990:LOSSL	PICM_BSYA_2990_LOSSL	THRESHOLD
□	21	2	PICM:BSYA:2990:LOSSH	PICM_BSYA_2990_LOSSH	THRESHOLD
□	22	1	PICM:BSYA:3320:LOSSL	PICM_BSYA_3320_LOSSL	THRESHOLD
□	22	2	PICM:BSYA:3320:LOSSH	PICM_BSYA_3320_LOSSH	THRESHOLD
□	23	1	PICM:BSYA:3321:LOSSL	PICM_BSYA_3321_LOSSL	THRESHOLD
□	23	2	PICM:BSYA:3321:LOSSH	PICM_BSYA_3321_LOSSH	THRESHOLD
□	24	1	PICM:BSYA:3720:LOSSL	PICM_BSYA_3720_LOSSL	THRESHOLD
□	24	2	PICM:BSYA:3720:LOSSH	PICM_BSYA_3720_LOSSH	THRESHOLD
□	25	1	PICM:BSYA:3721:LOSSL	PICM_BSYA_3721_LOSSL	THRESHOLD
□	25	2	PICM:BSYA:3721:LOSSH	PICM_BSYA_3721_LOSSH	THRESHOLD
□	26	1	PICM:BSYA:3890:LOSSL	PICM_BSYA_3890_LOSSL	THRESHOLD
□	26	2	PICM:BSYA:3890:LOSSH	PICM_BSYA_3890_LOSSH	THRESHOLD

33 Link Node 43

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	1	1	KICK:BSY0:66:A_KIK	KICK_BSY0_66_A_KIK	STATUS
□	1	2	KICK:BSY0:66:A_KIKRB	KICK_BSY0_66_A_KIKRB	STATUS
□	7	1	KICK:BSY0:66:TA120MISS	KICK_BSY0_66_TA120MISS	MISSED
□	7	2	KICK:BSY0:66:TS30MISS	KICK_BSY0_66_TS30MISS	MISSED
□	7	3	KICK:BSY0:66:TA30MISS	KICK_BSY0_66_TA30MISS	MISSED
□	7	4	KICK:BSY0:66:TS120MISS	KICK_BSY0_66_TS120MISS	MISSED
□	7	5	KICK:BSY0:66:SPARE	KICK_BSY0_66_SPARE	MISSED
□	7	6	KICK:BSY0:66:THRSHUNDR	KICK_BSY0_66_THRSHUNDR	MISSED
□	7	7	KICK:BSY0:66:THRSHOVER	KICK_BSY0_66_THRSHOVER	MISSED

34 Link Node 44

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	7	8	EIOC:LTU1:MP12:NOTRIG	EIOC_LTU1_MP12_NOTRIG	MISSED
□	9	1	MPS:UND1:950:SX_HRMNC_ENERGY_L	MPS_UND1_950_SX_HRMNC_ENERGY_L	THRESHOLD
□	9	2	MPS:UND1:950:SX_HRMNC_ENERGY_H	MPS_UND1_950_SX_HRMNC_ENERGY_H	THRESHOLD
□	9	3	MPS:UND1:950:SX_SS_ENERGY_L	MPS_UND1_950_SX_SS_ENERGY_L	THRESHOLD
□	9	4	MPS:UND1:950:SX_SS_ENERGY_H	MPS_UND1_950_SX_SS_ENERGY_H	THRESHOLD
□	9	5	MPS:UND1:1640:HX_ENERGY_L	MPS_UND1_1640_HX_ENERGY_L	THRESHOLD
□	9	6	MPS:UND1:1640:HX_ENERGY_H	MPS_UND1_1640_HX_ENERGY_H	THRESHOLD
□	9	7	MIRR:FEE1:1560:ENERGY_L	MIRR_FEE1_1560_ENERGY_L	THRESHOLD
□	9	8	MIRR:FEE1:1560:ENERGY_H	MIRR_FEE1_1560_ENERGY_H	THRESHOLD

35 Link Node 125

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	4	9	VVFS:SLTH:130:POSITION	VVFS_SLTH_130_POSITION	STATE
□	4	12	VVPG:SLTH:115:POSITION	VVPG_SLTH_115_POSITION	STATE
□	4	13	VVPG:SLTH:291:POSITION	VVPG_SLTH_291_POSITION	STATE

36 Link Node 127

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	4	1	VVPG:BSYH:837:POSITION	VVPG_BSYH_837_POSITION	STATE
□	4	2	VVMG:LTUH:174:POSITION	VVMG_LTUH_174_POSITION	STATE
□	4	3	VVMG:LTUH:355:POSITION	VVMG_LTUH_355_POSITION	STATE
□	4	4	VVFS:LTUH:102:POSITION	VVFS_LTUH_102_POSITION	STATE
□	4	5	VVPG:LTUH:102:POSITION	VVPG_LTUH_102_POSITION	STATE
□	4	9	COLL:BSYH:892:TEMP	COLL_BSYH_892_TEMP	STATE
□	4	14	VVPG:LTUH:265:POSITION	VVPG_LTUH_265_POSITION	STATE
□	4	15	VVPG:BSYH:470:POSITION	VVPG_BSYH_470_POSITION	STATE
□	4	16	VVPG:BSYH:541:POSITION	VVPG_BSYH_541_POSITION	STATE

37 Link Node 129

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	4	1	COLL:LTUH:253:TEMP	COLL_LTUH_253_TEMP	STATE
□	4	2	COLL:LTUH:276:TEMP	COLL_LTUH_276_TEMP	STATE
□	4	3	KICK:LTUH:320:ON	KICK_LTUH_320_ON	STATE
□	4	4	KICK:LTUH:320:OFF	KICK_LTUH_320_OFF	STATE
□	4	5	STPR:BSYH:847:IN_LIMIT	STPR_BSYH_847_IN_LIMIT	POSITION
□	4	6	STPR:BSYH:847:OUT_LIMIT	STPR_BSYH_847_OUT_LIMIT	POSITION
□	4	7	STPR:CLTS:585:IN_LIMIT	STPR_CLTS_585_IN_LIMIT	POSITION
□	4	8	STPP:CLTS:585:OUT_LIMIT	STPP_CLTS_585_OUT_LIMIT	POSITION
□	16	9	KICK:LTUH:320:CURRENT	KICK_LTUH_320_CURRENT	THRESHOLD

38 Link Node 132

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	4	3	BEND:LTUH:220:ON	BEND_LTUH_220_ON	STATE
□	4	4	BEND:LTUH:220:OFF	BEND_LTUH_220_OFF	STATE
□	4	9	OTRS:LTUH:449:IN_LIMIT	OTRS_LTUH_449_IN_LIMIT	POSITION
□	4	10	OTRS:LTUH:449:OUT_LIMIT	OTRS_LTUH_449_OUT_LIMIT	POSITION
□	4	13	COLL:LTUH:393:TEMP	COLL_LTUH_393_TEMP	STATE
□	4	14	COLL:LTUH:452:TEMP	COLL_LTUH_452_TEMP	STATE
□	4	15	COLL:LTUH:475:TEMP	COLL_LTUH_475_TEMP	STATE
□	16	11	BEND:LTUH:220:CURRENT	BEND_LTUH_220_CURRENT	THRESHOLD

39 Link Node 134

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	3	1	VVMG:LTUH:774:POSITION	VVMG_LTUH_774_POSITION	STATE
□	3	9	VVPG:LTUH:435:POSITION	VVPG_LTUH_435_POSITION	STATE
□	3	10	VVPG:LTUH:580:POSITION	VVPG_LTUH_580_POSITION	STATE
□	3	11	VVPG:LTUH:725:POSITION	VVPG_LTUH_725_POSITION	STATE
□	3	12	VVPG:LTUH:757:POSITION	VVPG_LTUH_757_POSITION	STATE
□	3	13	VVPG:LTUH:999:POSITION	VVPG_LTUH_999_POSITION	STATE
□	3	14	VVMG:LTUH:505:POSITION	VVMG_LTUH_505_POSITION	STATE
□	3	15	VVMG:LTUH:670:POSITION	VVMG_LTUH_670_POSITION	STATE
□	3	16	VVMG:LTUH:742:POSITION	VVMG_LTUH_742_POSITION	STATE
□	4	9	YAGS:LTUH:743:IN_LIMIT	YAGS_LTUH_743_IN_LIMIT	POSITION
□	4	10	YAGS:LTUH:743:OUT_LIMIT	YAGS_LTUH_743_OUT_LIMIT	POSITION
□	4	11	OTRS:LTUH:745:IN_LIMIT	OTRS_LTUH_745_IN_LIMIT	POSITION
□	4	12	OTRS:LTUH:745:OUT_LIMIT	OTRS_LTUH_745_OUT_LIMIT	POSITION

40 Link Node 136

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	16	9	CBLM:UNDH:2375:I0	CBLM_UNDH_2375_I0	THRESHOLD
□	16	10	CBLM:UNDH:2475:I0	CBLM_UNDH_2475_I0	THRESHOLD
□	16	11	CBLM:UNDH:2575:I0	CBLM_UNDH_2575_I0	THRESHOLD
□	16	12	CBLM:UNDH:2675:I0	CBLM_UNDH_2675_I0	THRESHOLD

41 Link Node 138

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	16	9	CBLM:UNDH:1775:I0	CBLM_UNDH_1775_I0	THRESHOLD
□	16	10	CBLM:UNDH:1875:I0	CBLM_UNDH_1875_I0	THRESHOLD
□	16	11	CBLM:UNDH:1975:I0	CBLM_UNDH_1975_I0	THRESHOLD
□	16	12	CBLM:UNDH:2075:I0	CBLM_UNDH_2075_I0	THRESHOLD
□	16	13	CBLM:UNDH:2175:I0	CBLM_UNDH_2175_I0	THRESHOLD
□	16	14	CBLM:UNDH:2275:I0	CBLM_UNDH_2275_I0	THRESHOLD

42 Link Node 139

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	4	2	DUMP:LTUH:970:IN_LIMIT	DUMP_LTUH_970_IN_LIMIT	POSITION
□	4	3	DUMP:LTUH:970:OUT_LIMIT	DUMP_LTUH_970_OUT_LIMIT	POSITION
□	4	9	VVPG:UNDH:1288:POSITION	VVPG_UNDH_1288_POSITION	STATE
□	4	10	VVPG:UNDH:1998:POSITION	VVPG_UNDH_1998_POSITION	STATE
□	4	11	VVPG:UNDH:2198:POSITION	VVPG_UNDH_2198_POSITION	STATE
□	4	12	VVMG:UNDH:1498:POSITION	VVMG_UNDH_1498_POSITION	STATE
□	4	13	VVMG:UNDH:1698:POSITION	VVMG_UNDH_1698_POSITION	STATE
□	4	14	VVMG:UNDH:2498:POSITION	VVMG_UNDH_2498_POSITION	STATE
□	16	11	CBLM:UNDH:1375:I0	CBLM_UNDH_1375_I0	THRESHOLD
□	16	12	CBLM:UNDH:1475:I0	CBLM_UNDH_1475_I0	THRESHOLD
□	16	13	CBLM:UNDH:1575:I0	CBLM_UNDH_1575_I0	THRESHOLD
□	16	14	CBLM:UNDH:1675:I0	CBLM_UNDH_1675_I0	THRESHOLD

43 Link Node 140

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	16	9	CBLM:UNDH:2775:I0	CBLM_UNDH_2775_I0	THRESHOLD
□	16	10	CBLM:UNDH:2875:I0	CBLM_UNDH_2875_I0	THRESHOLD
□	16	11	CBLM:UNDH:2975:I0	CBLM_UNDH_2975_I0	THRESHOLD
□	16	12	CBLM:UNDH:3075:I0	CBLM_UNDH_3075_I0	THRESHOLD
□	16	13	CBLM:UNDH:3175:I0	CBLM_UNDH_3175_I0	THRESHOLD
□	16	14	CBLM:UNDH:3275:I0	CBLM_UNDH_3275_I0	THRESHOLD

44 Link Node 141

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	3	1	OTRS:DMPH:695:IN_LIMIT	OTRS_DMPH_695_IN_LIMIT	POSITION
□	3	2	OTRS:DMPH:695:OUT_LIMIT	OTRS_DMPH_695_OUT_LIMIT	POSITION
□	3	4	BEND:DMPH:395:ON	BEND_DMPH_395_ON	STATE
□	3	5	BEND:DMPH:395:OFF	BEND_DMPH_395_OFF	STATE
□	3	9	VVMG:UNDH:2843:POSITION	VVMG_UNDH_2843_POSITION	STATE
□	4	1	VVPG:UNDH:3798:POSITION	VVPG_UNDH_3798_POSITION	STATE
□	4	2	VVPG:UNDH:4598:POSITION	VVPG_UNDH_4598_POSITION	STATE
□	4	3	VVPG:UNDH:5196:POSITION	VVPG_UNDH_5196_POSITION	STATE
□	4	4	VVMG:UNDH:3298:POSITION	VVMG_UNDH_3298_POSITION	STATE
□	4	5	VVMG:UNDH:3598:POSITION	VVMG_UNDH_3598_POSITION	STATE
□	4	6	VVMG:UNDH:4098:POSITION	VVMG_UNDH_4098_POSITION	STATE
□	4	7	VVMG:UNDH:4398:POSITION	VVMG_UNDH_4398_POSITION	STATE
□	4	8	VVMG:UNDH:2838:POSITION	VVMG_UNDH_2838_POSITION	STATE
□	4	9	VVFS:DMPH:157:POSITION	VVFS_DMPH_157_POSITION	STATE
□	4	11	VVPG:DMPH:396:POSITION	VVPG_DMPH_396_POSITION	STATE
□	4	12	VVPG:DMPH:424:POSITION	VVPG_DMPH_424_POSITION	STATE
□	4	13	VVMG:DMPH:643:POSITION	VVMG_DMPH_643_POSITION	STATE
□	4	14	VVMG:DMPH:681:POSITION	VVMG_DMPH_681_POSITION	STATE
□	4	15	VVPG:UNDH:2798:POSITION	VVPG_UNDH_2798_POSITION	STATE
□	4	16	VVPG:UNDH:2998:POSITION	VVPG_UNDH_2998_POSITION	STATE
□	16	9	CBLM:UNDH:4575:I0	CBLM_UNDH_4575_I0	THRESHOLD
□	16	10	CBLM:UNDH:4675:I0	CBLM_UNDH_4675_I0	THRESHOLD
□	16	11	BEND:DMPH:395:CURRENT	BEND_DMPH_395_CURRENT	THRESHOLD

45 Link Node 143

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	16	9	CBLM:UNDH:3375:I0	CBLM_UNDH_3375_I0	THRESHOLD
□	16	10	CBLM:UNDH:3475:I0	CBLM_UNDH_3475_I0	THRESHOLD
□	16	11	CBLM:UNDH:3575:I0	CBLM_UNDH_3575_I0	THRESHOLD
□	16	12	CBLM:UNDH:3675:I0	CBLM_UNDH_3675_I0	THRESHOLD
□	16	13	CBLM:UNDH:3775:I0	CBLM_UNDH_3775_I0	THRESHOLD
□	16	14	CBLM:UNDH:3875:I0	CBLM_UNDH_3875_I0	THRESHOLD

46 Link Node 144

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	16	9	CBLM:UNDH:3975:I0	CBLM_UNDH_3975_I0	THRESHOLD
□	16	10	CBLM:UNDH:4075:I0	CBLM_UNDH_4075_I0	THRESHOLD
□	16	11	CBLM:UNDH:4175:I0	CBLM_UNDH_4175_I0	THRESHOLD
□	16	12	CBLM:UNDH:4275:I0	CBLM_UNDH_4275_I0	THRESHOLD
□	16	13	CBLM:UNDH:4375:I0	CBLM_UNDH_4375_I0	THRESHOLD
□	16	14	CBLM:UNDH:4475:I0	CBLM_UNDH_4475_I0	THRESHOLD

47 Link Node 145

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	4	1	HXU:CLASS:8:0	HXU_CLASS_8_0	STATE
□	4	2	HXU:CLASS:9:0	HXU_CLASS_9_0	STATE
□	4	3	HXU:CLASS:10:0	HXU_CLASS_10_0	STATE
□	4	4	HXU:CLASS:11:0	HXU_CLASS_11_0	STATE
□	4	5	HXU:CLASS:12:0	HXU_CLASS_12_0	STATE
□	4	6	HXU:CLASS:13:0	HXU_CLASS_13_0	STATE
□	4	7	HXU:CLASS:14:0	HXU_CLASS_14_0	STATE
□	4	8	HXU:CLASS:15:0	HXU_CLASS_15_0	STATE
□	4	9	HXU:CLASS:0:0	HXU_CLASS_0_0	STATE
□	4	10	HXU:CLASS:1:0	HXU_CLASS_1_0	STATE
□	4	11	HXU:CLASS:2:0	HXU_CLASS_2_0	STATE
□	4	12	HXU:CLASS:3:0	HXU_CLASS_3_0	STATE
□	4	13	HXU:CLASS:4:0	HXU_CLASS_4_0	STATE
□	4	14	HXU:CLASS:5:0	HXU_CLASS_5_0	STATE
□	4	15	HXU:CLASS:6:0	HXU_CLASS_6_0	STATE
□	4	16	HXU:CLASS:7:0	HXU_CLASS_7_0	STATE

48 Link Node 195

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	4	1	BEND:CLTS:765:ON	BEND_CLTS_765_ON	STATE
□	4	2	BEND:CLTS:765:OFF	BEND_CLTS_765_OFF	STATE
□	4	9	VVPG:CLTS:372:POSITION	VVPG_CLTS_372_POSITION	STATE
□	4	10	STPR:CLTS:585:TEMP	STPR_CLTS_585_TEMP	STATE
□	4	11	BEND:CLTS:280:ON	BEND_CLTS_280_ON	STATE
□	4	12	BEND:CLTS:280:OFF	BEND_CLTS_280_OFF	STATE
□	4	13	KICK:CLTS:185:ON	KICK_CLTS_185_ON	STATE
□	4	14	KICK:CLTS:185:OFF	KICK_CLTS_185_OFF	STATE
□	4	15	BEND:CLTS:180:ON	BEND_CLTS_180_ON	STATE
□	4	16	BEND:CLTS:180:OFF	BEND_CLTS_180_OFF	STATE
□	16	9	KICK:CLTS:185:CURRENT	KICK_CLTS_185_CURRENT	THRESHOLD
□	16	10	BEND:CLTS:280:CURRENT	BEND_CLTS_280_CURRENT	THRESHOLD
□	16	11	BEND:CLTS:180:CURRENT	BEND_CLTS_180_CURRENT	THRESHOLD
□	16	12	BEND:CLTS:765:CURRENT	BEND_CLTS_765_CURRENT	THRESHOLD

49 Link Node 196

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	4	4	COLL:SLTS:428:TEMP	COLL_SLTS_428_TEMP	STATE
□	4	9	VVFS:SLTS:130:POSITION	VVFS_SLTS_130_POSITION	STATE
□	4	12	VVPG:SLTS:115:POSITION	VVPG_SLTS_115_POSITION	STATE
□	4	13	VVPG:SLTS:581:POSITION	VVPG_SLTS_581_POSITION	STATE

50 Link Node 199

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	4	9	VVFS:LTUS:109:POSITION	VVFS_LTUS_109_POSITION	STATE
□	4	10	VVPG:LTUS:108:POSITION	VVPG_LTUS_108_POSITION	STATE
□	4	11	VVPG:LTUS:272:POSITION	VVPG_LTUS_272_POSITION	STATE
□	4	12	VVMG:LTUS:185:POSITION	VVMG_LTUS_185_POSITION	STATE
□	4	13	VVMG:LTUS:348:POSITION	VVMG_LTUS_348_POSITION	STATE
□	4	14	VVPG:BSYS:904:POSITION	VVPG_BSYS_904_POSITION	STATE
□	4	15	COLL:BSYS:859:TEMP	COLL_BSYS_859_TEMP	STATE

51 Link Node 202

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	4	1	COLL:LTUS:345:TEMP	COLL_LTUS_345_TEMP	STATE
□	4	2	COLL:LTUS:116:TEMP	COLL_LTUS_116_TEMP	STATE
□	4	3	KICK:LTUS:350:ON	KICK_LTUS_350_ON	STATE
□	4	4	KICK:LTUS:350:OFF	KICK_LTUS_350_OFF	STATE
□	4	5	STPR:BSYS:891:TEMP	STPR_BSYS_891_TEMP	STATE
□	4	6	STPR:BSYS:897:TEMP	STPR_BSYS_897_TEMP	STATE
□	4	10	STPR:BSYS:891:IN_LIMIT	STPR_BSYS_891_IN_LIMIT	POSITION
□	4	11	STPR:BSYS:891:OUT_LIMIT	STPR_BSYS_891_OUT_LIMIT	POSITION
□	4	16	COLL:LTUS:235:TEMP	COLL_LTUS_235_TEMP	STATE
□	16	9	KICK:LTUS:350:CURRENT	KICK_LTUS_350_CURRENT	THRESHOLD

52 Link Node 204

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	16	9	BEND:LTUS:175:CURRENT	BEND_LTUS_175_CURRENT	THRESHOLD
□	16	10	BEND:LTUS:525:CURRENT	BEND_LTUS_525_CURRENT	THRESHOLD

53 Link Node 205

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	4	1	BEND:LTUS:175:ON	BEND_LTUS_175_ON	STATE
□	4	2	BEND:LTUS:175:OFF	BEND_LTUS_175_OFF	STATE
□	4	3	BEND:LTUS:525:ON	BEND_LTUS_525_ON	STATE
□	4	4	BEND:LTUS:525:OFF	BEND_LTUS_525_OFF	STATE
□	4	6	COLL:LTUS:372:TEMP	COLL_LTUS_372_TEMP	STATE
□	4	9	VVPG:LTUS:442:POSITION	VVPG_LTUS_442_POSITION	STATE
□	4	10	VVPG:LTUS:586:POSITION	VVPG_LTUS_586_POSITION	STATE
□	4	11	VVMG:LTUS:451:POSITION	VVMG_LTUS_451_POSITION	STATE
□	4	12	VVMG:LTUS:505:POSITION	VVMG_LTUS_505_POSITION	STATE
□	4	13	VVMG:LTUS:552:POSITION	VVMG_LTUS_552_POSITION	STATE
□	4	14	VVMG:LTUS:656:POSITION	VVMG_LTUS_656_POSITION	STATE

54 Link Node 206

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	4	12	VVMG:LTUS:744:POSITION	VVMG_LTUS_744_POSITION	STATE
□	4	13	VVPG:LTUS:726:POSITION	VVPG_LTUS_726_POSITION	STATE
□	4	14	VVPG:LTUS:757:POSITION	VVPG_LTUS_757_POSITION	STATE

55 Link Node 208

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	4	9	VVPG:UNDS:1651:POSITION	VVPG_UNDS_1651_POSITION	STATE
□	4	10	VVPG:UNDS:2177:POSITION	VVPG_UNDS_2177_POSITION	STATE
□	4	11	VVPG:UNDS:2877:POSITION	VVPG_UNDS_2877_POSITION	STATE
□	4	13	DUMP:LTUS:972:IN_LIMIT	DUMP_LTUS_972_IN_LIMIT	POSITION
□	4	14	DUMP:LTUS:972:OUT_LIMIT	DUMP_LTUS_972_OUT_LIMIT	POSITION
□	4	15	VVMG:LTUS:802:POSITION	VVMG_LTUS_802_POSITION	STATE
□	4	16	VVMG:LTUS:827:POSITION	VVMG_LTUS_827_POSITION	STATE

56 Link Node 210

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	16	9	CBLM:UNDS:2610:I0	CBLM_UNDS_2610_I0	THRESHOLD
□	16	10	CBLM:UNDS:2710:I0	CBLM_UNDS_2710_I0	THRESHOLD
□	16	11	CBLM:UNDS:2810:I0	CBLM_UNDS_2810_I0	THRESHOLD
□	16	12	CBLM:UNDS:2910:I0	CBLM_UNDS_2910_I0	THRESHOLD
□	16	13	CBLM:UNDS:3010:I0	CBLM_UNDS_3010_I0	THRESHOLD
□	16	14	CBLM:UNDS:3110:I0	CBLM_UNDS_3110_I0	THRESHOLD

57 Link Node 213

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	3	9	BEND:DMPS:395:ON	BEND_DMPS_395_ON	STATE
□	3	10	BEND:DMPS:395:OFF	BEND_DMPS_395_OFF	STATE
□	4	1	VVPG:UNDS:3877:POSITION	VVPG_UNDS_3877_POSITION	STATE
□	4	2	VVPG:UNDS:4477:POSITION	VVPG_UNDS_4477_POSITION	STATE
□	4	3	VVPG:UNDS:5198:POSITION	VVPG_UNDS_5198_POSITION	STATE
□	4	6	OTRS:DMPS:695:IN_LIMIT	OTRS_DMPS_695_IN_LIMIT	POSITION
□	4	7	OTRS:DMPS:695:OUT_LIMIT	OTRS_DMPS_695_OUT_LIMIT	POSITION
□	4	9	VVFS:DMPS:157:POSITION	VVFS_DMPS_157_POSITION	STATE
□	4	11	VVPG:DMPS:396:POSITION	VVPG_DMPS_396_POSITION	STATE
□	4	12	VVPG:DMPS:424:POSITION	VVPG_DMPS_424_POSITION	STATE
□	4	13	VVMG:DMPS:643:POSITION	VVMG_DMPS_643_POSITION	STATE
□	4	14	VVMG:DMPS:681:POSITION	VVMG_DMPS_681_POSITION	STATE
□	4	15	VVPG:UNDS:3477:POSITION	VVPG_UNDS_3477_POSITION	STATE
□	4	16	VVPG:UNDS:3577:POSITION	VVPG_UNDS_3577_POSITION	STATE
□	16	10	CBLM:UNDS:3410:I0	CBLM_UNDS_3410_I0	THRESHOLD
□	16	11	CBLM:UNDS:3510:I0	CBLM_UNDS_3510_I0	THRESHOLD
□	16	12	CBLM:UNDS:3610:I0	CBLM_UNDS_3610_I0	THRESHOLD
□	16	13	CBLM:UNDS:3710:I0	CBLM_UNDS_3710_I0	THRESHOLD
□	16	14	CBLM:UNDS:3810:I0	CBLM_UNDS_3810_I0	THRESHOLD

58 Link Node 214

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	16	9	CBLM:UNDS:3910:I0	CBLM_UNDS_3910_I0	THRESHOLD
□	16	10	CBLM:UNDS:4010:I0	CBLM_UNDS_4010_I0	THRESHOLD
□	16	11	CBLM:UNDS:4110:I0	CBLM_UNDS_4110_I0	THRESHOLD
□	16	12	CBLM:UNDS:4210:I0	CBLM_UNDS_4210_I0	THRESHOLD
□	16	13	CBLM:UNDS:4310:I0	CBLM_UNDS_4310_I0	THRESHOLD
□	16	14	CBLM:UNDS:4410:I0	CBLM_UNDS_4410_I0	THRESHOLD

59 Link Node 215

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	16	9	CBLM:UNDS:4510:I0	CBLM_UNDS_4510_I0	THRESHOLD
□	16	10	CBLM:UNDS:4610:I0	CBLM_UNDS_4610_I0	THRESHOLD
□	16	11	CBLM:UNDS:4710:I0	CBLM_UNDS_4710_I0	THRESHOLD
□	16	12	CBLM:UNDS:3310:I0	CBLM_UNDS_3310_I0	THRESHOLD
□	16	14	CBLM:UNDS:3210:I0	CBLM_UNDS_3210_I0	THRESHOLD

60 Link Node 216

Verified	Card	Channel	PV Prefix	Device Name	Fault Name
□	4	1	SXU:CLASS:8:1	SXU_CLASS_8_1	STATE
□	4	2	SXU:CLASS:9:1	SXU_CLASS_9_1	STATE
□	4	3	SXU:CLASS:10:1	SXU_CLASS_10_1	STATE
□	4	4	SXU:CLASS:11:1	SXU_CLASS_11_1	STATE
□	4	5	SXU:CLASS:12:1	SXU_CLASS_12_1	STATE
□	4	6	SXU:CLASS:13:1	SXU_CLASS_13_1	STATE
□	4	7	SXU:CLASS:14:1	SXU_CLASS_14_1	STATE
□	4	8	SXU:CLASS:15:1	SXU_CLASS_15_1	STATE
□	4	9	SXU:CLASS:0:1	SXU_CLASS_0_1	STATE
□	4	10	SXU:CLASS:1:1	SXU_CLASS_1_1	STATE
□	4	11	SXU:CLASS:2:1	SXU_CLASS_2_1	STATE
□	4	12	SXU:CLASS:3:1	SXU_CLASS_3_1	STATE
□	4	13	SXU:CLASS:4:1	SXU_CLASS_4_1	STATE
□	4	14	SXU:CLASS:5:1	SXU_CLASS_5_1	STATE
□	4	15	SXU:CLASS:6:1	SXU_CLASS_6_1	STATE
□	4	16	SXU:CLASS:7:1	SXU_CLASS_7_1	STATE