VIPC664-ET

VME64x IndustryPack® Carrier

User's Manual

Manual Revision: 3 12/21/99 Hardware Revision: A

VIPC664-ET
VME64x IndustryPack Carrier

SBS GreenSpring Modular I/O
181 Constitution Drive
Menlo Park, CA 94025
(650) 327-1200
(650) 327-3808 FAX

Table of Contents

List of Figures

Product Description

The VIPC664-ET carrier is designed for use in VME64 extensions chassis. All I/O is via the rear panel per VME64 extensions spec. Seven VMEbus interrupt maps are now user selectable for easy interrupt configuration. Two Megabytes of flash memory, power check diagnostics and general purpose front panel display LEDs have all been added for this new generation of carriers.

Circuit design is based on the proven VIPC61x carriers upgraded to reliable CPLD technology. Construction is nearly all surface mount. All components are rated for extended temperatures, or better. The VME interface supports A16:D16:D8(EO) short I/O access and A32:D16:D8(EO) extended memory access. (Note: A24, D64 and D32 modes are NOT supported on this product) Configuration shunts have been greatly simplified for easy I/O and memory address selection. A local 16 MHz oscillator is used so the VIPC664-ET is not dependent on low quality VMEbus SYSCLK signals. The VIPC664-ET supports the 8 MHz IP interface only. Local reset is driven by a power monitoring, supervisory, IC for clean reliable reset and power cycling

All I/O is via the rear panel P0 and P2 connectors per VME64 extensions spec. Four IndustryPack slots are available for four single-size or two double size IndustryPacks. 200 lines of I/O (50 per slot) are connected to the VME64x backplane pins on the 5-row DIN P2 and 2 mm H.M. P0 connectors.

VIPC664-ET must be used with a rear panel transition module for I/O access. Please contact factory for details about compatible transition modules.

Seven interrupt modes are user selectable with a three-shunt group. All IndustryPack IRQ* signals can be mapped to a single VMEbus interrupt level. In single level mode VMEbus levels IRQ1* through IRQ6* can be user selected. The factory default is VMEbus level IRQ1*. For legacy applications, an interrupt map identical to the VIPC61x is also selectable. For non-interrupting applications, all interrupts can be disabled.

The VIPC664-ET provides several new on-board features. An on-board two Megabyte array of non-volatile flash memory is provided for general-purpose storage. Interrupt capabilities are available for interrupt driven flash programming and erasure. The power check circuit and status register verify power to the IndustryPack slots with both a visual LED indicator and software accessible status bit and an interrupt. An on-board register controls four red/green pairs of LEDs, on the front panel, for user defined diagnostic indicators. Four surface mount ACK* flash LEDs blink to visually confirm completed IP access cycles to individual slots.

Key Features

- VME64x rear panel I/O.
- Extended temperature components -40 to +85°C
- Easy interrupt and address configuration.
- User selectable VME interrupt level.
- 2 Megabytes on-board flash memory.
- Power check diagnostics.
- General purpose front panels LEDs.
- On-board clock generation.
- On-board supervisory IC for clean local reset.
- Self-resetting PTC fuses.

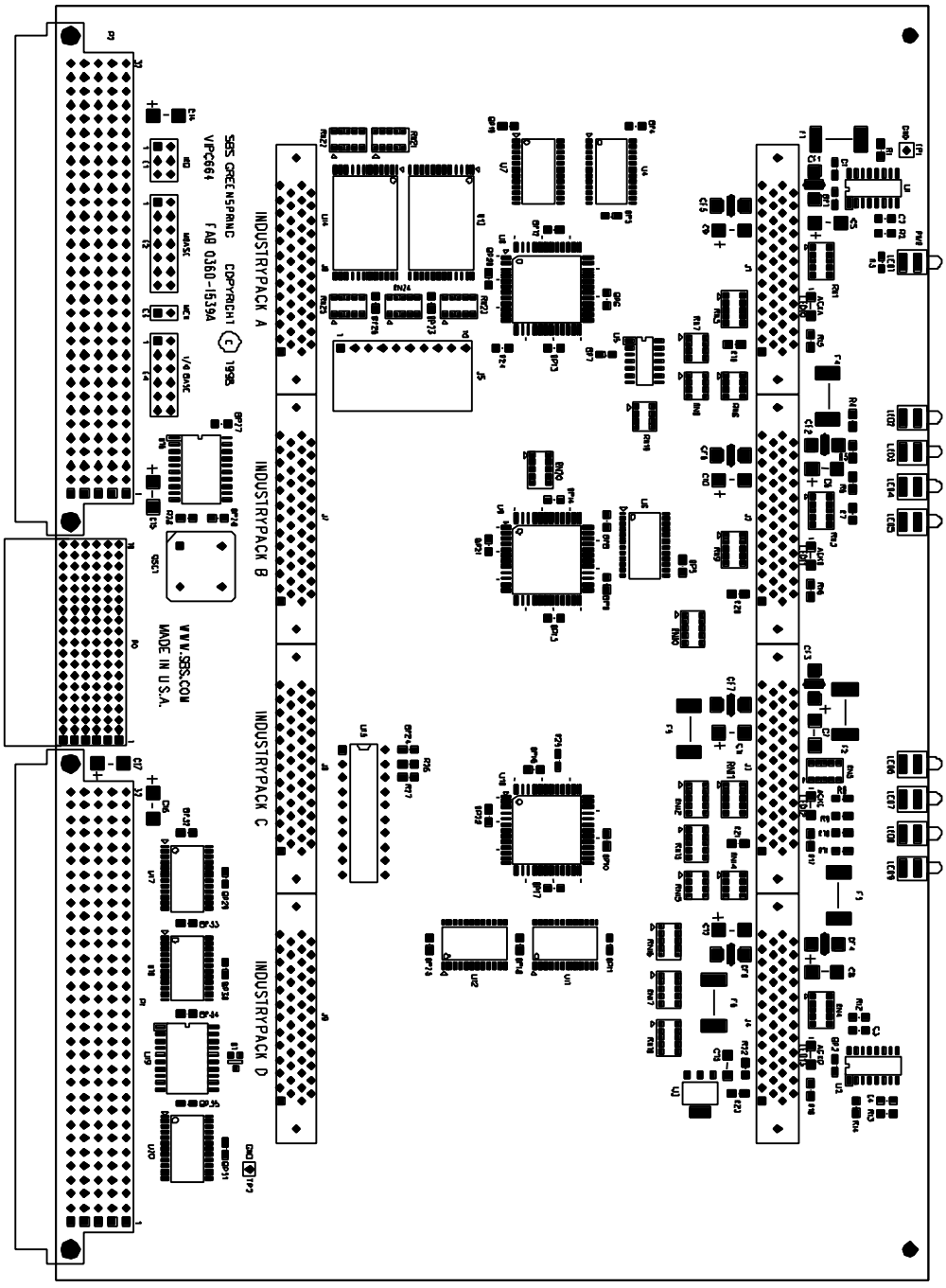

Figure 1 VIPC664-ET Assembly Drawing

Theory of Operation

VIPC664-ET provides access to up to four IndustryPacks. IndustryPack I/O and ID spaces are mapped into the VMEbus A16:D16:D8(EO) Short I/O space. IndustryPack memory is mapped into the VMEbus A32:D16:D8(EO) Extended memory space. VMEbus interrupts maintain the legacy mappings of the VIPC61x family, plus single level mappings are now also user selectable for interrupt intensive systems. The on-board registers of the carrier are appended to the short I/O space above the IndustryPack I/O and ID spaces. Similarly the on-board memory of the carrier is appended to the extended memory space above the IndustryPack memory spaces.

I/O Access

System designers will have to configure the VIPC664-ET for an I/O base address using shunt group E4. The default base address is 0x6000 in the VMEbus short I/O space. Each IndustryPack is allocated 128 bytes for I/O and 128 bytes for ID spaces. The on-board registers of the carrier are allocated 256 bytes in a similar manner. Although the VIPC664-ET is technically not an IndustryPack but it has an on-board ID space with information in a similar format. This can be used to track revisions and features of the carrier. The VIPC664-ET I/O base address must be located on a 0x1000 hex boundary. (I.E. 0x0000, 0x1000... 0x6000... etc.) The I/O map and E4 shunt settings are shown below. Further details of the on-board ID information and registers are given in the *On-board Features* section.

Address	Offset	Range	Assignment	Default	Size
I/O Base +	0x0000	0x0000 0x007F	IP A I/O Space	0x6000 0x607F	128 Bytes
I/O Base +	0x0080	0x0080 0x00FF	IP A ID Space	0x6080 0x60FF	128 Bytes
I/O Base +	0x0100	0x0100 0x017F	IP B I/O Space	0x6100 0x617F	128 Bytes
I/O Base +	0x0180	0x0180 0x01FF	IP B ID Space	0x6180 0x61FF	128 Bytes
I/O Base +	0x0200	0x0200 0x027F	IP C I/O Space	0x6200 0x627F	128 Bytes
I/O Base +	0x0280	0x0280 0x02FF	IP C ID Space	0x6280 0x62FF	128 Bytes
I/O Base +	0x0300	0x0300 0x037F	IP D I/O Space	0x6300 0x637F	128 Bytes
I/O Base +	0x0380	0x0380 0x03FF	IP D ID Space	0x6380 0x63FF	128 Bytes
I/O Base +	0x0400	0x0400 0x047F	Carrier on board registers	0x6400 0x647F	128 Bytes
I/O Base +	0x0480	0x0480 0x04FF	Carrier ID Space	0x6480 0x64FF	128 Bytes
I/O Base +	0x0500	0x0500 0x0FFF	Reserved	0x6500	2816 Bytes

Figure 2 VIPC664-ET I/O map
4096 bytes total

Shunt Location			Address Line	Default Setting	In = 0, Out = 1
E4.1	TO	E4.2	N/C	IN	0
E4.3	TO	E4.4	N/C	IN	0
E4.5	TO	E4.6	A12	IN	0
E4.7	TO	E4.8	A13	OUT	1
E4.9	TO	E4.10	A14	OUT	1
E4.11	TO	E4.12	A15	IN	0

Figure 3 I/O Address Settings
default I/O base address 0x6000

Memory Access

To use IndustryPacks with memory, system designers will have to enable the VIPC664-ET memory using the E3 shunt. And then configure the memory base address using shunt group E2. By default the memory access is enabled and the memory base address is D000'0000h in the VMEbus extended memory space.

To enable VIPC664-ET memory access install the E3 shunt. To disable VIPC664-ET memory access remove the E3 shunt. When the E3 shunt is removed VMEbus extended memory access cycles will be ignored by the VIPC664-ET and memory can be used for other purposes.

To configure a memory base address use the E2 shunt group. The amount of memory on IndustryPacks varies considerably. Some IndustryPacks have no memory at all. Be sure to review the User Manuals of installed IndustryPacks to determine if, and how much, memory is used by each. On the VIPC664-ET, each IndustryPack is allocated 8 Megabytes of memory space. IndustryPack memory spaces are therefore aligned on 8-Megabyte boundaries. IndustryPacks with less than 8 Megabytes will be aligned to the bottom of their respective sub-space and "padded" up to the next 8 Megabyte boundary. Accessing padded regions may produce ambiguous results. An additional 8 Megabytes is allocated for the on-board memory. This additional space is appended to the IndustryPack memory spaces at Base + 32 Megabytes. The VIPC664-ET memory base address must be located on a 64-Megabyte boundary. (i.e. D000'0000h, D400'0000h, D800'0000h etc) The shunt group E2 is used to select the memory base address. The memory map and E2 shunt settings are shown below. Further details of the on-board memory are given in the *On-board Features* section.

Default Memory Base	IP Slot	Memory Offset	Size	Default Range
D000’0000h	Slot A	0000’0000h	8 Megabyte	D000’0000h D07F’FFFFh
D000’0000h	Slot B	0080’0000h	8 Megabyte	D080’0000h D0FF’FFFFh
D000’0000h	Slot C	0100’0000h	8 Megabyte	D100’0000h D17F’FFFFh
D000’0000h	Slot D	0180’0000h	8 Megabyte	D180’0000h D1FF’FFFFh
D000’0000h	On board Flash	D200’0000h	2 Megabyte	D200’0000h D21F’FFFFh
D000’0000h	Reserved	D220’0000h	30 Megabyte	D220’0000h D3FF’FFFFh

Figure 4 Default Memory Map
default memory base address D000'0000h

Shunt Location			Address Line	Default	In = 0 Out = 1
E2.1	TO	E2.2	N/C	IN	0
E2.3	TO	E2.4	A26	IN	0
E2.5	TO	E2.6	A27	IN	0
E2.7	TO	E2.8	A29	OUT	1
E2.9	TO	E2.10	A29	IN	0
E2.11	TO	E2.12	A30	OUT	1
E2.13	TO	E2.14	A31	OUT	1

Figure 5 Memory Address Settings
default memory base address D000 0000h

Interrupts

To configure interrupts use the E1 shunt group. The first table below shows E1 options. On the VIPC664 all IndustryPack IRQ* signals can be mapped to a single VMEbus interrupt level. In single level mode VMEbus levels IRQ1* through IRQ6* can be user selected. The factory default is level IRQ1*. For non-interrupt applications, all interrupts can be Disabled completely.

One of the strengths of VMEbus in real time applications is its interrupt capability. The VMEbus defines seven prioritized interrupt levels. IRQ7* is the highest priority. IRQ1* is the lowest priority. IRQ7* is usually reserved for very important messages like catastrophic system failure. This effectively reduces the number of interrupt levels to six, which can be easily exceeded in any real world system. Single level IRQ mappings have proven to be popular in systems with lots of interrupt sources. Typically system designers will assign one interrupt level to one board or one class of interrupt source. Interrupt vectors (AKA Status IDs) can then be used to sort out the individual sources on the same level. This approach works well because the majority of IndustryPacks have user programmable interrupt vectors. And interrupt priority can be optimized with software. (Note the vector value is stored on the IP, not the carrier.)

SHUNT LOCATION			LOADING	VME IRQ LEVEL
E1.1	TO	E1.2	IN	VIPC61x MAP
E1.3	TO	E1.4	IN	See table below
E1.5	TO	E1.6	IN	
E1.1	TO	E1.2	OUT	IRQ1*
E1.3	TO	E1.4	IN	**DEFAULT**
E1.5	TO	E1.6	IN	
E1.1	TO	E1.2	IN	IRQ2*
E1.3	TO	E1.4	OUT	
E1.5	TO	E1.6	IN	
E1.1	TO	E1.2	OUT	IRQ3*
E1.3	TO	E1.4	OUT	
E1.5	TO	E1.6	IN	
E1.1	TO	E1.2	IN	IRQ4*
E1.3	TO	E1.4	IN	
E1.5	TO	E1.6	OUT	
E1.1	TO	E1.2	OUT	IRQ5*
E1.3	TO	E1.4	IN	
E1.5	TO	E1.6	OUT	
E1.1	TO	E1.2	IN	IRQ6*
E1.3	TO	E1.4	OUT	
E1.5	TO	E1.6	OUT	
E1.1	TO	E1.2	OUT	ALL
E1.3	TO	E1.4	OUT	INTERRUPTS
E1.5	TO	E1.6	OUT	DISABLED

Figure 6 E1 Interrupt Settings

IP Slot	IP IRQ Signal	VME IRQ Level
A	IRQ0*	IRQ1*
A	IRQ1*	IRQ2*
B	IRQ0*	IRQ3*
B	IRQ1*	IRQ4*
C	IRQ0*	IRQ5*
C	IRQ1*	IRQ6*
D	IRQ0*	IRQ7*
D	IRQ1*	N/C

Figure 7 VIPC61x Legacy Map

On-board Features

The VIPC664-ET offers several new onboard features including: Two Megabytes of flash memory, Power check circuit with status register, and User definable front panel LEDs.

The diagnostic module provides access to the onboard utilities. This is essentially a 5th IP with a control register, an interrupt structure, and an ID PROM. Access to the carrier power check status and flash RY/BY* signals is provided via the interrupt structure in the diagnostic module. The interrupt structure provides five registers to monitor, qualify and enable interrupts and a user programmable vector. This interrupt structure uses the standard format available on many GreenSpring industry packs.

Interrupts from on-board diagnostics are supported in single level VME modes only. Interrupts from on-board diagnostics are not defined in legacy interrupt mode and are disabled. The power check and Flash RY/BY* status can be polled at any time in all modes.

Base	Offset	Register	Description
Base +	0x400	CR	Control Register
Base +	0x402	INTD	Interrupt Data
Base +	0x404	INTP	Reserved
Base +	0x406	INTEN	Interrupt Enable
Base +	0x408	INTCLR	Interrupt Clear
Base +	0x40A	INTPEN	Interrupt Pending
Base +	0x40C	VECTOR	Interrupt Vector

Figure 8 VIPC664-ET on-board registers

CR: Control Register

The Control Register "CR" provides the four bits for utility and user diagnostic software. The default value of CR is 0. Setting a bit to 1 will light a green LED. Clearing a bit to 0 will light a red LED.

Bit	Description	bit = 1	bit = 0 (default)	Default	Access
CR.0	LED8 & LED9	LED9 = green, LED8 = off	LED9 = off, LED8 = red	0	R/W
CR.1	LED6 & LED7	LED7 = green, LED6 = off	LED7 = off, LED6 = red	0	R/W
CR.2	LED4 & LED5	LED5 = green, LED4 = off	LED4 = off, LED5 = red	0	R/W
CR.3	LED2 & LED3	LED3 = green, LED2 = off	LED3 = off, LED2 = red	0	R/W
CR.4				1	N/A
CR.5				1	N/A
CR.6				1	N/A
CR.7				1	N/A

Figure 9 CR Register

INTD: Interrupt data and Status Register

The interrupt data register "INTD" provides software direct access to the power check status and the flash RY/BY* signals. INTD can be polled at any time and in all interrupt modes. Data reads from INTD show the actual state of the signals when polled. INTD.0 monitors the power check circuit. If INTD.0 is 1 the carrier is OK and ready for use. If INTD.0 is 0 there is a power failure. INTD.1 indicates the status of the RD/BY* bit of the flash memory. This shows the flash memory erasure status. Reading a 1 from INTD.1 indicates that flash memory is ready for programming. Reading a 0 from INTD.1 indicates that a sector erasure is in progress and the flash should not be disturbed. INTD.1 can be polled at any time.

Bit	Description	bit = 1	bit = 0	Default	Access
INTD.0	Power Check	Power is OK, LED1 = Green	Power Failure, LED1 = off	1	R/O
INTD.1	Flash Ready	Flash Ready	Flash Busy (Erasing)	1	R/O
INTD.2				1	N/A
INTD.3				1	N/A
INTD.4				1	N/A
INTD.5				1	N/A
INTD.6				1	N/A
INTD.7				1	N/A

Figure 10 INTD Register

INTP: Interrupt Polarity Register

The interrupt polarity register "INTP" indicates the polarity of the interrupt triggering edge. For VIPC664-ET polarity is hardwired. The INTP register is provided for compatibility with other GreenSpring products.

Bit	Description	Bit = 0	Bit = 1	Default	Edge
INTP.0	Power Check	Power Fail	Power OK	0	Falling
INTP.1	Flash Ready	Flash busy	Flash Ready	1	Rising
INTP.2				1	N/A
INTP.3				1	N/A
INTP.4				1	N/A
INTP.5				1	N/A
INTP.6				1	N/A
INTP.7				1	N/A

Figure 11 INTP Register

INTEN: Interrupt Enable Register

The interrupt enable register "INTEN" enables interrupts from the carrier to the VMEbus backplane. Interrupts are disabled, by default, on power up and after reset. Writing a 0 to this register disables interrupts. Interrupt sources can be enabled individually by writing "1"s to either bit. INTEN.0 enables interrupts from the Power Check. INTEN.1 enables interrupts from the flash memory RY/BY* signal. If both INTEN.0 and INTEN.1 are set both interrupt sources are enabled. If simultaneous interrupts occur, the power check is top priority. See vector section for details.

Bit	Description	Bit = 0	Bit = 1	Default	Edge
INTEN.0	Power Check	Disabled	Enabled	0	R/W
INTEN.1	Flash Ready	Disabled	Enabled	0	R/W
INTEN.2				1	N/A
INTEN.3				1	N/A
INTEN.4				1	N/A
INTEN.5				1	N/A
INTEN.6				1	N/A
INTEN.7				1	N/A

Figure 12 INTEN Register

INTCLR: Interrupt Clear Register

The interrupt enable register "INTCLR" clears interrupts from the "INTPEN" register. Interrupts are latched into the interrupt pending register "INTPEN". INTCLR is a write only register, similar to a momentary push-button. Writing a 1 to INTCLR clears the INTPEN latches. Writing a 0 to this register has no effect. Because transient conditions on power up can be latched, default conditions for INTPEN cannot be guaranteed. It is recommended that interrupts be cleared, by writing 0xFF to INTCLR, before enabling interrupts.

Bit	Description	Default	Edge
INTCLR.0	Power Check	1	W/O
INTCLR.1	Flash Ready	1	W/O
INTCLR.2		1	N/A
INTCLR.3		1	N/A
INTCLR.4		1	N/A
INTCLR.5		1	N/A
INTCLR.6		1	N/A
INTCLR.7		1	N/A

Figure 13 INTCLR Register

INTPEN: Interrupt Pending Register

The interrupt pending register "INTPEN" indicates if an interrupt edge has occurred. Interrupts edges are detected and latched into this register and then, if the INTEN bit it set, passed on the VMEbus. Reading a 1 from this register indicates an interrupt is present and will be asserted if INTEN is set. Reading a 0 from this register indicates the interrupt source has not toggled. Because transient conditions on power up can be latched, default conditions for INTPEN cannot be guaranteed. It is recommended that interrupts be cleared, by writing 0xFF to INTCLR, before enabling interrupts.

Bit	Description	Default	Edge
INTPEN.0	Power Check	x	R/O
INTPEN.1	Flash Ready	x	R/O
INTPEN.2		1	N/A
INTPEN.3		1	N/A
INTPEN.4		1	N/A
INTPEN.5		1	N/A
INTPEN.6		1	N/A
INTPEN.7		1	N/A

Figure 14 INTPEN Register

VECTOR: Interrupt Vector register

The vector register has six user programmable bits. The lower two bits are used to encode the source of interrupts from VIPC664-ET. VECTOR.0 indicates the power check asserted the interrupt. VECTOR.1 indicates the flash asserted the interrupt. VECTOR.7 through VECTOR.2 are user programmable. The vector encoding will always give the power check priority. Simultaneous interrupts from the power check circuit and flash will result in the power check vector being asserted. In this condition the INTPEND register will show both interrupts are asserted.

VECTOR								Source
D7	D6	D5	D4	D3	D2	D1	D0	
X	X	X	X	X	X	0	0	reserved
X	X	X	X	X	X	0	1	Power Failure (priority)
X	X	X	X	X	X	1	0	Flash Ready
0	0	0	0	1	1	1	1	un-initialized vector

Figure 15 VECTOR Register
X = User Programmed

If the VECTOR register is not initialized by the user it will return the Motorola 68k family code for un-initialized interrupt vector, 0x0F. This un-initialized vector overrides the source encoding.

ID: ID PROM Registers

VIPC664-ET contains an ID PROM. The ID PROM aids in software auto configuration and management. The user's software, may verify the device it expects is actually installed at the location it expects, and is functional. The ID PROM contains the manufacturing revision level of the carrier and memory options. If a driver requires a particular revision be present, it may check for it directly. To be consistent with IndustryPacks, the VIPC664-ET ID PROM is located at the I/O base + 0x0480.

The ID PROM is implemented in the diagnostic module CPLD.

Offset	Description	Data
0x497	CRC (No Memory) 2 Megabytes Memory	 (0x6B) 0x03
0x495	No of bytes used	0x0C
0x493	Driver ID, high byte	0x00
0x491	Driver ID, low byte (0x00 = No Memory) 0x02 = 2 Megabytes Memory	 (0x00) 0x02
0x48F	Reserved	0x00
0x48D	Revision	0xA1
0x48B	Model No VIPC664-ET	0xB4
0x489	Manufacturer ID GreenSpring	0xF0
0x487	ASCII "C"	0x43
0x485	ASCII "A"	0x41
0x483	ASCII "P"	0x50
0x481	ASCII "I"	0x49

Figure 16 VIPC664 ID PROM Data

On-board Memory Programming

The VIPC664-ET features two Megabytes of AMD flash memory. Two AM29F800B-120 ICs are used in an array configuration. AMD data sheets explain in detail the techniques for programming these parts. Re-prints of the data sheets will be supplied with the carrier however, the best resource for up to date information is the World Wide Web. If you have web access browse the URLs listed below for the latest AM29F800 data.

http://www.amd.com

http://www.amd.com/products/products.html

http://www.amd.com/products/nvd/techdocs/techdocs.html

The AM29F800B features a bottom boot block. This feature divides the bottom sector of the flash into smaller portions that can be locked. Details of boot block architecture and programming are given in the AMD data sheets. Flash memory on VIPC664-ET is tested and erased in production. Users can implement the boot block feature as they see fit; however data may be erased if the board is returned for service.

The VIPC664-ET uses an array of two AM29F800 chips in byte mode; one IC for high byte [D15..D08] and one IC for low byte [D07..D00]. (i.e. BYTE* = 0 and A-1 is used). Because of this instruction codes must be written to both bytes. This can be done separately in byte access modes or simultaneously in word access modes. Also use the "byte" commands in tee AMD data sheet tables.

Programming the AMD Flash requires specific address and data combinations to access the flash controls. The VMEbus and IndustryPacks do not define an A0 address line. Byte strobes are used instead. To compensate for this, virtual command addresses specified in the AMD data sheets must be shifted. Address shifting is required for virtual command addresses only. Data accesses real locations should NOT be shifted. The table below shows the corrected addresses for VIPC664-ET.

Default Memory Base Address	VIPC664-ET Flash offset	AMD Control Address	VIPC664-ET Address
D000'0000h +	200'0000h	AAAAh	D201'5554h
D000'0000h +	200'0000h	5555h	D200'AAAAh

Figure 17 Flash Address Correction

Flash Memory Example

The following example of flash access on VIPC664-ET uses a debugger called RomBug. cw = change word. d = dump. In this example the base memory address of the VIPC664-ET is D200 0000h. The first example is a simple write sequence where the data word 0x1234 is written to an address of D200 0000h.

```
RomBug: cw d2015554 aaaa
0xD2015556   FFFF: .
RomBug: cw d200aaaa 5555
0xD200AAAC   FFFF: .
RomBug: cw d2015554 a0a0
0xD2015556   FFFF: .
RomBug: cw d2000000 1234
0xD2000002   FFFF: .
RomBug: d d2000000 10
0xD2000000    - 1234FFFF FFFFFFFF FFFFFFFF FFFFFFFF  .4..............
```

The second example is a sector erase where the first 16 kilobyte sector of the flash is erased.

```
RomBug: cw d2015554 aaaa
0xD2015556   FFFF: .
RomBug: cw d200aaaa 5555
0xD200AAAC   FFFF: .
RomBug: cw d2015554 8080
0xD2015556   FFFF: .
RomBug: cw d2015554 aaaa
0xD2015556   FFFF: .
RomBug: cw d200aaaa 5555
0xD200AAAC   FFFF: .
RomBug: cw d2000000 3030
0xD2000002   4C4C: .
RomBug: d d2000000 10
0xD2000000    - FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF  ................
```

Shunts by Location

VIPC664-ET has four groups of user configurable shunts. These are used to set the I/O base address, the memory base address and the interrupt scheme. For convenience the shunts are summarized below in numerical order. The default settings are shown in the first table below.

E4.11	E4.12	IN
E4.9	E4.10	OUT
E4.7	E4.8	OUT
E4.5	E4.6	IN
E4.3	E4.4	IN
E4.1	E4.2	IN
E3.1	E3.2	IN
E2.13	E2.14	OUT
E2.11	E2.12	OUT
E2.9	E2.10	IN
E2.7	E2.8	OUT
E2.5	E2.6	IN
E2.3	E2.4	IN
E2.1	E2.2	IN
E1.5	E1.6	IN
E1.3	E1.4	IN
E1.1	E1.2	OUT

Figure 18 DEFAULT SHUNT SETTINGS

E1 Shunt Group.

This group is used to select the interrupt map. See Interrupts section for details.

SHUNT LOCATION	LOADING	VME IRQ LEVEL
E1.1 TO E1.2	IN	VIPC61x MAP
E1.3 TO E1.4	IN	See table below
E1.5 TO E1.6	IN	
E1.1 TO E1.2	OUT	IRQ1*
E1.3 TO E1.4	IN	**DEFAULT**
E1.5 TO E1.6	IN	
E1.1 TO E1.2	IN	IRQ2*
E1.3 TO E1.4	OUT	
E1.5 TO E1.6	IN	
E1.1 TO E1.2	OUT	IRQ3*
E1.3 TO E1.4	OUT	
E1.5 TO E1.6	IN	
E1.1 TO E1.2	IN	IRQ4*
E1.3 TO E1.4	IN	
E1.5 TO E1.6	OUT	
E1.1 TO E1.2	OUT	IRQ5*
E1.3 TO E1.4	IN	
E1.5 TO E1.6	OUT	
E1.1 TO E1.2	IN	IRQ6*
E1.3 TO E1.4	OUT	
E1.5 TO E1.6	OUT	
E1.1 TO E1.2	OUT	ALL
E1.3 TO E1.4	OUT	INTERRUPTS
E1.5 TO E1.6	OUT	DISABLED

Figure 19 E1 Interrupt Config Shunts

IP Slot	IP IRQ Signal	VME IRQ Level
A	IRQ0*	IRQ1*
A	IRQ1*	IRQ2*
B	IRQ0*	IRQ3*
B	IRQ1*	IRQ4*
C	IRQ0*	IRQ5*
C	IRQ1*	IRQ6*
D	IRQ0*	IRQ7*
D	IRQ1*	N/C

Figure 20 VIPC61x Legacy Map

E2 Shunt Group.

This group is used to select a base memory address. See Memory Access section for details.

Shunt Location			Address Line	Default	In = 0 Out = 1
E2.1	TO	E2.2	N/C	IN	0
E2.3	TO	E2.4	A26	IN	0
E2.5	TO	E2.6	A27	IN	0
E2.7	TO	E2.8	A29	OUT	1
E2.9	TO	E2.10	A29	IN	0
E2.11	TO	E2.12	A30	OUT	1
E2.13	TO	E2.14	A31	OUT	1

Figure 21 E2 Memory Address Config Shunts default memory base address D000 0000h

E3 Shunt.

This shunt is used to enable memory. See Memory Access section for details.

E3	Memory
IN (default)	Enabled
OUT	Disabled

Figure 22 E3 Memory Enable Shunt

E4 Shunt Group.

This shunt is used to select an I/O base address. See I/O Access section for details.

Shunt Location			Address Line	Default Setting	In = 0, Out = 1
E4.1	TO	E4.2	N/C	IN	0
E4.3	TO	E4.4	N/C	IN	0
E4.5	TO	E4.6	A12	IN	0
E4.7	TO	E4.8	A13	OUT	1
E4.9	TO	E4.10	A14	OUT	1
E4.11	TO	E4.12	A15	IN	0

Figure 23 E4 I/O Address Config Shunts default I/O base address 0x6000

VME64x Pin Assignment

P1 ROW A	SIGNAL	P1 ROW B	SIGNAL	P1 ROW C	SIGNAL	P1 ROW D	SIGNAL	P1 ROW Z	SIGNAL
P1.A01	D00	P1.B01	N/C	P1.C01	D08	P1.D01	N/C	P1.Z01	N/C
P1.A02	D01	P1.B02	N/C	P1.C02	D09	P1.D02	N/C	P1.Z02	GND
P1.A03	D02	P1.B03	N/C	P1.C03	D10	P1.D03	N/C	P1.Z03	N/C
P1.A04	D03	P1.B04	BG0IN*	P1.C04	D11	P1.D04	N/C	P1.Z04	GND
P1.A05	D04	P1.B05	BG0OUT*	P1.C05	D12	P1.D05	N/C	P1.Z05	N/C
P1.A06	D05	P1.B06	BG1IN*	P1.C06	D13	P1.D06	N/C	P1.Z06	GND
P1.A07	D06	P1.B07	BG1OUT*	P1.C07	D14	P1.D07	N/C	P1.Z07	N/C
P1.A08	D07	P1.B08	BG2IN*	P1.C08	D15	P1.D08	N/C	P1.Z08	GND
P1.A09	GND	P1.B09	BG2OUT*	P1.C09	GND	P1.D09	N/C	P1.Z09	N/C
P1.A10	N/C	P1.B10	BG3IN*	P1.C10	N/C	P1.D10	N/C	P1.Z10	GND
P1.A11	GND	P1.B11	BG3OUT*	P1.C11	BERR*	P1.D11	N/C	P1.Z11	N/C
P1.A12	DS1*	P1.B12	N/C	P1.C12	RESET*	P1.D12	+3.3V	P1.Z12	GND
P1.A13	DS0*	P1.B13	N/C	P1.C13	LWORD*	P1.D13	N/C	P1.Z13	N/C
P1.A14	WRITE*	P1.B14	N/C	P1.C14	AM5	P1.D14	+3.3V	P1.Z14	GND
P1.A15	GND	P1.B15	N/C	P1.C15	A23	P1.D15	N/C	P1.Z15	N/C
P1.A16	DTACK*	P1.B16	AM0	P1.C16	A22	P1.D16	+3.3V	P1.Z16	GND
P1.A17	GND	P1.B17	AM1	P1.C17	A21	P1.D17	N/C	P1.Z17	N/C
P1.A18	AS*	P1.B18	AM2	P1.C18	A20	P1.D18	+3.3V	P1.Z18	GND
P1.A19	GND	P1.B19	AM3	P1.C19	A19	P1.D19	N/C	P1.Z19	N/C
P1.A20	IACK*	P1.B20	GND	P1.C20	A18	P1.D20	+3.3V	P1.Z20	GND
P1.A21	IACKIN*	P1.B21	N/C	P1.C21	A17	P1.D21	N/C	P1.Z21	N/C
P1.A22	IACKOUT*	P1.B22	N/C	P1.C22	A16	P1.D22	+3.3V	P1.Z22	GND
P1.A23	AM4	P1.B23	GND	P1.C23	A15	P1.D23	N/C	P1.Z23	N/C
P1.A24	A07	P1.B24	IRQ7*	P1.C24	A14	P1.D24	+3.3V	P1.Z24	GND
P1.A25	A06	P1.B25	IRQ6*	P1.C25	A13	P1.D25	N/C	P1.Z25	N/C
P1.A26	A05	P1.B26	IRQ5*	P1.C26	A12	P1.D26	+3.3V	P1.Z26	GND
P1.A27	A04	P1.B27	IRQ4*	P1.C27	A11	P1.D27	N/C	P1.Z27	N/C
P1.A28	A03	P1.B28	IRQ3*	P1.C28	A10	P1.D28	+3.3V	P1.Z28	GND
P1.A29	A02	P1.B29	IRQ2*	P1.C29	A09	P1.D29	N/C	P1.Z29	N/C
P1.A30	A01	P1.B30	IRQ1*	P1.C30	A08	P1.D30	+3.3V	P1.Z30	GND
P1.A31	-12V	P1.B31	N/C	P1.C31	+12V	P1.D31	N/C	P1.Z31	N/C
P1.A32	+5V	P1.B32	+5V	P1.C32	+5V	P1.D32	N/C	P1.Z32	GND

Figure 24 P1 pin assignment

I/O Pin Assignment

ROW A	SIG	ROW B	SIG	ROW C	SIG	ROW D	SIG	ROW Z	SIG
P2.A01	IOB41	P2.B01	+5V	P2.C01	IOB42	P2.D01	IOC47	P2.Z01	IOC46
P2.A02	IOB43	P2.B02	GND	P2.C02	IOB44	P2.D02	IOC48	P2.Z02	GND
P2.A03	IOB45	P2.B03	N/C	P2.C03	IOB46	P2.D03	IOC50	P2.Z03	IOC49
P2.A04	IOB47	P2.B04	A24	P2.C04	IOB48	P2.D04	IOB01	P2.Z04	GND
P2.A05	IOB49	P2.B05	A25	P2.C05	IOB50	P2.D05	IOB03	P2.Z05	IOB02
P2.A06	IOA01	P2.B06	A26	P2.C06	IOA02	P2.D06	IOB04	P2.Z06	GND
P2.A07	IOA03	P2.B07	A27	P2.C07	IOA04	P2.D07	IOB06	P2.Z07	IOB05
P2.A08	IOA05	P2.B08	A28	P2.C08	IOA06	P2.D08	IOB07	P2.Z08	GND
P2.A09	IOA07	P2.B09	A29	P2.C09	IOA08	P2.D09	IOB09	P2.Z09	IOB08
P2.A10	IOA09	P2.B10	A30	P2.C10	IOA10	P2.D10	IOB10	P2.Z10	GND
P2.A11	IOA11	P2.B11	A31	P2.C11	IOA12	P2.D11	IOB12	P2.Z11	IOB11
P2.A12	IOA13	P2.B12	GND	P2.C12	IOA14	P2.D12	IOB13	P2.Z12	GND
P2.A13	IOA15	P2.B13	+5V	P2.C13	IOA16	P2.D13	IOB15	P2.Z13	IOB14
P2.A14	IOA17	P2.B14	N/C	P2.C14	IOA18	P2.D14	IOB16	P2.Z14	GND
P2.A15	IOA19	P2.B15	N/C	P2.C15	IOA20	P2.D15	IOB18	P2.Z15	IOB17
P2.A16	IOA21	P2.B16	N/C	P2.C16	IOA22	P2.D16	IOB19	P2.Z16	GND
P2.A17	IOA23	P2.B17	N/C	P2.C17	IOA24	P2.D17	IOB21	P2.Z17	IOB20
P2.A18	IOA25	P2.B18	N/C	P2.C18	IOA26	P2.D18	IOB22	P2.Z18	GND
P2.A19	IOA27	P2.B19	N/C	P2.C19	IOA28	P2.D19	IOB24	P2.Z19	IOB23
P2.A20	IOA29	P2.B20	N/C	P2.C20	IOA30	P2.D20	IOB25	P2.Z20	GND
P2.A21	IOA31	P2.B21	N/C	P2.C21	IOA32	P2.D21	IOB27	P2.Z21	IOB26
P2.A22	IOA33	P2.B22	GND	P2.C22	IOA34	P2.D22	IOB28	P2.Z22	GND
P2.A23	IOA35	P2.B23	N/C	P2.C23	IOA36	P2.D23	IOB30	P2.Z23	IOB29
P2.A24	IOA37	P2.B24	N/C	P2.C24	IOA38	P2.D24	IOB31	P2.Z24	GND
P2.A25	IOA39	P2.B25	N/C	P2.C25	IOA40	P2.D25	IOB33	P2.Z25	IOB32
P2.A26	IOA41	P2.B26	N/C	P2.C26	IOA42	P2.D26	IOB34	P2.Z26	GND
P2.A27	IOA43	P2.B27	N/C	P2.C27	IOA44	P2.D27	IOB36	P2.Z27	IOB35
P2.A28	IOA45	P2.B28	N/C	P2.C28	IOA46	P2.D28	IOB37	P2.Z28	GND
P2.A29	IOA47	P2.B29	N/C	P2.C29	IOA48	P2.D29	IOB39	P2.Z29	IOB38
P2.A30	IOA49	P2.B30	N/C	P2.C30	IOA50	P2.D30	IOB40	P2.Z30	GND
P2.A31	+3.3V	P2.B31	GND	P2.C31	+3.3V	P2.D31	N/C	P2.Z31	+3.3V
P2.A32	+5V	P2.B32	+5V	P2.C32	+5V	P2.D32	N/C	P2.Z32	GND

Figure 25 P2 pin assignment

ROW A	SIG	ROW B	SIG	ROW C	SIG	ROW D	SIG	ROW E	SIG	ROW F	SIG
P0.A01	IOD01	P0.B01	IOD02	P0.C01	IOD03	P0.D01	IOD04	P0.E01	IOD05	P0.F01	GND
P0.A02	IOD06	P0.B02	IOD07	P0.C02	IOD08	P0.D02	IOD09	P0.E02	IOD10	P0.F02	GND
P0.A03	IOD11	P0.B03	IOD12	P0.C03	IOD13	P0.D03	IOD14	P0.E03	IOD15	P0.F03	GND
P0.A04	IOD16	P0.B04	IOD17	P0.C04	IOD18	P0.D04	IOD19	P0.E04	IOD20	P0.F04	GND
P0.A05	IOD21	P0.B05	IOD22	P0.C05	IOD23	P0.D05	IOD24	P0.E05	IOD25	P0.F05	GND
P0.A06	IOD26	P0.B06	IOD27	P0.C06	IOD28	P0.D06	IOD29	P0.E06	IOD30	P0.F06	GND
P0.A07	IOD31	P0.B07	IOD32	P0.C07	IOD33	P0.D07	IOD34	P0.E07	IOD35	P0.F07	GND
P0.A08	IOD36	P0.B08	IOD37	P0.C08	IOD38	P0.D08	IOD39	P0.E08	IOD40	P0.F08	GND
P0.A09	IOD41	P0.B09	IOD42	P0.C09	IOD43	P0.D09	IOD44	P0.E09	IOD45	P0.F09	GND
P0.A10	IOD46	P0.B10	IOD47	P0.C10	IOD48	P0.D10	IOD49	P0.E10	IOD50	P0.F10	GND
P0.A11	IOC01	P0.B11	IOC02	P0.C11	IOC03	P0.D11	IOC04	P0.E11	IOC05	P0.F11	GND
P0.A12	IOC06	P0.B12	IOC07	P0.C12	IOC08	P0.D12	IOC09	P0.E12	IOC10	P0.F12	GND
P0.A13	IOC11	P0.B13	IOC12	P0.C13	IOC13	P0.D13	IOC14	P0.E13	IOC15	P0.F13	GND
P0.A14	IOC16	P0.B14	IOC17	P0.C14	IOC18	P0.D14	IOC19	P0.E14	IOC20	P0.F14	GND
P0.A15	IOC21	P0.B15	IOC22	P0.C15	IOC23	P0.D15	IOC24	P0.E15	IOC25	P0.F15	GND
P0.A16	IOC26	P0.B16	IOC27	P0.C16	IOC28	P0.D16	IOC29	P0.E16	IOC30	P0.F16	GND
P0.A17	IOC31	P0.B17	IOC32	P0.C17	IOC33	P0.D17	IOC34	P0.E17	IOC35	P0.F17	GND
P0.A18	IOC36	P0.B18	IOC37	P0.C18	IOC38	P0.D18	IOC39	P0.E18	IOC40	P0.F18	GND
P0.A19	IOC41	P0.B19	IOC42	P0.C19	IOC43	P0.D19	IOC44	P0.E19	IOC45	P0.F19	GND

Figure 26 P0 pin assignment

Warranty and Repair

SBS GreenSpring Modular I/O warrants this product to be free from defects in workmanship and materials under normal use and service and in its original, unmodified condition, for a period of one year from the time of purchase. If the product is found to be defective within the terms of this warranty, SBS GreenSpring's sole responsibility shall be to repair, or at SBS GreenSpring's sole option to replace, the defective product. The product must be returned by the original customer, insured, and shipped prepaid to SBS GreenSpring. All replaced products become the sole property of SBS GreenSpring.

SBS GreenSpring's warranty of and liability for defective products is limited to that set forth herein. SBS GreenSpring disclaims and excludes all other product warranties and product liability, expressed or implied, including but not limited to any implied warranties of merchantability or fitness for a particular purpose or use, liability for negligence in manufacture or shipment of product, liability for injury to persons or property, or for any incidental or consequential damages.

SBS GreenSpring's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of SBS GreenSpring.

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. SBS GreenSpring will not be responsible for damages due to improper packaging of returned items. For service on SBS GreenSpring products not purchased directly from SBS GreenSpring contact your reseller. Products returned to SBS GreenSpring for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
SBS GreenSpring Modular I/O
181 Constitution Drive
Menlo Park, CA 94025
(415) 327-1200
FAX: (415) 327-3808
Internet Address support@greenspring.com

Specifications

VME64x Conformance	Revision IEEE P1024/D1.2 VITA 1.1-199x Draft 2.0 wcb
Form Factor	Double High, Single Slot, 6U
IndustryPack® Conformance	ANSI/VITA 4– 1995
I/O Pin Assignment Conformance	ANSI/VITA 4.1– 1997 Draft 0.8
Number of IndustryPacks	4 single-wide, or 2 double-wide
IP Memory Mapping	VME Access A32:D16:D8(EO) AM Codes: 09, 0A, 0D & 0E
Memory Size	40 Megabyte total footprint 8 Megabytes per IP 2 Megabytes flash on carrier
IP I/O Mapping	VME Access A16:D16:D8(EO) AM Codes: 29 & 2D
I/O Size	2 kilobytes
VMEbus Interrupts	user selectable VME levels IRQ1* - IRQ7* supported.
I/O Interconnect	Rear Panel Only P0 & P2 see tables
Indicators	4 green ACK* flash LEDs 1 Power check LED 4 red/green utility pairs.
Power Requirements	+5 V @ 600 mA typical +12V @ 40 mA -12V @ 60 mA Additional power is consumed by IndustryPacks
Environmental	Operating temp: -40°C to +85°C 5 to 95% relative humidity (non-condensing) Storage temp: -60°C to +95°C
Overall Size	6.5 in (165 mm) deep 9.2 in (233 mm) wide 0.66 in (17 mm) thick
Weight	12 oz. (340 grams)

Order Information

VIPC664-ET	Includes: VIPC664-ET VIPC664-ET User's Manual Technical Documentation: VIPC664-ETBill of Materials VIPC664-ETAssembly Drawing VIPC664-ETSchematics