Series IP470A Industrial I/O Pack
48-Channel Digital I/O Module With Interrupts

USER'S MANUAL

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IMPORTANT SAFETY CONSIDERATIONS

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

1.0 GENERAL INFORMATION

The Industrial I/O Pack (IP) Series IP470A module provides 48 channels of general-purpose digital inputs and outputs for interfacing to the VMEbus or PCI bus, according to your carrier board. Four units may be mounted on a single carrier board to provide up to 192 I/O points per system slot.

Inputs and outputs of this module are CMOS and TTL compatible. Each of the I/O lines can be used as either an input, an output, or an output with readback capability. Each I/O line has built-in event sense circuitry with programmable polarity and interrupt support. The inputs may also operate as independent event sense inputs (without interrupts). Outputs are open drain and may sink up to 15mA each. A 4.7K pull-up is provided for each drain and is installed in sockets on the board (SIP resistors) for easy removal or replacement. Inputs include hysteresis and programmable debounce. Interrupt, event, and debounce functionality applies to all 48 channels of this model. The IP470A utilizes state of the art Surface-Mounted Technology (SMT) to achieve its wide functionality and is an ideal choice for a wide range of industrial I/O applications that require a high-density, highly reliable, high-performance interface at a low cost.

MODEL	OPERATING TEMPERATURE RANGE
IP470A	0 to +70°C
IP470AE	-40 to +85°C

KEY IP470A FEATURES

- **High Channel Count** - Provides programmable monitor and control of 48 I/O points. Four units mounted on a carrier board provide 192 I/O points in a single VMEbus or PCI bus system slot.
- **High-Speed/0 Wait States** - No wait states are required for all read/write cycles (all cycles complete in 250ns) and hold states are supported.
- **Programmable Polarity Event Interrupts (all 48 channels)** - Interrupts are software programmable for positive (low-to-high) or negative (high-to-low) input level transitions on all 48 channels. Using two channels per input signal, change-of-state transitions may also be configured for up to 24 inputs.
- **Programmable Debounce (all 48 channels)** - The event sense input circuitry includes programmable debounce times for all 48 channels. Debounce time is the duration of time that must pass before the input transition is recognized as valid. This helps prevent false events and increases noise immunity.
- **CMOS (TTL Compatible)** - Input threshold is at TTL levels and includes hysteresis. I/O circuitry uses CMOS technology. As such, output levels are CMOS compatible, even while sinking high current (see Specifications Section).

- **Output Readback Function** - Readback buffers are provided that allow the output port registers to be read back.
- **High Output Sink Capability** - All outputs may sink up to 15mA with a voltage drop ≤ 0.5V.
- **Outputs are "Glitch-Free" -** Unlike some competitive units, the outputs of this device do not "glitch" (momentarily turn on) upon power-up or power-down for steady and safe control.
- **Open Drain Outputs Include Pull-ups -** All outputs include 4.7K pull-ups to +5V in the form of resistor SIP's installed in sockets on the board for convenient removal or replacement.
- **Overvoltage Protection** - Individual I/O channels include over-voltage clamps for increased ESD & transient protection.
- **High Impedance Inputs** - High impedance inputs minimize input current and loading of the input source.
- **No Configuration Jumpers or Switches** - All configuration is performed through software commands with no internal jumpers to configure or switches to set.
- **Industry Compatible P2 Pinouts** - the field side P2 pinout configuration of this module is common to similar models and directly compatible with industry accepted digital I/O cards, screw termination panels, and electromechanical & solid-state relay boards (consult factory for recommendations).

INDUSTRIAL I/O PACK INTERFACE FEATURES

- **High density -** Single-size, industry standard, IP module footprint. Four units mounted on a carrier board provide up to 128 isolated input points in a single system slot. Both VMEbus and PCI bus carriers are supported.
- **Local ID** - Each IP module has its own 8-bit ID ROM which is accessed via data transfers in the "ID Read" space.
- **8-bit I/O** - Port register Read/Write is performed through 8-bit data transfer cycles in the IP module I/O space.
- **High Speed with No Wait States** - Access times for all data transfer cycles are described in terms of "wait" states--0 wait states are required for all read and write operations of this model. See Specifications section for detailed information.

SIGNAL INTERFACE PRODUCTS

This IP module will mate directly to any industry standard IP carrier board. Acromag's AVME9630/9668 3U/6U non-intelligent VMEbus carrier boards and Acromag's APC862x series PCI bus carrier boards are supported. A wide range of other Acromag IP modules are available to serve your signal conditioning and interface needs.

Cables:

Model 5025-551-X (Shielded Cable) or Model 5025-550-X (Non-Shielded Cable): A Flat 50-pin cable with female connectors at both ends for connecting to the AVME9630/9660, other compatible carrier boards, or Model 5025-552 termination panels. The shielded cable is recommended for optimum performance with precision analog I/O applications, while the unshielded cable is recommended for digital I/O. The cables are available in 4, 7, or 10 feet lengths. Custom lengths (12 feet maximum) are available upon request.

Termination Panel:

Model 5025-552: DIN-rail mountable panel provides 50 screw terminals for universal field I/O termination. Connects to Acromag AVME9630/9668, or other compatible carrier boards, via flat 50-pin ribbon cable (Model 5025-550-X or 5025-551-X).

Transition Module:

Model TRANS-GP: This module repeats field I/O connections of IP modules A through D for rear exit from the card cage. It is available for use in card cages, which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. Connects to AVME9630/9660 boards via a flat 50-pin ribbon cable within the card cage (cable Model 5025-550-X or 5025-551-X).

IP MODULE Win32 DRIVER SOFTWARE

Acromag provides a software product (sold separately) to facilitate the development of Windows (98/Me/2000/XP®) applications accessing Industry Pack modules installed on Acromag PCI Carrier Cards and CompactPCI Carrier Cards. This software (Model IPSW-API-WIN) consists of low-level drivers and Windows 32 Dynamic Link Libraries (DLLS) that are compatible with a number of programming environments including Visual C++, Visual Basic, Borland C++ Builder and others. The DLL functions provide a high-level interface to the carriers and IP modules eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers.

IP MODULE VXWorks SOFTWARE

Acromag provides a software product (sold separately) consisting of board VxWorks® software. This software (Model IPSW-API-VXW) is composed of VxWorks® (real time operating system) libraries for all Acromag IP modules and carriers including the AVME9670, AVME9660/9630, APC8620A/21A, ACPC8630/35, and ACPC8625. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag PCI boards.

IP MODULE QNX SOFTWARE

Acromag provides a software product (sold separately) consisting of board QNX® software. This software (Model IPSW-API-QNX) is composed of QNX® (real time operating system) libraries for all Acromag IP modules and carriers including the AVME9670, AVME9660/9630, APC8620A/21A, ACPC8630/35, and ACPC8625. The software supports X86 PCI bus only and is implemented as library of "C" functions. These functions link with existing user code to make possible simple control of all Acromag IP modules and carriers.

2.0 PREPARATION FOR USE

UNPACKING AND INSPECTION

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static-sensitive components and should only be handled at a static-safe workstation.

CARD CAGE CONSIDERATIONS

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the carrier board, plus the installed IP modules, within the voltage tolerances specified.

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

The dense packing of the IP modules to the carrier board restricts airflow within the card cage and is cause for concern. Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air filtering.

BOARD CONFIGURATION

Power should be removed from the board when installing IP modules, cables, termination panels, and field wiring. Refer to Mechanical Assembly Drawing 4501-434 and your IP module documentation for configuration and assembly instructions. Model IP470A digital I/O boards have no hardware jumpers or switches to configure. However, 4.7KΩ pull-up resistor SIP's are installed in sockets on the board, and these may be easily changed or removed where required (see Drawing 4502-057).

CONNECTORS

IP Field I/O Connector (P2)

P2 provides the field I/O interface connections for mating IP modules to the carrier board. P2 is a 50-pin female receptacle header, which mates to the male connector of the carrier board (AMP 173280-3 or equivalent). This provides excellent connection integrity and utilizes gold plating in the mating area. Threaded metric M2 screws and spacers are supplied with the module to provide additional stability for harsh environments (see Mechanical Assembly Drawing 4501-434). The field and logic side connectors are keyed to avoid incorrect assembly.

P2 pin assignments are unique to each IP model (see Table 2.1) and normally correspond to the pin numbers of the field I/O interface connector on the carrier board (you should verify this for your carrier board).

Table 2.1: IP470A Field I/O Pin Connections (P2)

Pin Description		Number	Pin Description		Number
	I/O00	8		I/O24	32
P	I/O01	7	P	I/O25	31
O	I/O02	6	O	I/O26	30
R	I/O03	5	R	I/O27	29
T	I/O04	4	T	I/O28	28
	I/O05	3		I/O29	27
0	I/O06	2	3	I/O30	26
	I/O07	1		I/O31	25
	I/O08	16		I/O32	40
P	I/O09	15	P	I/O33	39
O	I/O10	14	O	I/O34	38
R	I/O11	13	R	I/O35	37
T	I/O12	12	T	I/O36	36
	I/O13	11		I/O37	35
1	I/O14	10	4	I/O38	34
	I/O15	09		I/O39	33
	I/O16	24		I/O40	48
P	I/O17	23	P	I/O41	47
O	I/O18	22	O	I/O42	46
R	I/O19	21	R	I/O43	45
T	I/O20	20	T	I/O44	44
	I/O21	19		I/O45	43
2	I/O22	18	5	I/O46	42
	I/O23	17		I/O47	41
				+5V OUT[1]	49
				COMMON	50

Note:

1. By default, pin 49 of P2 is connected to the +5V supply of the IP module, but may be optionally connected to common (or opened) by repositioning surface mount resistor R72 (see Drawing 4502-057 for location). The +5V connection is in series with fuse F1 (2A Littelfuse 245002 or equivalent).

Note that the I/O points of this module are assembled in groups of eight. Each group of eight I/O lines is referred to as a port. Registers at port addresses 0-5 control and monitor I/O lines 00-47. Individual I/O ports may be masked from writes to the port when the port is used for input. This helps prevent contention errors. Further, event polarities may be defined as positive (low-to-high), or negative (high-to-low) for individual nibbles (groups of 4 I/O lines, or half ports). Outputs of this device are open drain and operate using low-level true (active-low) logic . The pinouts of P2 are arranged to be compatible with

similar industry models and are directly compatible with industry accepted I/O panels, termination panels, and relay racks. Consult the factory for information on compatible products.

I/O Noise and Grounding Considerations

The IP470A is non-isolated between the logic and field I/O grounds since output common is electrically connected to the IP module ground. Consequently, the field I/O connections are not isolated from the carrier board and backplane. Special care has been taken in the design of this module to help minimize the negative effects of ground bounce, impedance drops, and switching transients. However, care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections.

This device is capable of switching many channels at high total currents. Additionally, the nature of the IP interface is inherently inductive. I/O channels have special circuitry to help protect the device from ESD, over-voltage, and switching transients, within limitations. However, when switching inductive loads, it is important that careful consideration be given to the use of snubber devices to shunt the reverse emf that develops when the current through an inductor is interrupted. Filtering and bypassing at the load may also be necessary. Additionally, proper grounding with thick conductors is essential. Interface cabling and ground wiring should be kept as short as possible. For outputs of this device, the 4.7KΩ pull-up resistors provide only limited digital drive capability. Likewise, outputs are intended to sink only 15mA or less. As such, the use of an interposing device may be required for controlling or isolating the load, or to provide additional system protection. The output pull-up resistor SIP's are installed in sockets on the board allowing their values to be adjusted for greater drive capability if required (see Drawing 4502-057).

The signal ground connection at the I/O ports is common to the IP interface ground, which is typically common to safety (chassis) ground when mounted on a carrier board and inserted in a backplane. As such, be careful not to attach I/O ground to safety ground via any device connected to these ports, or a ground loop will be produced, and this may adversely affect operation.

IP Logic Interface Connector (P1)

P1 of the IP module provides the logic interface to the mating connector on the carrier board. The pin assignments of P1 are standard for all IP modules according to the Industrial I/O Pack Specification (see Table 2.2). This connector is a 50-pin female receptacle header , which mates to the male connector of the carrier board. This provides excellent connection integrity and utilizes gold plating in the mating area. Threaded metric M2 screws and spacers are supplied with the IP module to provide additional stability for harsh environments (see Drawing 4501-434 for assembly details). Field and logic side connectors are keyed to avoid incorrect assembly.

Table 2.2: Standard Logic Interface Connections (P1)

Pin Description	Number	Pin Description	Number
GND	1	GND	26
CLK	2	+5V	27
Reset*	3	R/W*	28
D00	4	IDSEL*	29
D01	5	***DMAReq0****	30
D02	6	MEMSEL*	31
D03	7	***DMAReq1****	32
D04	8	IntSel*	33
D05	9	***DMAck0****	34
D06	10	IOSEL*	35
D07	11	***RESERVED***	36
D08	12	A1	37
D09	13	***DMAEnd****	38
D10	14	A2	39
D11	15	***ERROR****	40
D12	16	A3	41
D13	17	INTReq0*	42
D14	18	A4	43
D15	19	***INTReq1****	44
BS0*	20	A5	45
BS1*	21	***STROBE****	46
-12V	22	A6	47
+12V	23	ACK*	48
+5V	24	***RESERVED***	49
GND	25	GND	50

An Asterisk (*) is used to indicate an active-low signal.
BOLD ITALIC Logic Lines are NOT USED by this IP Model.

3.0 PROGRAMMING INFORMATION

ADDRESS MAPS

This board is addressable in the Industrial Pack I/O space to control the input/output configuration, control, and status monitoring or 48 digital I/O channels. Each of the I/O points can be configured as either an input, an output, or an output with readback capability. Interrupt, event, and debounce capability applies to all 48 channels.

This board operates in two modes: Standard Mode and Enhanced Mode. Standard Mode provides simple monitor and control of 48 digital I/O lines. In Standard Mode, each I/O line is configured as either an input, an output, or an output with readback capability. Data is read from or written to one of eight groups (ports) as designated by the address and read and write signals. A Mask Register is used to disable writes to I/O ports designated as inputs to prevent possible contention between an external input signal and the output mosfet. Enhanced Mode includes the same functionality of Standard Mode, but adds access to 48 additional event sense inputs connected to each I/O point of ports 0-5 . Thus, the Enhanced Mode allows event-triggered interrupts to be generated. Selectable hardware debounce may also be applied in Enhanced Mode for noise free edge-detection of incoming signals.

Memory is organized and addressed in separate banks of eight registers or ports (eight ports to a bank). The Standard Mode of operation addresses the first group of 8 registers or ports (ports 0-5 for reading/writing I/O0-47, Port 6 which is not used,

and Port 7 which is the Mask Register). If the Enhanced Mode is selected, then 3 additional banks of 8 registers are accessed to cover the additional functionality in this mode. The first bank of the Enhanced Mode (bank 0) is similar in operation to the Standard Mode. The second bank (bank 1) provides event sense and interrupt control. The third bank is used to configure the debounce circuitry to be applied to input channels in the Enhanced Mode. Two additional registers are provided to enable the interrupt request line, generate a software reset, and store the interrupt vector.

The I/O space may be as large as 64, 16-bit words (128 bytes) using address lines A1..A6, but the IP470A uses only a portion of this space. The I/O space address map for the IP470A is shown in Table 3.1. Note the base address for the IP module I/O space (see your carrier board instructions) must be added to the addresses shown to properly access the I/O space. All accesses are performed on an 8-bit byte basis (D0..D7).

This manual is presented using the "Big Endian" byte ordering format. Big Endian is the convention used in the Motorola 68000 microprocessor family and is the VMEbus convention. In Big Endian, the lower-order byte is stored at odd-byte addresses. Thus, byte accesses are done on odd address locations. The Intel x86 family of microprocessors use the opposite convention, or "Little Endian" byte ordering. Little Endian uses even-byte addresses to store the low-order byte. As such, use of this module on a PCI bus (PC) carrier board will require the use of the even address locations to access the 8-bit data, while a VMEbus carrier will require the use of odd address locations.

Note that some functions share the same register address. For these items, the address lines are used along with the read and write signals to determine the function required.

Standard (Default) Mode Memory Map

The following table shows the memory map for the Standard Mode of operation. This is the Default mode reached after power-up or system reset. Standard Mode provides simple monitor and control of 48 digital I/O lines. In Standard Mode, each I/O line is configured as either an input, or an output (with readback capability), but not both. Data is read from or written to one of eight groups (ports), as designated by the address and read and write signals. A Mask Register is used to disable writes to I/O ports designated as input ports. That is, when a port (group of 8 I/O lines) is used as an input port, writes to this port must be blocked (masked) to prevent contention between the output circuitry and any external device driving this line.

To switch to Enhanced Mode, four unique bytes must be written to port 7, in consecutive order, without doing any reads or writes to any other port and with interrupts disabled. This is usually done immediately after power-up or reset. The data pattern to be written is 07H, 0DH, 06H, and 12H, and this must be written after reset or power-up.

Table 3.1A: IP470A R/W Space Address (Hex) Memory Map

Base Addr+	MSB D15 D08	LSB D07 D00	Base Addr+
STANDARD MODE (DEFAULT) REGISTER DEFINITION:			
00	Not Driven[1]	READ/WRITE - Port 0 I/O Register I/O0-I/O7	**01**
02	Not Driven[1]	READ/WRITE - Port 1 I/O Register I/O8-I/O15	**03**
04	Not Driven[1]	READ/WRITE - Port 2 I/O Register I/O16-23	**05**
06	Not Driven[1]	READ/WRITE - Port 3 I/O Register I/O24-I/O31	**07**
08	Not Driven[1]	READ/WRITE - Port 4 I/O Register I/O32-I/O39	**09**
0A	Not Driven[1]	READ/WRITE - Port 5 I/O Register I/O40-I/O47	**0B**
0C	Not Driven[1]	READ/WRITE - Port 6 NOT USED	**0D**
0E	Not Driven[1]	READ/WRITE - Port 7 WRITE MASK REGISTER (Also Enhanced Mode Select Register)	**0F**
10 ↓ 7E	NOT USED[2]		**11 ↓ 7F**

1. The upper 8 bits of these registers are not driven and pull-ups on the carrier data bus will cause these bits to read high (1's).
2. The IP will return "0" for all addresses that are "Not Used".

Enhanced Mode Memory Maps

The following table shows the memory maps used for the Enhanced Mode of operation. Enhanced Mode includes the same functionality of Standard Mode, but allows each I/O port's event sense input and debounce logic to be enabled. Thus, the Enhanced Mode allows input event triggered interrupts to occur.

In Enhanced Mode, a memory map is given for each of 3 memory banks. The first memory bank (bank 0) has the same functionality as the Standard Mode. Additionally, its port 7 register is used to select which bank to access (similar to Standard Mode where port 7 was used to select the Enhanced Mode). Bank 1 provides read/write access to the 48 event sense inputs. Bank 2 provides access to the registers used to control the debounce circuitry applied to the event sense inputs.

Table 3.1B: IP470A R/W Space Address (Hex) Memory Map

Base Addr+	MSB D15 D08	LSB D07 D00	Base Addr+
ENHANCED MODE, REGISTER BANK [0] DEFINITION:			
00	Not Driven[1]	READ/WRITE - Port 0 I/O Register I/O0-I/O7	**01**
02	Not Driven[1]	READ/WRITE -Port 1 I/O Register I/O8-I/O15	**03**
04	Not Driven[1]	READ/WRITE - Port 2 I/O Register I/O16-I/O23	**05**
06	Not Driven[1]	READ/WRITE - Port 3 I/O Register I/O24-I/O31	**07**
08	Not Driven[1]	READ/WRITE - Port 4 I/O Register I/O32-I/O39	**09**
0A	Not Driven[1]	READ/WRITE - Port 5 I/O Register I/O40-I/O47	**0B**
0C	Not Driven[1]	READ/WRITE - Port 6 NOT USED	**0D**
0E	Not Driven[1]	READ - Port 7 READ MASK REGISTER (Also Current Bank Status)	**0F**
0E	Not Driven[1]	WRITE - Port 7 WRITE MASK REGISTER (Also Bank Select Register)	**0F**
ENHANCED MODE, REGISTER BANK [1] DEFINITION:			
00	Not Driven[1]	READ - Port 0 Event Sense Status Reg. (Port 0 I/O Points 0-7)	**01**
00	Not Driven[1]	WRITE - Port 0 Event Sense Clear Register (Port 0 I/O Points 0-7)	**01**
02	Not Driven[1]	READ - Port 1 Event Sense Status Reg. (Port 1 I/O Points 8-15)	**03**
02	Not Driven[1]	WRITE - Port 1 Event Sense Clear Register (Port 1 I/O Points 8-15)	**03**
04	Not Driven[1]	READ - Port 2 Event Sense Status Reg. (Port 2 I/O Points 16-23)	**05**
04	Not Driven[1]	WRITE - Port 2 Event Sense Clear Register (Port 2 I/O Points 16-23)	**05**
06	Not Driven[1]	READ - Port 3 Event Sense Status Reg. (Port 3 I/O Points 24-31)	**07**
06	Not Driven[1]	WRITE - Port 3 Event Sense Clear Register (Port 3 I/O Points 24-31)	**07**
08	Not Driven[1]	READ - Port 4 Event Sense Status Reg. (Port 4 I/O Points 32-39)	**09**
08	Not Driven[1]	WRITE - Port 4 Event Sense Clear Register (Port 4 I/O Points 32-39)	**09**
0A	Not Driven[1]	READ - Port 5 Event Sense Status Reg. (Port 5 I/O Points 40-47)	**0B**
0A	Not Driven[1]	WRITE - Port 5 Event Sense Clear Register (Port 5 I/O Points 40-47)	**0B**

Table 3.1B...continued:

Base Addr+	MSB D15 D08	LSB D07 D00	Base Addr+
...ENHANCED MODE, REGISTER BANK [1] DEFINITIONS:			
0C	Not Driven[1]	READ - Port 6 Event Status for Ports 0-5 and Interrupt Status Reg.	**0D**
0C	Not Driven[1]	WRITE - Port 6 Event Polarity Control Register for Port 0-3	**0D**
0E	Not Driven[1]	READ - Port 7 Event Polarity Control for Ports 4 & 5 and Current Bank Status Reg.	**0F**
0E	Not Driven[1]	WRITE - Port 7 Event Polarity Control for Ports 4 & 5 and Bank Select Register	**0F**
ENHANCED MODE, REGISTER BANK [2] DEFINITION:			
00	Not Driven[1]	READ/WRITE - Port 0 Debounce Control Register (for Ports 0-5)	**01**
02	Not Driven[1]	READ/WRITE - Port 1 Debounce Duration Reg. 0 (for Ports 0-3)	**03**
04	Not Driven[1]	READ/WRITE - Port 2 Debounce Duration Reg. 1 (for Ports 4 & 5)	**05**
06	Not Driven[1]	WRITE ONLY - Port 3 Debounce Clock Select (8MHz or I/O47)	**07**
08 ↓ 0C	Not Driven[1]	Port 4,5,6 NOT USED[2]	**09 ↓ 0D**
0E	Not Driven[1]	READ/WRITE - Port 7 Bank Status/Select Register	**0F**
INDEPENDENT FIXED FUNCTION REGISTERS:			
10 ↓ 1C	NOT USED[2]		**11 ↓ 1D**
1E	Not Driven[1]	READ/WRITE Interrupt Enable Register (enables INTREQ0) & Software Reset Generator	**1F**
20 ↓ 2C	NOT USED[2]		**21 ↓ 2D**
2E	Not Driven[1]	READ/WRITE Interrupt Vector Register[4]	**2F**
30 ↓ 7E	NOT USED[2]		**31 ↓ 7F**

Notes (Table 3.1):

1. The upper 8 bits of these registers are not driven and pull-ups on the carrier data bus will cause these bits to read high (1's).
2. The IP will return "0" for all addresses that are "Not Used".".
3. All Reads and Writes are 0 wait state.
4. The Interrupt Vector Register also decodes at base address + 6FH due to simplified address decoding.

REGISTER DEFINITIONS

STANDARD MODE REGISTERS

Port I/O Registers (Standard Mode, Ports 0-5, Read/Write)

Six I/O Registers are provided to control/monitor 48 possible I/O points. Data is read from or written to one of six groups (Ports 0-5) of eight I/O lines, as designated by the address and read and write signals. Each port assigns the least significant data line (D0) to the least significant I/O line of the port grouping (e.g. I/O00 for port 0). Thus, a write to this register controls the state of the open-drain output (low level true). A read of this register returns the status (ON/OFF) of the I/O point. A Mask Register is used to disable writes to I/O ports designated as input ports. That is, when a port (group of 8 I/O lines) is used as an input port, writes to this port must be blocked (masked) to prevent contention between the output circuitry and any external device driving this input line.

Outputs are open-drain mosfets with pull-ups installed. Thus, on power-up or reset, the port registers are reset to 0, forcing the outputs to be set high (OFF).

Write Mask Register & Enhanced Mode Select Register (Standard Mode, Port 7, Read/Write)

This register is used to mask the ability to write data to the six I/O ports. Writing a '1' to bits 0-5 of the Mask Register will mask ports 0-5 from write-control respectively. A read of this register will return the status of the mask. A Mask Register is used to disable writes to I/O ports designated as input ports. Thus, when a port (group of 8 I/O lines) is used for input, writes to this port must be blocked (masked) to prevent contention between the output circuitry (open-drain) and any external devices driving this port.

Standard Mode Write Mask Register (Port 7)

BIT	WRITE TO REGISTER	READ FROM REGISTER
0	Port 0 Write Mask	Port 0 Write Mask
1	Port 1 Write Mask	Port 1 Write Mask
2	Port 2 Write Mask	Port 2 Write Mask
3	Port 3 Write Mask	Port 3 Write Mask
4	Port 4 Write Mask	Port 4 Write Mask
5	Port 5 Write Mask	Port 5 Write Mask
6	NOT USED	NOT USED
7	NOT USED	NOT USED

Bits 6 & 7 of this register are not used. On power-up reset, this register defaults to the unmasked/clear state, allowing writes to the output ports.

This register is also used to select the Enhanced Mode of operation. To switch to Enhanced Mode, four unique bytes must be written to port 7, in consecutive order, without doing any reads or writes to any other port and with interrupts disabled. The data pattern to be written is 07H, 0DH, 06H, and 12H, in order, and this must be written immediately after reset or power-up.

ENHANCED MODE

BANK 0 REGISTERS

Port I/O Registers (Enhanced Mode Bank 0, Ports 0-5, Read/Write)

Six I/O Registers are provided to control/monitor 48 possible I/O points. Data is read from or written to one of six groups (Ports 0-5) of eight I/O lines, as designated by the address and read and write signals. Each port assigns the least significant data line (D0) to the least significant I/O line of the port grouping (e.g. I/O00 for port 0). A write to this register controls the state of the open-drain output (low level true). A read of this register returns the status (ON/OFF) of the I/O point. A Mask Register is used to disable writes to I/O ports designated as input ports. That is, when a port (group of 8 I/O lines) is used as an input port, writes to this port must be blocked (masked) to prevent contention between the output circuitry and any external devices driving this port.

Outputs are open-drain mosfets with pull-ups installed. Thus, on power-up or reset, the port registers are reset to 0, forcing the outputs to be set high (OFF).

Write Mask Register And Bank Select Register 0 (Enhanced Mode Bank 0, Port 7, Read/Write)

This register is used to mask the ability to write data to the six I/O ports in Enhanced Mode. Writing a '1' to bits 0-5 of the Mask Register will mask ports 0-5 from write-control respectively. A read of this register will return the status of the mask. A Mask Register is used to disable writes to I/O ports designated as input ports. Thus, when a port (group of 8 I/O lines) is used for input, writes to this port must be blocked (masked) to prevent contention between the output circuitry and any external devices driving this port.

Enhanced Mode Write Mask Register (Port 7)

BIT	WRITE TO REGISTER	READ FROM REGISTER
0	Port 0 Write Mask	Port 0 Write Mask
1	Port 1 Write Mask	Port 1 Write Mask
2	Port 2 Write Mask	Port 2 Write Mask
3	Port 3 Write Mask	Port 3 Write Mask
4	Port 4 Write Mask	Port 4 Write Mask
5	Port 5 Write Mask	Port 5 Write Mask
6	Bank Select Bit 0	Bank Status Bit 0
7	Bank Select Bit 1	Bank Status Bit 1

Bits 6 & 7 of this register are used to select/monitor the bank of registers to be addressed. In Enhanced Mode, three banks (banks 0-2) of eight registers may be addressed. Bank 0 is similar to the Standard Mode bank of registers. Bank 1 allows the 48 event inputs to be monitored and controlled. Bank 2 registers control the debounce circuitry of the event inputs. Bits 7 and 6 select the bank as follows:

Enhanced Mode Bank Select

Bit 7 Bit 6	BANK OF REGISTERS
00	Bank 0 - Read/Write I/O
01	Bank 1 - Event Status/Clear
10	Bank 2 - Event Debounce Control, Clock, and Duration
11	INVALID - DO NOT WRITE

On power-up reset, the device is put into the Standard Mode and this register defaults to the unmasked state (allowing writes to the output ports), and bank 0 (Default).

BANK 1 REGISTERS

Event Sense Status & Clear Registers For I/O0-47 (Enhanced Mode Bank 1, Ports 0-5, Read/Write)

Each I/O line of each port includes an event sense input. Reading each port will return the status of each I/O port sense line. Writing '0' for a bit position of each port will clear the event on the corresponding line. When writing ports 0-5 of Enhanced Mode bank 1, each data bit written with logic 0 clears the corresponding event sense flip/flop. Each data bit of ports 0-5 must be written with a 1 to re-enable (or initially enable) the corresponding event sense input after it is cleared. Reading ports 0-5 of Enhanced Mode bank 1 returns the current event sense flip/flop status.

Port 0 Event Sense/Status Register (Ports 1-5 Similar)

BIT	READ PORT	WRITE "0"	WRITE "1"
0	Port 0 I/O0 Event Status	Clear I/O0 Event Sense Flip/Flop	Re-enable I/O0 Event Sense
1	Port 0 I/O1 Event Status	Clear I/O1 Event Sense Flip/Flop	Re-enable I/O1 Event Sense
2	Port 0 I/O2 Event Status	Clear I/O2 Event Sense Flip/Flop	Re-enable I/O2 Event Sense
3	Port 0 I/O3 Event Status	Clear I/O3 Event Sense Flip/Flop	Re-enable I/O3 Event Sense
4	Port 0 I/O4 Event Status	Clear I/O4 Event Sense Flip/Flop	Re-enable I/O4 Event Sense
5	Port 0 I/O5 Event Status	Clear I/O5 Event Sense Flip/Flop	Re-enable I/O5 Event Sense
6	Port 0 I/O6 Event Status	Clear I/O6 Event Sense Flip/Flop	Re-enable I/O6 Event Sense
7	Port 0 I/O7 Event Status	Clear I/O7 Event Sense Flip/Flop	Re-enable I/O7 Event Sense

Event Interrupt Status Register For Ports 0-5 (Enhanced Mode Bank 1, Port 6, Read Only)

Reading this register will return the event interrupt status of I/O ports 0-5 (bits 0-5) and the interrupt status flag (bit 7). Bit 7 of this register indicates an event sense was detected on any of the 6 event sense ports ("1" = interrupt asserted/event sensed). Note that the interrupt status flag may optionally drive the Interrupt Request Line of the carrier board (see Interrupt Enable Register).

Event Interrupt Status Register For Ports 0-5

BIT	READ EVENT STATUS REGISTER
0	Port 0 Interrupt Status (I/O0-I/O7)
1	Port 1 Interrupt Status (I/O8-I/O15)
2	Port 2 Interrupt Status (I/O16-I/O23)
3	Port 3 Interrupt Status (I/O24-I/O31)
4	Port 4 Interrupt Status (I/O32-I/O39)
5	Port 5 Interrupt Status (I/O40-I/O47)
6	NOT USED
7	Interrupt Status Flag

Event Polarity Control Register For Ports 0-3 (Enhanced Mode Bank 1, Port 6, Write Only)

A write to this register controls the polarity of the input sense event for nibbles of ports 0-3 (channels 0-31, four channels at a time). A "0" written to a bit in this register will cause the corresponding event sense input lines to flag negative events (high-to-low transitions). A "1" will cause positive events to be sensed (low-to-high transitions). The polarity of the event sense logic must be set prior to enabling the event input logic. Note that no events will be detected until enabled via the Event Sense Status & Clear Register. Further, interrupts will not be reported to the carrier board unless control of Interrupt Request Line 0 has been configured via the Interrupt Enable Register.

Event Polarity Control Register

BIT	WRITE "0" (NEGATIVE)	WRITE "1" (POSITIVE)
0	Negative Events on Port 0 I/O0 through I/O3	Positive Events on Port 0 I/O0 through I/O3
1	Negative Events on Port 0 I/O4 through I/O7	Positive Events on Port 0 I/O4 through I/O7
2	Negative Events on Port 1 I/O8 through I/O11	Positive Events on Port 1 I/O8 through I/O11
3	Negative Events on Port 1 I/O12 through I/O15	Positive Events on Port 1 I/O12 through I/O15
4	Negative Events on Port 2 I/O16 through I/O19	Positive Events on Port 2 I/O16 through I/O19
5	Negative Events on Port 2 I/O20 through I/O23	Positive Events on Port 2 I/O20 through I/O23
6	Negative Events on Port 3 I/O24 through I/O27	Positive Events on Port 3 I/O24 through I/O27
7	Negative Events on Port 3 I/O28 through I/O31	Positive Events on Port 3 I/O28 through I/O31

Event Polarity Control For Ports 4 & 5 & Bank Select Register (Enhanced Mode Bank 1, Port 7, Read/Write)

A write to this register controls the polarity of the input sense event for nibbles of ports 4 & 5 (channels 32-47, four channels at a time). A "0" written to a bit in this register will cause the corresponding event sense input lines to flag negative events (high-to-low transitions). A "1" will cause positive events to be sensed (low-to-high transitions). The polarity of the event sense logic must be set prior to enabling the event input logic. Note that no events will be detected until enabled via the Event Sense Status & Clear Register. Further, interrupts will not be reported to the carrier board unless control of Interrupt Request Line 0 has been configured via the Interrupt Enable Register.

Event Polarity Control Register

BIT	WRITE "0" (NEGATIVE)	WRITE "1" (POSITIVE)
0	Negative Events on Port 4 I/O32 through I/O35	Positive Events on Port 4 I/O32 through I/O35
1	Negative Events on Port 4 I/O36 through I/O39	Positive Events on Port 4 I/O36 through I/O39
2	Negative Events on Port 5 I/O40 through I/O43	Positive Events on Port 5 I/O40 through I/O43
3	Negative Events on Port 5 I/O44 through I/O47	Positive Events on Port 5 I/O44 through I/O47
4	NOT USED	
5	NOT USED	
6	Bank Select Bit 0	
7	Bank Select Bit 1	

Bits 6 & 7 of this register are used to select/monitor the bank of registers to be addressed. In Enhanced Mode, three banks (banks 0-2) of eight registers may be addressed. Bank 0 is similar to the Standard Mode bank of registers. Bank 1 allows the 48 event inputs to be monitored and controlled. Bank 2 registers control the debounce circuitry of the event inputs. Bits 7 and 6 select the bank as follows:

Bank Select Register (Write)

Bit 7 Bit 6	BANK OF REGISTERS
00	Bank 0 - Read/Write I/O
01	Bank 1 - Event Status/Clear
10	Bank 2 - Event Debounce Control, Clock, and Duration
11	INVALID - DO NOT WRITE

Bank Select Status Register 1 (Enhanced Mode Bank 1, Port 7, Read Only)

Bits 0-5 of this register are not used. Bits 6 & 7 of this register are used to indicate the bank of registers to be addressed. In Enhanced Mode, three banks (banks 0-2) of eight registers may be addressed. Bank 0 is similar to the Standard Mode bank of registers. Bank 1 allows the 48 event inputs to be monitored and controlled. Bank 2 registers control the debounce circuitry of the event inputs. Bits 7 and 6 select the bank as follows:

Bank Selected Status Register (Read)

Bit 7 Bit 6	BANK OF REGISTERS
00	Bank 0 - Read/Write I/O
01	Bank 1 - Event Status/Clear
10	Bank 2 - Event Debounce Control, Clock, and Duration
11	INVALID - DO NOT WRITE

BANK 2 REGISTERS

Debounce Control Register (Enhanced Mode Bank 2, Port 0, Read/Write)

This register is used to control whether each individual port is to be passed through the debounce logic before being recognized by the circuitry. A "0" disables the debounce logic, and a "1" enables the debounce logic. Debounce is applied to both inputs and event sense inputs, and only in Enhanced Mode.

Debounce Control Register

BIT	DEBOUNCE CONTROL
0	Port 0 (I/O0-I/O7)
1	Port 1 (I/O8-I/O15)
2	Port 2 (I/O16-I/O23)
3	Port 3 (I/O24-I/O31)
4	Port 4 (I/O32-I/O39)
5	Port 5 (I/O40-I/O47)
6 & 7	NOT USED

"0"	"1"
Disable	Enable

Debounce Duration Register 0 (Enhanced Mode Bank 2, Port 1, Read/Write)

Debounce Duration Register 1 (Enhanced Mode Bank 2, Port 2, Read/Write)

These registers control the duration required by each input signal before it is recognized by each individual input in the Enhanced Mode (both inputs and event inputs). Register 0 controls debounce for ports 0-3. Register 1 controls debounce for ports 4 & 5. If the debounce clock selected is the 8MHz IP clock (see Debounce Clock Select Register), then the debounce times are selected as shown below to within ±250nS. Alternately, the debounce clock may be input on I/O47 and other values configured (see Debounce Clock Select Register), but this reduces the effective number of input channels to 47.

Debounce Duration Register 0:

BIT	DEBOUNCE CONTROL
0	Port 0 Debounce Value Bit 0
1	Port 0 Debounce Value Bit 1
2	Port 1 Debounce Value Bit 0
3	Port 1 Debounce Value Bit 1
4	Port 2 Debounce Value Bit 0
5	Port 2 Debounce Value Bit 1
6	Port 3 Debounce Value Bit 0
7	Port 3 Debounce Value Bit 1

Duration (8MHz):

Bit 1,0	Time
00	4 us
01	64 us
10	1 ms
11	8 ms

Debounce Duration Register 1

BIT	DEBOUNCE CONTROL
0	Port 4 Debounce Value Bit 0
1	Port 4 Debounce Value Bit 1
2	Port 5 Debounce Value Bit 0
3	Port 5 Debounce Value Bit 1
4,5,6,7	NOT USED

Note that with an 8MHz clock, a debounce value of 00 sets a nominal value of 4us, 01 sets 64us, 10 sets 1ms, and 11 sets 8ms. The default value is 00, setting a 4us debounce period for an 8MHz debounce clock.

When using I/O47 as the debounce clock the effective debounce can be calculated by taking the clock period (in seconds) and multiplying it by the appropriate constant shown in the table below. The debounce will have an error of ±2 clock periods.

Debounce Duration Selection	Debounce Count Constant
00	32
01	512
10	8000
11	64000

Debounce Clock Select Register
(Enhanced Mode Bank 2, Port 3, Write Only)

This register selects the source clock for the event sense input debounce circuitry. If bit 0 of this register is 0 (default value), then the debounce source clock is taken from I/O47 (pin 41 of P2), thus reducing the effective number of inputs to 47. If bit 0 is set to 1, then the 8MHz IP bus clock is used (recommended). Bits 1-7 of this register are not used and will always read as zero. **WARNING IF USING I/O47 AS THE DEBOUNCE CLOCK, DO NOT SET THE I/O AS AN ACTIVE OUTPUT VIA THE PORT I/O REGISTERS. SETTING I/O47 AS AN ACTIVE OUTPUT MAY CAUSE A BUS CONFLICT.**

Bank Select (Write) & Status (Read) Register 2
(Enhanced Mode Bank 2, Port 7, Read and Write)

Bits 0-5 of this register are not used. Bits 6 & 7 of this register are used to indicate (read) or select (write) the bank of registers to be addressed. In Enhanced Mode, three banks (banks 0, 1, & 2) of eight registers may be addressed. Bank 0 is similar to the Standard Mode bank of registers. Bank 1 allows the 48 event inputs to be monitored and controlled. Bank 2 registers control the debounce circuitry of inputs. Bits 7 and 6 select/indicate the bank as follows:

Bank Select (Write) & Status (Read) Register

Bit 7 Bit 6	BANK OF REGISTERS
00	Bank 0 - Read/Write I/O
01	Bank 1 - Event Status/Clear
10	Bank 2 - Debounce Control, Clock, & Duration
11	INVALID - DO NOT WRITE

INDEPENDENT FIXED FUNCTION CONTROL REGISTERS

Interrupt Enable & Software Reset Register (Read/Write)

Bit 0 of this register specifies if the internal event sense interrupts are to be reported to the carrier or not (i.e. whether they drive INTREQ0 or not). This bit defaults to 0 (interrupt request disabled) and event interrupts are only flagged internally. That is, you would have to poll the Event Status Register to determine if an interrupt had occurred or not and the INTREQ0 line would not be driven. If bit 0 of this register is set to “1”, then interrupts will drive the INTREQ0 line and permit Interrupt Select Cycles (INTSEL) to occur. This bit is cleared following a system reset, but not a software reset (see below).

Writing a 1 to the bit 1 position of this register will cause a software reset to occur (be sure to preserve the current state of bit 0 when conducting a software reset). This bit is not stored and merely acts as a trigger for software reset generation (this bit will always readback as 0). The effect of a software reset is similar to a carrier reset, except that it is not driven by the carrier and it only resets the digital ASIC chip that provides the field interface functions. Likewise, the Interrupt Vector Register or the Interrupt Enable Bit of this register is not cleared in response to a software reset (these are not stored in the ASIC). It is useful for use with some carriers, which do not implement the bus reset control. Bits 2-7 of this register are not used and will always read high (1’s).

Interrupt Vector Register (Read/Write)

This 8-bit read/write register is used to store the interrupt vector. Interrupts are driven by events in the Enhanced Mode. In response to an interrupt select cycle, the IP module will execute a read of this register. This register is cleared following a system reset, but not a software reset. Note that interrupts will not be reported to the carrier board unless control of Interrupt Request Line 0 has been enabled via the Interrupt Enable register.

IP Identification PROM - (Read Only, 32 Odd-Byte Addresses)

Each IP module contains an identification (ID) PROM that resides in the ID space per the IP module specification. This area of memory contains 32 bytes of information at most. Both fixed and variable information may be present within the ID PROM. Fixed information includes the "IPAC" identifier, model number, and manufacturer's identification codes. Variable information includes unique information required for the module. The IP470A ID PROM does not contain any variable (e.g. unique calibration) information. ID PROM bytes are addressed using only the odd addresses in a 64-byte block (on the “Big Endian” VMEbus). Even addresses are used on the “Little Endian” PC bus. The IP470A ID PROM contents are shown in Table 3.2. Note that the base-address for the IP module ID space (see your carrier board instructions) must be added to the addresses shown to properly access the ID PROM. Execution of an ID PROM Read requires 0 wait states.

Table 3.2: IP470A ID Space Identification (ID) PROM

Hex Offset From ID PROM Base Address	ASCII Character Equivalent	Numeric Value (Hex)	Field Description
01	I	49	All IP's have 'IPAC'
03	P	50	
05	A	41	
07	C	43	
09		A3	Acromag ID Code
0B		08	IP Model Code[1]
0D		00	Not Used (Revision)
0F		00	Reserved
11		00	Not Used (Driver ID Low Byte)
13		00	Not Used (Driver ID High Byte)
15		0C	Total Number of ID PROM Bytes
17		ED	CRC
19 to 3F		yy	Not Used

Notes (Table 3.2):

1. The IP model number is represented by a two-digit code within the ID PROM (the IP470A model is represented by 08 Hex).

THE EFFECT OF RESET

Power-up or bus-initiated software reset will set the outputs to the false (high) state and place the module in the Standard Operating Mode (thus disabling debounce and event detection). Pull-ups on the I/O lines ensure a false (high) input signal for inputs left floating (i.e. reads as 0). A reset will also clear the mask register and enable writes to the I/O ports. Further, all I/O event inputs are reset, set to negative events, and are disabled following reset. The Interrupt Enable Register (IER) and Interrupt Vector Register (IVR) are also cleared (except for IER generated software resets).

Another form of software reset (IER register initiated) acts similar to a carrier or power-up reset, except that it is not driven by the carrier and only resets the digital ASIC chip installed on the module. As such, the Interrupt Vector Register and Interrupt Enable Register are not cleared for a software reset initiated in this manner (writing a 1 to the bit 1 position of the IER Register will cause this type of software reset to occur). Reset in this manner has been provided for use with some ISA carriers which do not implement the bus reset control, or when the interrupt vector and interrupt enable information must be preserved following reset.

Basic I/O Operation

Note that the I/O lines of this module are assembled in groups of eight. Each group of eight I/O lines is referred to as a port. Ports 0-5 control and monitor I/O lines 0-47. Additionally, ports are grouped eight to a bank. There are four banks of ports used for controlling this module (Standard Mode, plus Enhanced Mode Banks 0, 1, and 2), plus 2 additional registers for enabling the interrupt request line, generating a software reset, and storing the interrupt vector.

In both the Standard and Enhanced operating modes, each group of eight parallel input lines (port) are gated to the data bus D0..D7 lines. These input signals are inverted--when an output is ON (set to “1”), the transistor sinks current and drives the output low (this is readback as a “1”). Inputs include hysteresis. Further, each input port is connected such that the current status of a given output port can be read back via the corresponding input port. Individual ports may also be masked from writes to the port when the port is intended for input only and this helps prevent contention errors.

Each port I/O line includes an integrated, 47.5KΩ (nominal) pull-up resistor to +5V. Additional 4.7KΩ pull-up resistor SIP’s are also installed in sockets on the board. For inputs, the pull-ups provide a low (false=0) input indication if the input is left floating.

Each I/O line is in the form of an open-drain signal. Thus, data written to any port used as an input must be masked or always false (zero) to avoid contention errors between the output circuitry and an input signal from an external device. All 48 I/O lines are placed into the false (high output) state following power-up or a system reset. The 4.7KΩ pull-up resistor SIP’s installed in sockets on the board provide only limited digital high-drive capability for the output signals. You may need to adjust these pull-up values for your application (see Drawing 4502-057 for SIP resistor location).

Enhanced Operating Mode

In the Enhanced Mode of operation, each port signal has an associated event sense input and debounce logic circuit. The event sense inputs are used to sense high-to-low level or low-to-high level transitions on digital input lines at CMOS thresholds. Interrupts may also be triggered by events. The optional debounce logic can act as a filter to “glitches” or transients present on the received signals.

Individual ports may be masked from writes to the port when the port is used for input. This helps prevent contention errors. Further, event polarities may be defined as positive or negative for individual nibbles (in groups of 4 I/O lines, or half ports).

The Enhanced Mode is entered by writing four unique bytes to the Port 7 register, in consecutive order, without doing any reads or writes to any other port and with interrupts disabled. The data pattern to be written is 07H, 0DH, 06H, and 12H, and this must be written immediately after reset or power-up.

In Enhanced Mode, there are three groups (or banks) of eight registers or ports. The first group, bank 0, provides register functionality similar to Standard Mode. The second group, bank 1, provides monitor and control of the event sense inputs. The third group, bank 2, is used to configure the debounce circuitry for each input while in the Enhanced Mode.

Event Sense Inputs

The IP470A has event sense logic built-in for all 48 digital I/O lines, I/O00 through I/O47. Event sensing may be configured to generate an interrupt to the carrier, or merely reflect the interrupt

internally. Event sensing is enabled in Enhanced Mode only. Inputs can be set to detect positive or negative events, on a nibble-by-nibble (group of 4 I/O lines) basis. The event sensing is enabled on an individual channel basis. You can combine event sensing with the built-in debounce control circuitry to obtain "glitch-free" edge detection of incoming signals.

To program events, determine which I/O lines are to have events enabled and which polarity is to be detected, high-to-low level transitions (negative) or low-to-high level transitions (positive). Set each half-port (nibble) to the desired polarity, and then enable each of the event inputs to be detected. Optionally, load the interrupt vector register and enable the interrupt request line. Note that all I/O event inputs are reset, set to negative events, and disabled after a power-up or software reset has occurred.

Note that no events will be detected until enabled via the Event Sense Status & Clear Register. Further, interrupts will not be reported to the carrier board unless control of Interrupt Request Line 0 has been configured via the Interrupt Enable Register.

Change-Of-State Detection

Change-of-State signal detection requires that both a high-to-low and low-to-high signal transition be detected. On the IP470A, if change-of-state detection for an input signal is desired, two channels connected to the same input signal would be required--one sensing positive transitions, one sensing negative transitions.

Since channel polarity is programmable on a nibble basis (group of four), the first nibble of a port could be configured for low-to-high transitions, the second nibble for high-to-low transitions. As such, up to 24 change-of-state detectors may be configured.

Debounce Control

Debounce control is built into the on-board digital FPGA employed by the IP470A and is enabled in the Enhanced Mode only. You can combine debounce with event sensing to obtain "glitch-free" edge detection of incoming signals for all 48 channels. That is, the debounce circuitry will automatically filter out "glitches" or transients that can occur on received signals, for error-free edge detection and increased noise immunity. With debounce, an incoming signal must be stable for the entire debounce time before it is recognized by the I/O or event sense logic. Debounce is applied to both inputs and event sense inputs and only in Enhanced Mode.

The debounce circuitry can be configured to use the 8MHz carrier clock, or a clock signal present on I/O47, to determine the debounce times (see the Debounce Clock Select register). If the debounce clock is taken from I/O47, then the effective number of inputs is reduced to 47. If the IP470A is configured to use the 8MHz carrier clock (recommended), a debounce value of 4us, 64us, 1ms, or 8ms may be selected (see the Debounce Duration Register). As such, an incoming signal must be stable for the debounce time before it is recognized by the I/O pin or event sense logic. A slower clock may be used to provide even longer debounce times (this clock would have to be provided on I/O47).

Upon initialization of the debounce circuitry, be sure to delay at least the programmed debounce time before reading any of the input ports or event signals to ensure that the input data is valid prior to being used by the software.

Interrupt Generation

This model provides control for generation of interrupts on positive or negative events, for all 48 channels. Interrupts are only generated in the Enhanced Mode for event channels when enabled via the Event Sense/Status Register. Writing 0 to the corresponding event sense bit in the Event Sense/Status Register will clear the event sense flip/flop. Successive interrupts will only occur if the event channel has been reset by writing a 1 to the corresponding event sense bit in the Event Sense/Status Register (after writing 0 to clear the event sense flip/flop). Interrupts may be reflected internally and reported by polling the module, or optionally reported to the carrier by enabling control of the Interrupt Request line (Intreq0). Control of this line is initiated via bit 0 of the Interrupt Enable Register (IER).

After pulling the IntReq0 line low and in response to an Interrupt Select cycle, the module will provide its 8-bit interrupt vector. The interrupt vector is written to the Interrupt Vector Register. The IP module will thus execute a read of the Interrupt Vector Register in response to an interrupt select cycle. The IntReq0 line will be released as soon as the conditions generating the interrupt have been cleared or return to normal, and the event sense flip/flop has been cleared by writing 0 to the corresponding bit position of the Event Sense Status Register, or until the Interrupt Enable Register bit is cleared. Zero wait states are required to complete an interrupt select cycle.

Note that the state of the inputs (on/off) can be determined by reading the corresponding port address while in bank 0 of the Enhanced Mode. However, the event sense status can only be read by reading the corresponding port address while in bank 1 of the Enhanced Mode. Remember, the event sense status is a flag that is raised when a specific positive or negative transition has occurred for a given I/O point, while the state refers to its current level.

Note that the Interrupt Enable Register and Interrupt Vector Register are cleared following a power-up or bus initiated software reset, but not a software reset initiated via writing a one to bit 1 of the Interrupt Enable Register. Keep this in mind when you wish to preserve the information in these two registers following a reset.

PROGRAMMING EXAMPLE

The following example outlines the steps necessary to configure the IP470A for Enhanced Mode operation, to setup event-generated interrupts, configure debounce, and read and write inputs. It is assumed that the module has been reset and no prior (non-default) configuration exists.

For this example, we will configure port 0 I/O points as a four-channel change-of-state detector. For change-of-state detection, both positive and negative polarities must be sensed and thus, two channels are required to detect a change-of-state on a single input signal. I/O00-I/O03 will be used to detect positive events (low-to-high transitions); I/O04-07 will be used to detect negative events (high-to-low transitions). I/O00 and I/O04 will be tied to the first input signal, I/O01 & I/O05 to the second, I/O02 & I/O06 to the third, and I/O03 & I/O07 to the fourth. Any change-of-state detected on these input signals will cause an interrupt to be generated.

1. After power-up or reset, the module is placed in the Standard Operating Mode. To switch to Enhanced Mode, execute four consecutive write cycles to port 7 with the following data: 07H first, followed by 0DH, followed by 06H, then 12H.

   At this point, you are in Enhanced Mode bank 0. Port 7 would be used to access register banks 1 & 2.

2. Write 80H to the port 7 address to select register bank 2 where debounce will be configured for our port 0 input channels.

   At this point, you are in Enhanced Mode Bank 2 where access to the debounce configuration registers is obtained.

3. For our example, we want use the 8MHz system clock to generate our debounce time. By default, the debounce clock is taken from I/O47 (pin 41 of P2). Select the 8MHz system clock as the debounce clock by writing 01H to the port 3 address of this bank (Debounce Clock Select Register).

4. The default debounce duration is 4us with the 8MHz clock selected in step 3. Write 01H to the port 1 address of this bank to select a 64us debounce time (Debounce Duration Register 0). An incoming signal must be stable for the entire debounce time before it will be recognized as a valid input transition.

   Note that Debounce Duration Register 1 (port address 2) would be used to configure debounce durations for I/O points of ports 4 & 5.

5. Enable the debounce circuitry for port 0 inputs by setting bit 0 of the Debounce Control Register. Write 01H to the Port 0 address of this bank (Debounce Control Register).

   If the module had been configured earlier, you would first read this register to check the existing settings of debounce enable for the other ports of this module with the intent of preserving their configuration by adjusting the value written above.

6. Write 40H to the port 7 address to select register bank 1 where the event polarity requirements of our application will be configured.

   At this point, you are in Enhanced Mode Bank 1 where access to the event polarity/status registers is obtained.

7. For change-of-state detection, both positive and negative polarities must be sensed. As such, two channels are required to detect a change-of-state on a single input signal. For our example, I/O00-I/O03 will be used to detect positive events (low-to-high transitions); I/O04-07 will be used to detect negative events (high-to-low transitions). Write 01H to the port 6 address to set I/O00-I/O03 to positive edge detection, and I/O04-07 to negative edge detection (Port 4 and 5 I/O channels would use the Port 7 address).

   Note that this port address has a dual function depending on whether a read or write is being executed. As such, if the current polarity configuration for the other ports must be preserved, then it must be remembered since it cannot be read back.

8. To enable event sensing for the port 0 I/O points, write FFH to the Event Sense Status Register for port 0 I/O points at the port 0 address in this bank.

   Note that writing a 1 to a bit position enables the event sense detector, while writing a 0 clears the event sensed without enabling further event sensing.

9. Write 00H to the port 7 address to select register bank 0 where the port 0 input channels may be write-masked.

   Note that the port 7 address bank selection only operates from bits 6 & 7 of this register, while bits 0-3 are used to select the event polarity for port 4 & 5 I/O channels. Keep this in mind when switching banks so as not to inadvertently change the polarity configuration of port 4 & 5 input channels in the process of switching register banks. Likewise, this register has a dual function depending on whether a read or write is executed. As such, the polarity settings cannot be read back and must be remembered if they are to be preserved for successive writes.

   At this point, you are in Enhanced Mode Bank 0 where access to the write-mask register is obtained.

10. For our example, port 0 I/O points are to be used for inputs only and writes to this port should be masked to prevent the possibility of data contention between the built-in output circuitry and the devices driving these inputs. Write 01H to the port 7 address to mask writes to port 0.

11. Read 01H from the port 7 address to verify bank 0 access (bits 6 & 7 are 0) and port 0 write masking (bit 0 is 1).

12. (OPTIONAL) Write your interrupt vector to the Interrupt Vector Register Address (Note that this register operates independent of the current bank since it does not reside at any of the bank addresses).

13. (OPTIONAL) Write 01H to the Interrupt Enable Register (IER) address location to enable IP control of the IP Interrupt Request 0 line (IntReq0).

    When a change-of-state is detected, IntReq0 will be pulled low (if the event sense detection circuitry has been enabled and IER bit 0=1). In response, the host will execute an Interrupt Select cycle and the contents of the Interrupt Vector Register will be provided. To enable further interrupts to occur for an event that has already occurred for an I/O point, the Event Sense Status Register must be written with a 1 to reenable event sensing for subsequent events (but only after first writing 0 to the corresponding bit position to clear the event sense flip/flop).

    Note that the state of the inputs (on/off) can be determined by reading the corresponding port address while in bank 0 of the Enhanced Mode. However, the event sense status can only be read by reading the corresponding port address while in bank 1 of the Enhanced Mode. Remember, the event sense status is a flag that is raised when a specific positive or negative transition has occurred for a given I/O point, while the state refers to its current level.

4.0 THEORY OF OPERATION

This section provides a description of the basic functionality of the circuitry used on the board. Refer to the Drawing 4502-047 as you review this material.

IP470A OPERATION

The IP470A is built around a Field-Programmable Gate Array (FPGA) IC. The device provides the control interface necessary to operate the module, the IP identification space, all registers, and provides I/O interface and configuration functions. The FPGA monitors and controls the functions of the 48 digital I/O used by this model. It also provides debounce control and event sensing functions.

Electronic protection array circuitry is also installed on board for increased ESD and overvoltage protection of each I/O line. I/O lines are pulled up to +5V via 4.7KΩ SIP resistors installed in sockets on the board. However, weak internal pull-ups of 47.5KΩ nominal are always present on these lines with the SIP resistors removed.

LOGIC/POWER INTERFACE

The logic interface to the carrier board is made through connector P1 (refer to Table 2.2). P1 also provides +5V to power the module (the ±12V lines are not used). Not all of the IP logic P1 pin functions are used.

The FPGA installed on the IP Module provides the control signals required to operate the board. It decodes the selected addresses in the I/O, Interrupt, and ID spaces and produces the chip selects, control signals, and timing required by the control registers, as well as, the acknowledgement signal required by the carrier board per the IP specification. It also stores the interrupt vector and controls whether event interrupts will drive the carrier board interrupt request line.

The ID Space (read only) is implemented in the FPGA and provides the identification for the individual module per the IP specification. The ID Space & configuration and control registers are all accessed through an 8-bit data bus interface to the carrier board.

KNOWN DIFFERENCES BETWEEN THE IP470 AND IP470A

Due to changes in the field I/O circuitry, the IP470A no longer has any measurable input hysteresis. Additional specifications have also been added that were not defined on the original IP470 including maximum slew rate, output turn on and turn off time, and input response time. These specifications can be found in section 6.0 of this manual.

In addition further enhancements to the device include precision debounce (no longer contains -25% error) and a decrease in input capacitance. In addition, all IP read and write requests are acknowledged preventing a possible lock-up of the bus. The original IP470 did not respond (Ack*) to Not Used Registers and any system response would be defined by the carrier (e.g. IP timeout). Not-Used registers always read as zero unless otherwise noted in this manual.

The jumper J1 on the IP470 has been replaced with two 0-Ohm resistors in the IP470A. J1 was used to select either 5V or Ground for Pin 49 of the Field I/O. That selection now requires removing a zero ohm resistor and replacing it with another. Furthermore, the SIP resistors though located in similar places on the board may pull-up different signals. See Acromag drawing 4205-057 for further details on both issues.

One additional difference is the power-on initialization time for the IP470A has increased to 200ms maximum. The module will not respond to any signal for up to 200ms following power-up. For further details on the differences between the models please contact Acromag.

5.0 SERVICE AND REPAIR

SERVICE AND REPAIR ASSISTANCE

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation For Use, have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Verify that there are no blown fuses. Replacement of the carrier and/or IP with one that is known to work correctly is a good technique to isolate a faulty board.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

WHERE TO GET HELP

If you continue to have problems, your next step should be to visit the Acromag worldwide web site at http://www.acromag.com. Our web site contains the most up-to-date product and software information.

Go to the “Support” tab to access:

- Application Notes
- Frequently Asked Questions (FAQ’s)
- Product Knowledge Base
- Tutorials
- Software Updates/Drivers

An email question can also be submitted from within the Knowledge Base or directly from the “Contact Us” tab.

Acromag’s application engineers can also be contacted directly for technical assistance via telephone or FAX through the numbers listed below. When needed, complete repair services are also available.

Phone: 248-624-1541
Fax: 248-624-9234
Email: solutions@acromag.com

6.0 SPECIFICATIONS

GENERAL SPECIFICATIONS

Physical Configuration.....Single Industrial I/O Pack Module.
- Length.....3.880 inches (98.5 mm).
- Width.....1.780 inches (45.2 mm).
- Board Thickness.....0.062 inches (1.59 mm).
- Max Component Height.....0.314 inches (7.97 mm).

Connectors:
- P1 & P2 .....IP logic (P1) & field (P2) interface connectors -.50-pin female receptacle header.

Power:
- +5 Volts (±5%).....85mA, Typical (all outputs active); 35mA, Typical (all outputs inactive); 160mA, Maximum.
- ±12 Volts (±5%) from P1.....0mA Maximum (Not Used).

ENVIRONMENTAL

Operating Temperature.....0 to +70°C.
-40 to +85°C (E Versions)
Relative Humidity.....5-95% non-condensing.
Storage Temperature.....-55°C to +150°C.
Non-Isolated.....Logic and field commons have a direct electrical connection.
Radiated Field Immunity (RFI)....Complies with EN61000-4-3 (10V/m, 80 to 1000MHz AM & 900MHz. keyed) and European Norm EN50082-1 with no digital upsets.
Conducted RF Immunity (CRFI)..Complies with EN61000-4-6 3V/rms, 150KHz to 80MHz) and European Norm EN50082-1 with no digital upsets.
Electromagnetic Interference Immunity (EMI).....No digital upset under the influence of EMI from switching solenoids, commutator motors, and drill motors.
Electrostatic Discharge Immunity (ESD).....Complies with EN61000-4-2 Level 3 (8KV enclosure port air discharge) and Level 2 (4KV enclosure port contact discharge) and European Norm EN50082-1.
Surge Immunity.....Not required for signal I/O per European Norm EN50082-1.
Electric Fast Transient Immunity EFT..... Complies with EN61000-4-4 Level 2 (0.5KV at field I/O terminals) and European Norm EN50082-1.
Radiated Emissions..... Meets or exceeds European Norm EN50081-1 for class B equipment. Shielded cable with I/O connections in shielded enclosure are required to meet compliance.

DIGITAL INPUTS

Input Channel Configuration.....48 buffered inputs. For DC voltage applications only, observe proper polarity. Input Debounce. Each input includes debounce circuitry with variable debounce times. Debounce times are programmable and derived from a clock signal present on I/O47, or the 8MHz system clock, in combination with the debounce duration register value. Note that if the debounce clock is delivered on I/O47, then this effectively reduces the number of inputs to 47. As such, use of the 8MHz system clock is recommended.
Interrupts.....48 channels of interrupts may be configured for high-to-low, low-to-high, and change-of-state (two inputs required) event types.
Input Voltage Range.....Ground -0.25V to +5 Volt supply +0.25V.
Input Low Voltage Range.....0.8V Maximum to 0.25V below Common Ground.
Input High Voltage Range.....2.2V Minimum to (Supply + 0.25V) Maximum.
Input transition rise of fall time.....3mS/V Maximum
Input Response Time.....250nS Typical
Input Threshold.....1.5V Typical.
Input/Output Capacitance.....20pF Maximum, 10pF Typical.
Input Leakage Current.....±10uA, Typical.
Debounce Times.....The Input debounce is implemented using a counter.

Debounce Register Setting	Debounce Count
00	32
01	512
10	8000
11	64000

The debounce time can be calculated by taking the clock period (in seconds) and multiplying it by the debounce count given in the table on the left. Note that all debounce times, including the internal 8MHz clock, have a tolerance of ±2 clock periods. The default 8MHz has debounce times of 4us, 64us, 1ms, or 8ms with an error of 250ns.

DIGITAL OUTPUTS

Output Channel Configuration.... 48 open-drain CMOS outputs. For DC voltage applications only, observe proper polarity.
Output Low Voltage.....0.1VDC Typical, 0.4VDC Maximum at 12mA.
Output High Voltage.....(Supply -0.2V) at -10uA.
Output "ON" Current Range.....0 to 15mA DC (for $V_{OL} \leq 0.5V$).
Output R_{ds} ON Resistance.....33Ω, Maximum (25°C).
Output Pullups.....4.7KΩ pull-ups are installed in sockets on the board. Even with these pull-ups removed, weak integrated 47.5KΩ nominal pull-ups are always present. See Drawing 4502-057 for resistor locations.

Turn On Time.....125nS Typical
Turn Off Time (4.7K pull-ups).....2μS Typical

INDUSTRIAL I/O PACK COMPLIANCE

Specification..... This device meets or exceeds all written Industrial I/O Pack specifications per ANSI/VITA 4-1995 for 8MHz operation.
Electrical/Mechanical Interface…Single-Size IP Module.

I/O Space (IOSEL*).....16-bit or 8-bit read/write of low byte.
ID Space (IDSEL*).....8-bit read: Supports Type 1, 32 bytes per IP (Consecutive odd byte address).
Interrupt Space (INTSEL*).....8-bit read of Interrupt Vector Register contents.
Memory Space (MEMSEL*).…….Not Used.

Power-Up Initialization Time.....200mS Max. (During this time the IP module will ignore all signals.)

Access Times (8MHz Clock):
All Read/Write Cycles.....0 wait states (250ns cycle).

APPENDIX

CABLE: MODEL 5025-550-x (Non-Shielded)
MODEL 5025-551-x (Shielded)

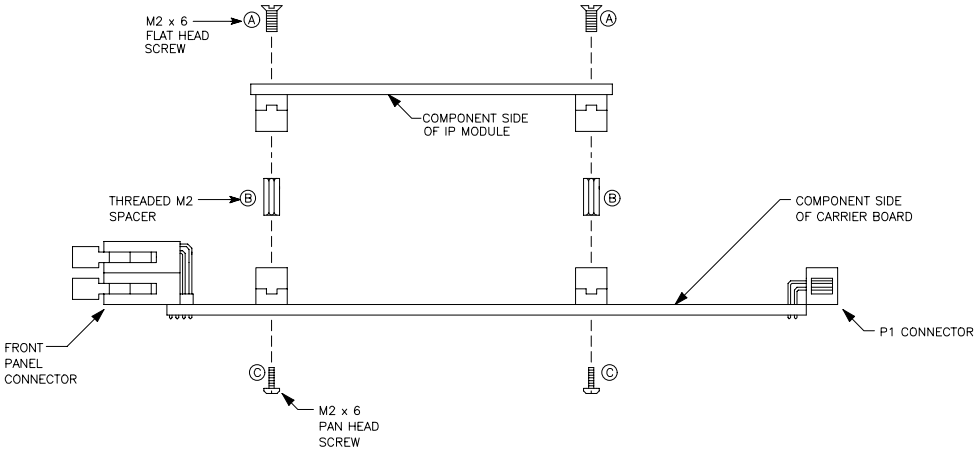
Type: Flat Ribbon Cable, 50-wires (female connectors at both ends). The cables are available in 4, 7, or 10 feet lengths. Custom lengths (12 feet maximum) are available upon request. Choose shielded or unshielded cable according to model number. The unshielded cable is recommended for digital I/O, while the shielded cable is recommended for optimum performance with precision analog I/O applications.
Application: Application: Used to connect Model 5025-552 termination panel to carrier board 50-pin field connectors.
Length: Last field of part number designates length in feet (4, 7, or 10 feet standard). It is recommended that this length be kept to a minimum to reduce noise and power loss.
Cable: 50-wire flat ribbon cable, 28 gage. Non-Shielded cable model uses Acromag Part 2002-211 (3M Type C3365/50 or equivalent). Shielded cable model uses Acromag Part 2002-261 (3M Type 3476/50 or equivalent).
Headers (Both Ends): 50-pin female header with strain relief. *Header* - Acromag Part 1004-512 (3M Type 3425-6600 or equivalent). *Strain Relief* - Acromag Part 1004-534 (3M Type 3448-3050 or equivalent).
Keying: Headers at both ends have polarizing key to prevent improper installation.
Schematic and Physical Attributes: For Shielded cable model, see Drawing 4501-463.
Shipping Weight: 1.0 pound (0.5Kg), packed.

TERMINATION PANEL: MODEL 5025-552

Type: Termination Panel For IP Carrier Boards
Application: To connect field I/O signals to the Industrial I/O Pack (IP). *Termination Panel:* Acromag Part 4001-040 (Phoenix Contact Type FLKM 50). The 5025-552 termination panel facilitates the connection of up to 50 field I/O signals and connects to the AVME9630/9660/9668 or APC8620/21 non-intelligent carrier boards via a flat ribbon cable (Model 5025-550-x or 5025-551-x). The A-E connectors on the carrier board connect the field I/O signals to the P2 connector on each of the Industrial I/O Pack modules. Field signals are accessed via screw terminal strips. The terminal strip markings on the termination panel (1-50) correspond to P2 (pins 1-50) on the Industrial I/O Pack (IP). Each Industrial I/O Pack (IP) has its own unique P2 pin assignments. Refer to the IP module manual for correct wiring connections to the termination panel.
Schematic and Physical Attributes: See Drawing 4501-464.
Field Wiring: 50-position terminal blocks with screw clamps. Wire range 12 to 26 AWG.
Connections to Acromag non-intelligent carrier boards: P1, 50-pin male header with strain relief ejectors. Use Acromag 5025-550-x or 5025-551-x cable to connect panel to VME board. Keep cable as short as possible to reduce noise and power loss.
Mounting: Termination panel is snapped on the DIN mounting rail.
Printed Circuit Board: Military grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: -40°C to +100°C.
Storage Temperature: -40°C to +100°C.
Shipping Weight: 1.25 pounds (0.6kg) packed.

TRANSITION MODULE: MODEL TRANS-GP

Type: Transition module for AVME9630/9660 boards.
Application: To repeat field I/O signals of IP modules A through D for rear exit from VME card cages. This module is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. Connects to Acromag termination panel 5025-552 from the rear of the card cage, and to AVME9630/9660 boards within card cage, via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).
Schematic and Physical Attributes: See Drawing 4501-465.
Field Wiring: 50-pin header (male) connectors (3M 3433-D303 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to Acromag termination panel 5025-552 from the rear of the card cage, or to AVME9630/9660/9668 boards within card cage, via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).
Connections to AVME9630/9660: 50-pin header (male) connectors (3M 3433-1302 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to AVME9630/9660 boards within the card cage via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X). Transition module is inserted into a 6U-size, single-width slot at the rear of the VMEbus card cage.
Mounting: Transition module is inserted into a 6U-size, single-width slot at the rear of the VMEbus card cage.
Printed Circuit Board: Military grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: -40 to +85°C.
Storage Temperature: -55°C to +105°C.
Shipping Weight: 1.25 pounds (0.6Kg) packed.

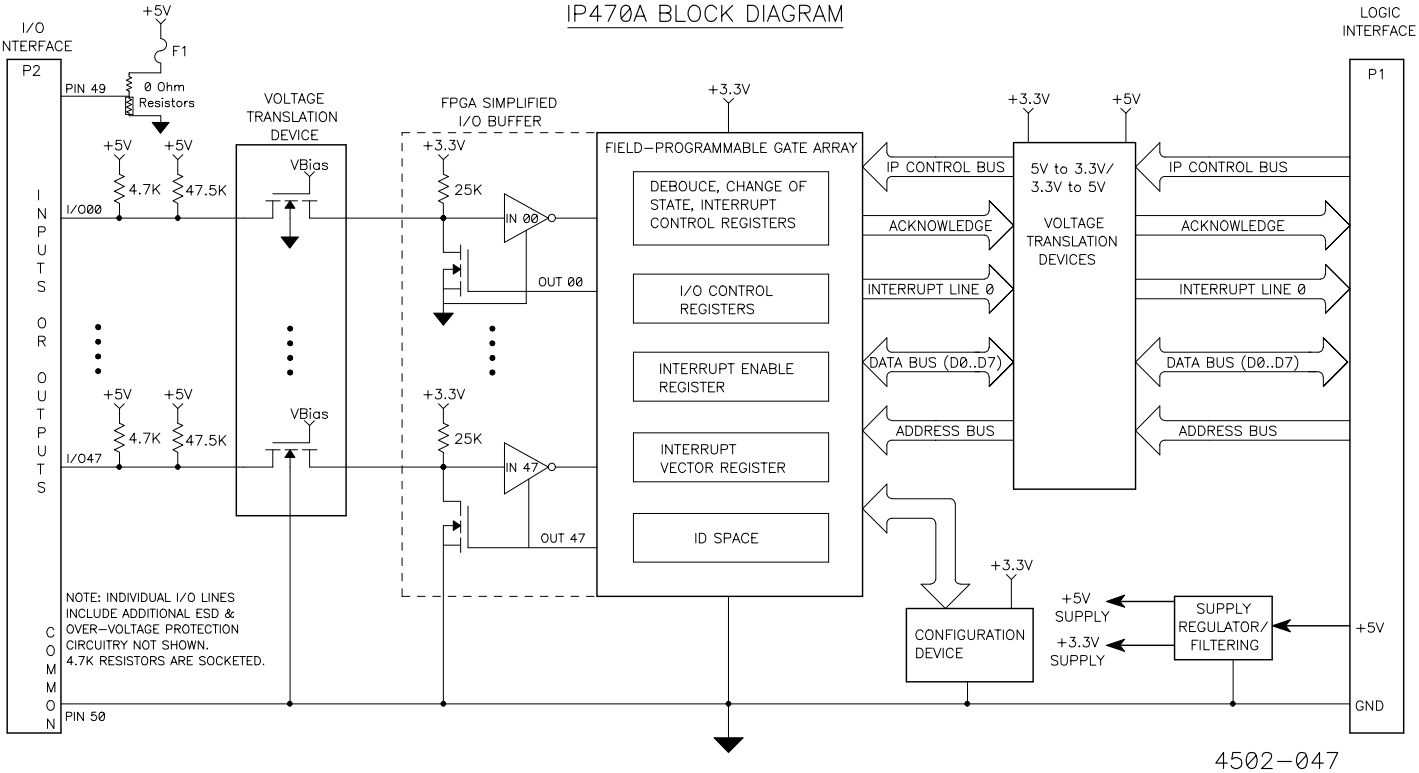


ASSEMBLY PROCEDURE:

1. THREADED SPACERS ARE PROVIDED IN TWO DIFFERENT LENGTHS. THE SHORTER LENGTH IS FOR USE WITH AVME 9630/9660 CARRIER BOARDS (SHOWN). CHECK YOUR CARRIER BOARD TO DETERMINE ITS REQUIREMENTS. MOUNTING HARDWARE PROVIDED MAY NOT BE COMPATIBLE WITH ALL TYPES OF CARRIER BOARDS.
2. INSERT FLAT HEAD SCREWS (ITEM A) THROUGH SOLDER SIDE OF IP MODULE AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES) UNTIL HEX SPACER IS COMPLETELY SEATED.
3. CAREFULLY ALIGN IP MODULE TO CARRIER BOARD AND PRESS TOGETHER UNTIL CONNECTORS AND SPACERS ARE SEATED.
4. INSERT PAN HEAD SCREWS (ITEM C) THROUGH SOLDER SIDE OF CARRIER BOARD AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES).

IP MODULE TO CARRIER BOARD MECHANICAL ASSEMBLY 4501-434B

IP470A BLOCK DIAGRAM

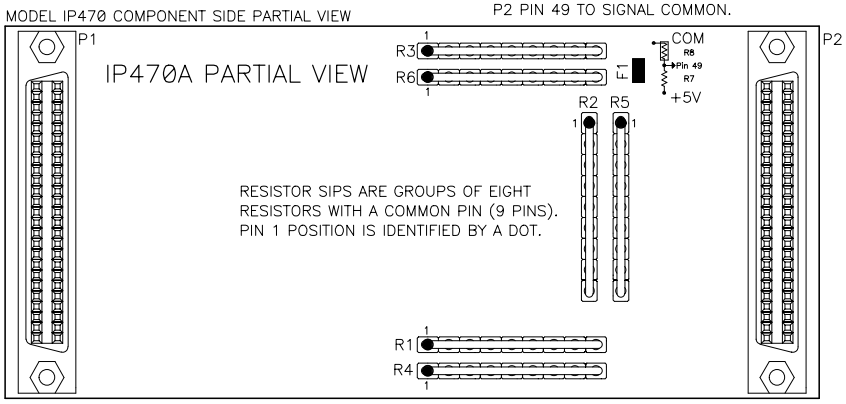


4502-047

IP470A PULLUP RESISTOR LOCATION DRAWING FOR REMOVAL AND REPLACEMENT WHERE REQUIRED

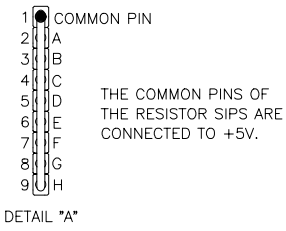
NOTE THAT 0 OHM RESISTOR R7 TIES P2 PIN 49 TO +5V. HOWEVER IT MAY BE REMOVED AND 0 OHM RESISTOR R8 INSERTED TO TIE P2 PIN 49 TO SIGNAL COMMON.

MODEL IP470 COMPONENT SIDE PARTIAL VIEW



RESISTOR SIPS ARE MOUNTED IN SOCKETS AND CAN BE REMOVED IF REQUIRED.

RESISTOR SIPS ARE DIVIDED AS SHOWN



MODULE IS SHIPPED WITH ALL SIP RESISTORS INSTALLED

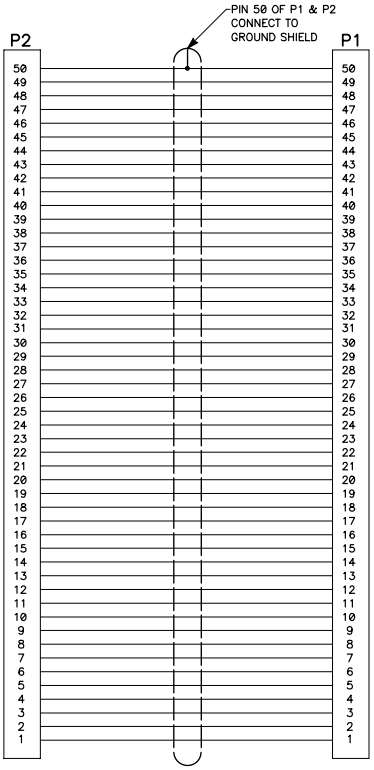
NOTES CONCERNING PULLUP RESISTORS R1–R6, ZERO OHM RESISTORS R7–R8, AND FUSE F1:

1. ALL I/O POINTS INCLUDE OPEN DRAIN OUTPUT CIRCUITRY WITH 4.7K OHM PULLUP RESISTORS TO +5V IN THE FORM OF SIP RESISTORS AS SHOWN. THESE SIP RESISTORS ARE INSTALLED IN SOCKETS AND MAY BE MODIFIED AS REQUIRED.
2. ZERO OHM RESISTOR R7 TIES P2 PIN 49 TO +5V THROUGH FUSE F1. ALTERNATELY, R7 CAN BE REMOVED AND R8 CAN BE INSERTED TO TIE P2 PIN 49 TO GROUND. R7 AND R8 ARE 0805 0 OHM RESISTORS (ACROMAG PART 1400–214). MODEL IS SHIPPED WITH ONLY R7 INSTALLED (+5V TO P2 PIN 49).
3. FUSE F1 TIES P2 PIN 49 TO +5V THROUGH 0 OHM RESISTOR R7. F1 IS A 2 AMP LITTELFUSE NO. 466003NR OR EQUIVALENT (ACROMAG PART 1430–005).

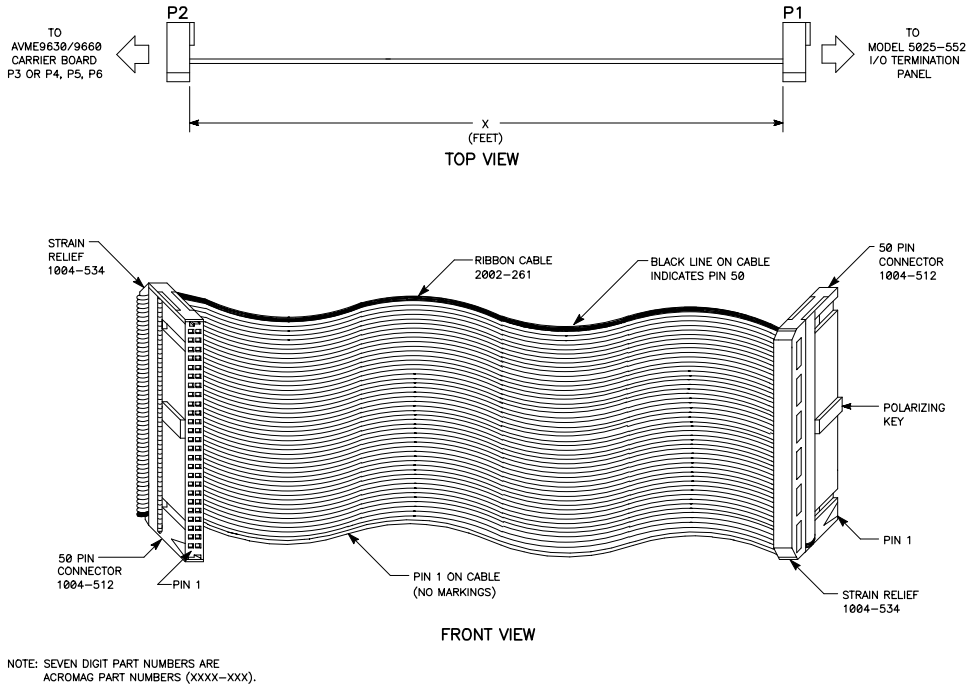
SIP RESISTOR IDENTIFICATION

SIP	VALUE	FUNCTION	PORT
R1:A...R1:H	4.7K OHM	I/O07...I/O00 PULLUP	PORT 0
R2:A...R2:H	4.7K OHM	I/O15...I/O08 PULLUP	PORT 1
R3:A...R3:H	4.7K OHM	I/O23...I/O16 PULLUP	PORT 2
R4:A...R4:H	4.7K OHM	I/O31...I/O24 PULLUP	PORT 3
R5:A...R5:H	4.7K OHM	I/O39...I/O32 PULLUP	PORT 4
R6:A...R6:H	4.7K OHM	I/O47...I/O40 PULLUP	PORT 5

4502–057



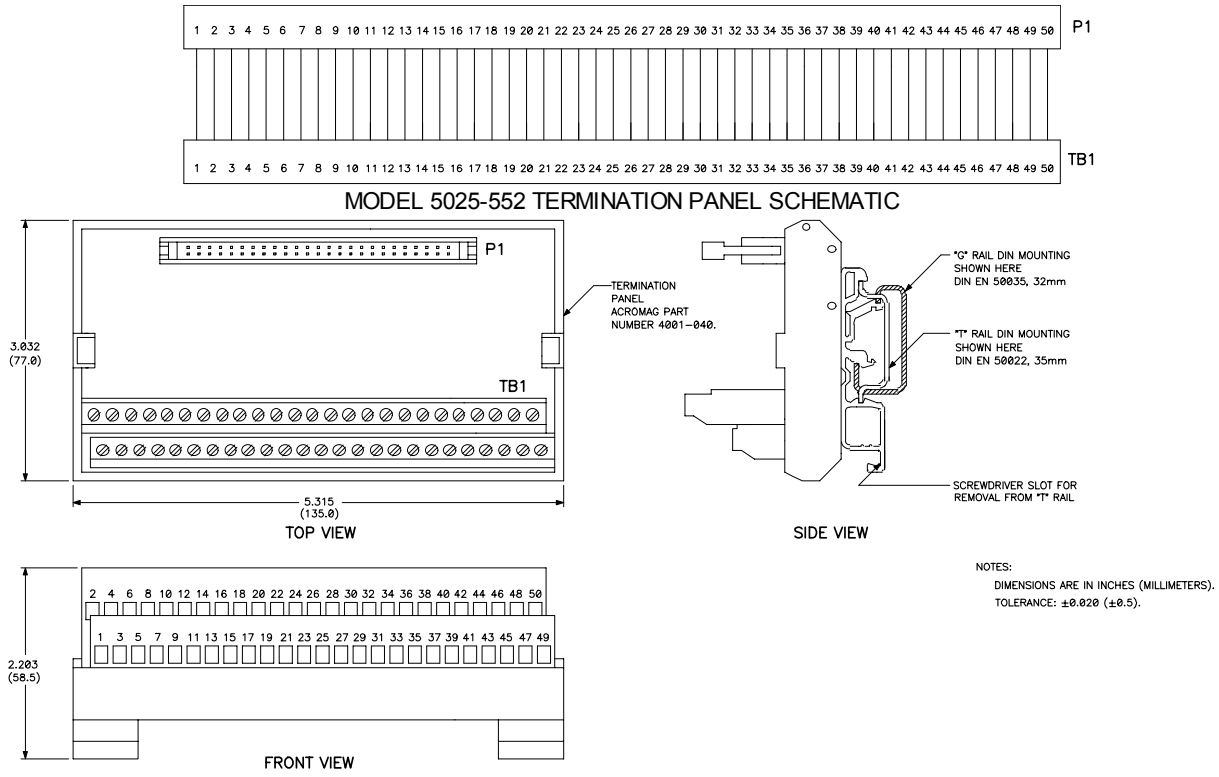
MODEL 5025-551-x SCHEMATIC



NOTE: SEVEN DIGIT PART NUMBERS ARE ACROMAG PART NUMBERS (XXXX–XXX).

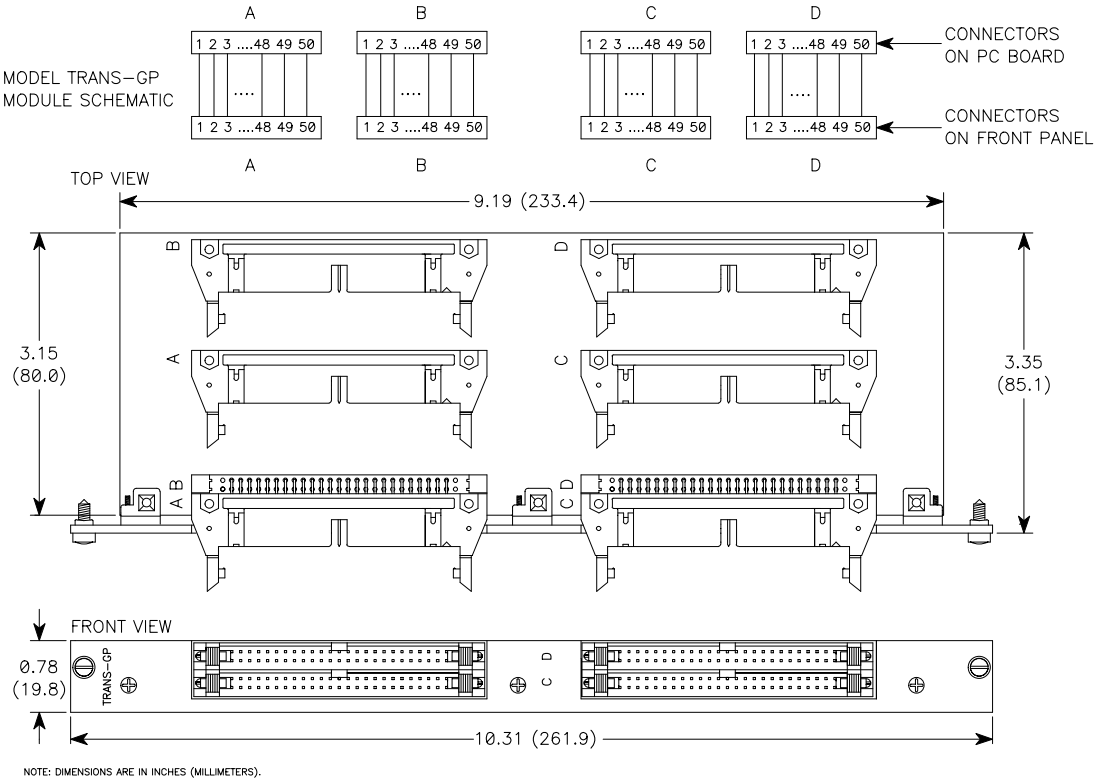
MODEL 5025-551-x SIGNAL CABLE, SHIELDED

4501-463A



MODEL 5025-552 TERMINATION PANEL SCHEMATIC

MODEL 5025-552 TERMINATION PANEL 4501-464A



TRANS-GP MECHANICAL DIMENSIONS AND SIMPLIFIED SCHEMATIC 4501-465A