VMIVME-3122

HIGH-PERFORMANCE 16-BIT ANALOG-TO-DIGITAL CONVERTER BOARD

PRODUCT MANUAL

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RECORD OF REVISIONS

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SAFETY SUMMARY

THE FOLLOWING GENERAL SAFETY PRECAUTIONS MUST BE OBSERVED DURING ALL PHASES OF THIS OPERATION, SERVICE, AND REPAIR OF THIS PRODUCT. FAILURE TO COMPLY WITH THESE PRECAUTIONS OR WITH SPECIFIC WARNINGS ELSEWHERE IN THIS MANUAL VIOLATES SAFETY STANDARDS OF DESIGN, MANUFACTURE, AND INTENDED USE OF THIS PRODUCT. VME MICROSYSTEMS INTERNATIONAL CORPORATION ASSUMES NO LIABILITY FOR THE CUSTOMER'S FAILURE TO COMPLY WITH THESE REQUIREMENTS.

GROUND THE SYSTEM

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY SYSTEM

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VME Microsystems International Corporation for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

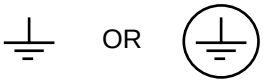
DANGEROUS VOLTAGES, CAPABLE OF CAUSING DEATH, ARE PRESENT IN THIS SYSTEM. USE EXTREME CAUTION WHEN HANDLING, TESTING, AND ADJUSTING.

SAFETY SYMBOLS

GENERAL DEFINITIONS OF SAFETY SYMBOLS USED IN THIS MANUAL

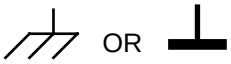
Instruction manual symbol: the product is marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the system.

Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts are so marked).



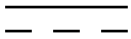
Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.

Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.

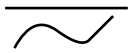


Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.

Alternating current (power line).



Direct current (power line).



Alternating or direct current (power line).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

```
**************
*  CAUTION   *
**************
```

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE:

The NOTE sign denotes important information. It calls attention to a procedure, a practice, a condition, or the like, which is essential to highlight.

VMIVME-3122
HIGH PERFORMANCE 16-BIT ANALOG TO DIGITAL CONVERTER BOARD

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

LIST OF FIGURES

TABLE OF CONTENTS (Concluded)

LIST OF TABLES

APPENDIX

SECTION 1

INTRODUCTION

1.1 GENERAL DESCRIPTION

The VMIVME-3122 Board is a member of VMIC's extensive family of analog input/output products for the VMEbus. With 16-bit digitizing resolution, program-controlled gain, selectable conversion rate, and automatic scanning of 64 differential or single-ended analog inputs, the VMIVME-3122 Board provides exceptional dynamic range and analog input channel density. Various operating modes are supported, including autoscanning, data bursts, and external synchronization. This board is designed to interface directly with VMIC's line of signal conditioning boards for digitizing the outputs from thermocouples, RTDs, and strain gages.

Individual channel gains can be downloaded for use during scanning operations, or the board can be configured with a fixed gain that is common to all channels. Multiple boards can be synchronized together to enable as many as 16 boards to initiate each scan simultaneously. An Interval Timer, Bus Interrupter, Channel Counter, and Midscan/Endscan flag simplify the monitoring of data within the dual port data buffer. The system applications that can benefit from the VMIVME-3122 capabilities include factory automation, process control, data acquisition systems, training simulators, and laboratory instrumentation. The following brief overview of principal features illustrates the flexibility and performance that is available with the VMIVME-3122 Board:

a. 16, 32, or 64 differential or single-ended analog inputs
b. 16-bit A/D conversion
c. 381Hz to 100 kHz selectable scanning rate
d. Programmable gains of x1 or x10
e. A/D converter ranges of ±2.5 V, ±5 V, ±10 V, 0 to +5 V, 0 to +10 V
f. Programmable channel gains
g. 16- to 1,024-word dual port data buffer
h. Operation in short I/O (A16), standard (A24), or extended (A32) data space
i. Programmable channel block size and buffer size
j. Optional low pass input filters
k. Continuous and burst operating modes
l. Free running operation or external/internal triggering
m. Bus interrupter for Midscan or Endscan indication
n. Programmable interval timer for timed data bursts
o. Direct cabling from VMIC signal conditioning boards
p. Initializes after a reset in autoscan mode with gain = x1

1.2 FUNCTIONAL DESCRIPTION

The VMIVME-3122 (Figure 1.2-1) is a high-resolution, 16-bit, 64-channel Analog Scanning and Digitizing Input board for VMEbus system applications. Dual-ported data memory, on-board timers, automatically controlled gain, and a programmable bus interrupter enable the VMIVME-3122 Board to support extensive analog input traffic, with minimum involvement of the host processor.

Analog inputs are scanned and digitized sequentially. The digital values are stored in a dual port data buffer which can be accessed at any time from the VMEbus. The gain of each channel can be programmed individually, or can be set in software for a fixed gain that is common to all channels. Channel gain is software selectable as x1 or x10. A/D converter voltage ranges are jumper-selectable for ±2.5 V, ±5 V, ±10 V, 0 to 5 V, 0 to 10 V.

When a system or program reset occurs, the board initializes in the 64-channel autoscanning mode at a rate of 100 kHz and all channel gains are initialized to unity (x1). After a reset operation, the program can select the timed burst or triggered burst modes, and can modify the block size, buffer size, and channel gains as necessary. The channel block is adjustable as 1, 8, 16, 32, or 64 channels, and the data buffer size can be selected from 16 to 1,024 data words in binary increments.

Timed data bursts are controlled by an interval timer which can provide repetitive or single-shot burst intervals of up to 687 sec. A burst can consist of from 8 to1,024-channel samples. A data ready flag is available at the middle or end of a scan, and an interrupt request can be generated simultaneously with the flag. The interrupt can also be initiated after a specific number of samples have been acquired.

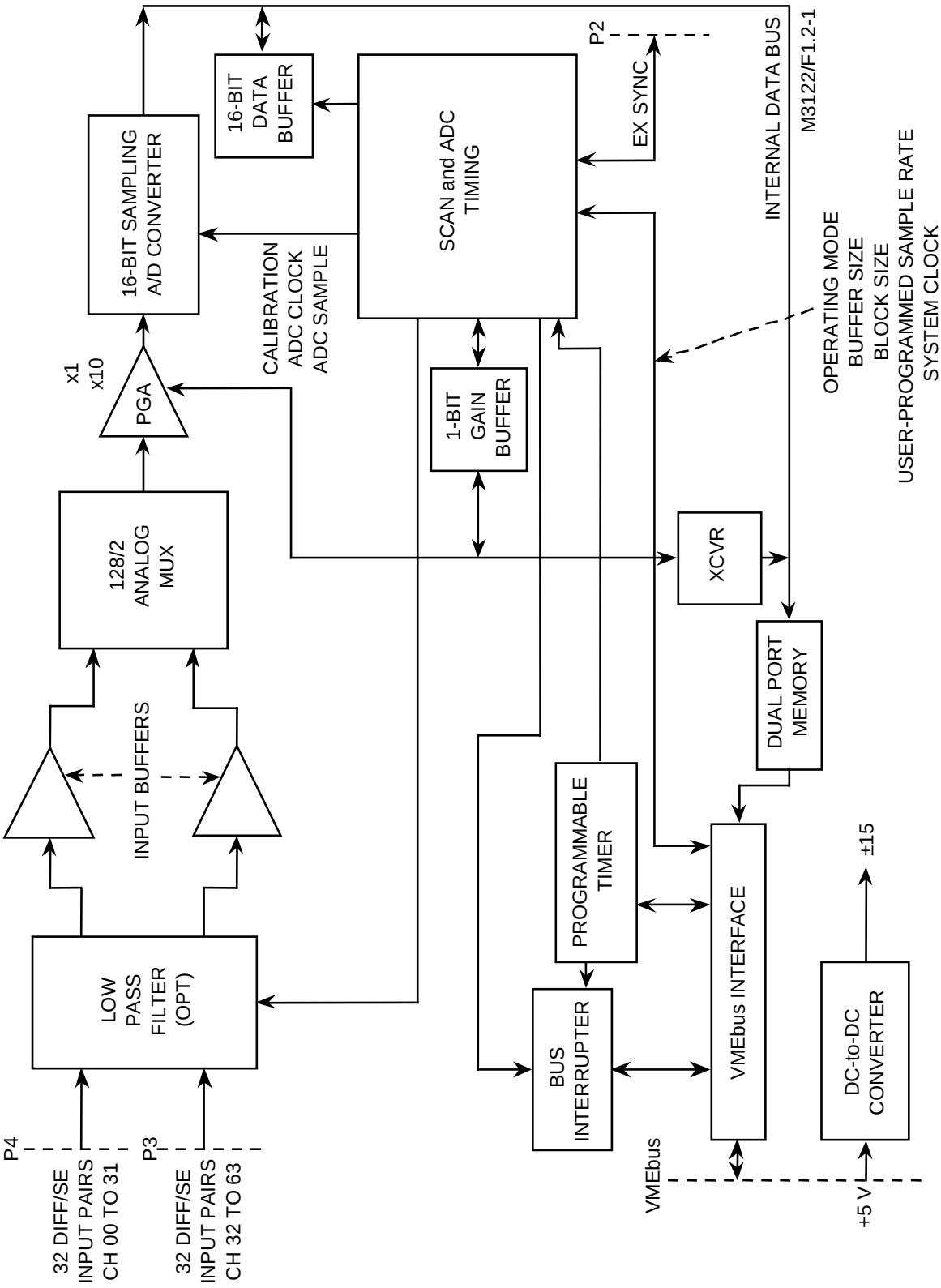


Figure 1.2-1. VMIVME-3122 Functional Block Diagram

1.3 REFERENCE MATERIAL LIST

For a detailed explanation of the VMEbus and its characteristics, the publication “The VMEbus Specification” is available from:

VITA
VFEA International Trade Association
10229 N. Scottsdale Road
Scottsdale, AZ 85253
(602) 951-8866

The following Application and Configuration Guides are available from VMIC to assist in the selection, specification, and implementation of systems based upon VMIC’s products:

TITLE	DOCUMENT NO.
Digital Input Board Application Guide	825-000000-000
Change-of-State Application Guide	825-000000-002
Digital I/O (with Built-in-Test) Product Line Description	825-000000-003
Synchro/Resolver (Built-in-Test) Subsystem Configuration Guide	825-000000-004
Analog I/O Products (with Built-in-Test) Configuration Guide	825-000000-005
Connector and I/O Cable Application Guide	825-000000-006

SECTION 2

PHYSICAL DESCRIPTION AND SPECIFICATIONS

REFER TO 800-003122-000 SPECIFICATION

SECTION 3

THEORY OF OPERATION

3.1 INTRODUCTION

This section describes the internal organization of the VMIVME-3122 board, and reviews the general principles of operation. Section 3.2 summarizes the major board functions, and the remainder of Section 3 addresses each function individually. The information in this section is supplemented by programming details in Section 4 and by the schematic diagrams in Appendix A.

3.2 INTERNAL FUNCTIONAL ORGANIZATION

The VMIVME-3122 board contains the following principal hardware functions, as shown in Figure 1.2-1 of Section 1:

a. Analog input multiplexing and digitizing
b. VMEbus interface
c. Scan timing and control
d. Data and gain buffers
e. Interval timer and channel counter (Intel 8254)
f. Bus interrupter
g. Power converter

Input Buffers, Analog Multiplexers, a Programmable Amplifier, and a 16-bit A/D Converter digitize the analog input channels. The digitized values are stored in a dual-ported data buffer for access from the VMEbus. Optional low pass input filters minimize the effects of system noise and eliminate high frequency signal components which would otherwise cause accuracy problems. Input Buffers eliminate the error associated with varying source resistance. The scan rate is selectable from 381 Hz to 100 kHz according to the scan rate equations in Section 4.3.4. Operating modes are described in detail in Section 4.5. Regulated ±15 VDC power for the analog networks is obtained from the 5 VDC bus through a DC-to-DC Converter.

A separate gain buffer permits the input gain of each channel to be assigned individually. Gain codes ($0 = x1, $1 = x10) are first loaded into the gain buffer from the bus, and the gain for each channel is then used during the scanning process. A fixed gain for all channels can also be software programmed if programmable gain per channel is not required.

Control signals and data transfers take place through the VMEbus P1 and P2 connectors. VMEbus Interface Logic controls data transfers through the P1 and P2 interface, and latches the operating mode parameters. Status monitoring and sequence timing are supported by a Bus Interrupter and Programmable Timer, both of which are controlled from the bus. Scan timing logic controls the analog input scanning process, uses the gain buffer to adjust input gain, sets the sampling rate, and routes digitized channel data to the data buffer.

3.3 CONTROL INTERFACE

3.3.1 Board Selection

VMEbus data transfer requests are accepted when the Board-Selection Comparator detects a match between the on-board selection jumpers shown in Figure 3.3.1-1, and the address and address modifier lines from the backplane. When a match is detected, the board responds with a data transfer, after which the open collector DTACK interface signal is asserted (LOW). DTACK returns to the negated (HIGH) state when the transfer has been completed. During an interrupt response, DTACK is provided by the interrupt controller.

3.3.2 Read/Write Operations

Data Bus lines D00 through D15 are bi-directional and move data to or from the board through a 16-bit Data Transceiver in response to control signals from Interface Timing and Control Logic. The data transceiver isolates the VMEbus data lines from the Internal Data Bus. Address lines A12 through A31 map the board into either short I/O A16 space, standard A24 space or extended A32 space. Data transfer control signals from the VMEbus determine whether data is moved to the board (Write) or from the board (Read). Both D8 (EO) and D16 transfers are supported.

There are several registers on the board which control operational mode, buffer and block size, interrupt sources, gain mode, sample rate, and trigger mode. These various registers are described individually in Section 4.

3.3.3 Bus Interrupter

Access to the VMEbus interrupt structure is provided through a Bus Interrupter. If the interrupt is enabled, an interrupt is generated in response to a request either by the scan timing logic as a data ready flag, or by the channel counter after a specific number of buffer locations have been updated. The interrupt function is implemented inside the EPM7160 Programmable Logic Device. Details of the interrupter capabilities are described in Section 4.

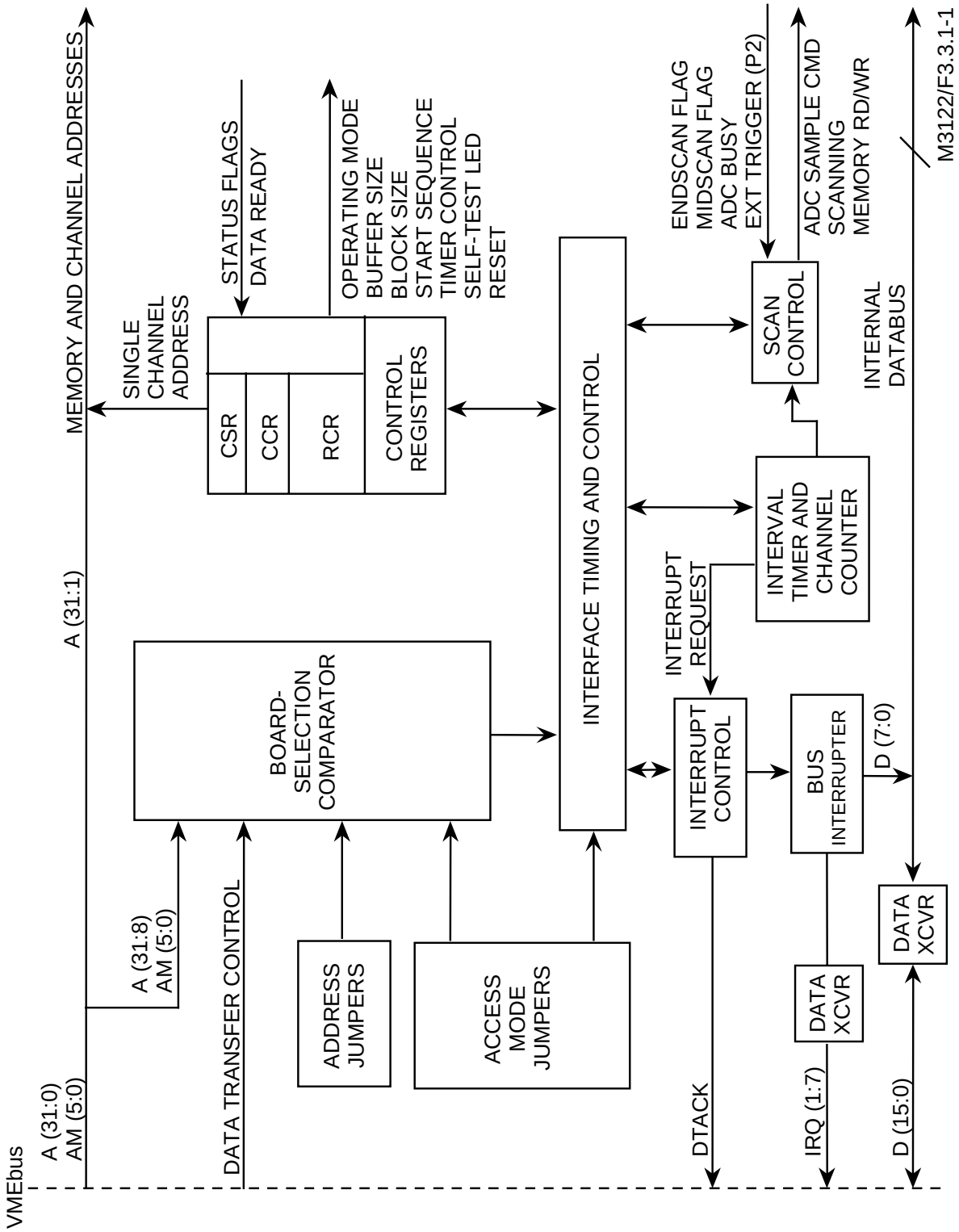


Figure 3.3.1-1. VMEbus Interface Logic

3.3.4 Interval Timer and Channel Counter

A triple 16-bit counter device contains the Interval Timer and Channel Counter. Two of the counter sections are driven from an 6.25 MHz clock, and can be cascaded as a 32-bit timer for delays up to 687 seconds. Timed data acquisition bursts (see Sections 3.6 and 4.5) occur at the interval programmed into the Interval Timer. The channel counter can be programmed to generate an interrupt after a programmed number of data buffer locations have been updated, or can be read directly to serve as a data pointer.

3.4 DATA BUFFER MEMORY

3.4.1 Organization and Control

Digitized inputs are stored in a 16-bit data buffer, the size of which can be software configured from 8 data words to 1,024 data words. Data in the buffer is organized into consecutive channel blocks, each of which represents a complete scan of all active channels.

Both buffer size and block size are controlled by the Configuration Control (CCR). The input channels are sampled consecutively, starting with Channel 00 located at the bottom (lowest address) of each block in the buffer, and proceeding through the highest channel at the top of the block.

The total address space of the VMIVME-3122 is 4096 bytes. Memory located at offset address $0880 to $0FFE is available as on-board scratch pad memory.

3.4.2 Data Storage and Retrieval

The data buffer can be loaded or read from the bus at any time. Arbitration for the buffer occurs at the beginning of an update from the A/D converter. If the converter has control of the memory when a bus transfer is initiated, the transfer will be extended by approximately 250 nsec while the buffer update is completed.

If a bus transfer is in progress when a converter access is requested, the bus transfer will proceed normally and the converter access will take place after the transfer has been completed.

A data ready flag can be programmed to occur at the end of the buffer, or can be programmed to occur at the middle of the buffer. The data ready flag can initiate an interrupt request, or can be read from the bus as a status flag.

3.5 OPERATING MODES

All operating modes available with the VMIVME-3122 are controlled through the Control and Status Register (CSR) and the Configuration Control Register (CCR). The operating modes are a combination of trigger modes from the CSR and scan mode from the CCR. Operating modes are described in detail in Section 4, and are summarized here as trigger and scan modes:

Trigger Modes
a. Software Trigger
b. External Trigger
c. Interval Timer Trigger

Software Trigger is selected by clearing both trigger mode control bits in the CSR. With both bits cleared, a write command to the Software Trigger Command register located at relative address $000E causes the selected scan mode to begin.

External Trigger is selected by clearing trigger mode bit 13 and setting trigger mode bit 12. This enables the board to accept an external trigger. Upon receiving the external trigger, the selected scan mode is initiated.

Interval Timer Trigger is selected by setting bit 13 and clearing bit 12. This setting enables the interval timer and the selected scan mode is initiated each time the timer programmed time interval expires.

Scan Modes
a. Autoscan
b. Single Scan
c. Random Access

Autoscan is selected by clearing both scan mode control bits in the CCR and is the default selection after a reset operation. All active channels are scanned continuously in this mode.

Single Scan is selected by clearing scan mode control bit 7 and setting bit 6. All active channels are scanned through once, and the scan process is stopped until the next trigger event.

Random Access is selected by setting bit 7 and letting bit 6 be a Don’t Care. In this mode, a channel is selected by entering the channel number in bits D05-D00 in the CCR. This desired channel is sampled, digitized, and stored at RAM offset address $0080.

3.6 ANALOG INPUT MULTIPLEXING, SAMPLING, AND DIGITIZING

3.6.1 Input Configuration

Analog inputs from connectors P3 and P4 are routed through low pass Input Filters and OP AMP Buffers to the input multiplexers shown in Figure 3.6.1-1. Channels 00 to 31 are connected through P4 and Channels 32 to 63 are connected through P3. To provide at least one ground in each of the input connectors, the LOW inputs for Channels 31 and 63 can be jumpered individually to AGND, or can be left ungrounded (see Sections 5.4 and 5.6). AGND is the internal analog ground. The center row (B row) pins on P3 and P4 are connected to AGND. This provides a return for all channels if 96-wire ribbon cables are used for the analog inputs.

The Analog Multiplexers route one of each group of eight channels to the PGA multiplexers, which in turn selects an input to route to the PGA. Input address lines A0 and A1 control the input multiplexer, while A3, A4, and A5 select the PGA multiplexer input. Each input multiplexer has an individual enable signal which enables the multiplexer with the desired channel.

Crosstalk and source impedance errors are minimized by the input OP AMP Buffers. The buffers provide a constant low impedance to the multiplexer inputs. Each channel contains a buffer on each input line.

3.6.2 Gain Control

The Programmable Gain Amplifier (PGA) applies a gain of x1 or x10 to the differential channel from the PGA multiplexer, and produces a single-ended output. PGA gain is selected by the GAIN_X1_L control line (Section 3.2).

3.6.3 Analog-to-Digital Conversion

The output of the PGA is buffered by a unity gain buffer and digitized by the 16-bit successive approximation A/D Converter shown in Figure 3.6.3-1a. The ADC has a built-in sample and hold. Each conversion is initiated by the sample command, and the read ADC strobe writes the digitized value to the data buffer through the internal data bus. Total conversion time is 10 µsec at the highest sample rate available. The sample command takes 2 µsec, leaving 8 µsec for actual A/D conversion. The ADC timing is shown in Figure 3.6.3-1b.

3.7 POWER CONVERTER

Electrical power for the analog networks is supplied by a single DC-to-DC converter which converts 5 VDC logic power from the VMEbus into isolated and regulated ±15 VDC. This product does not require the optional ±12 V on the VMEbus backplane.

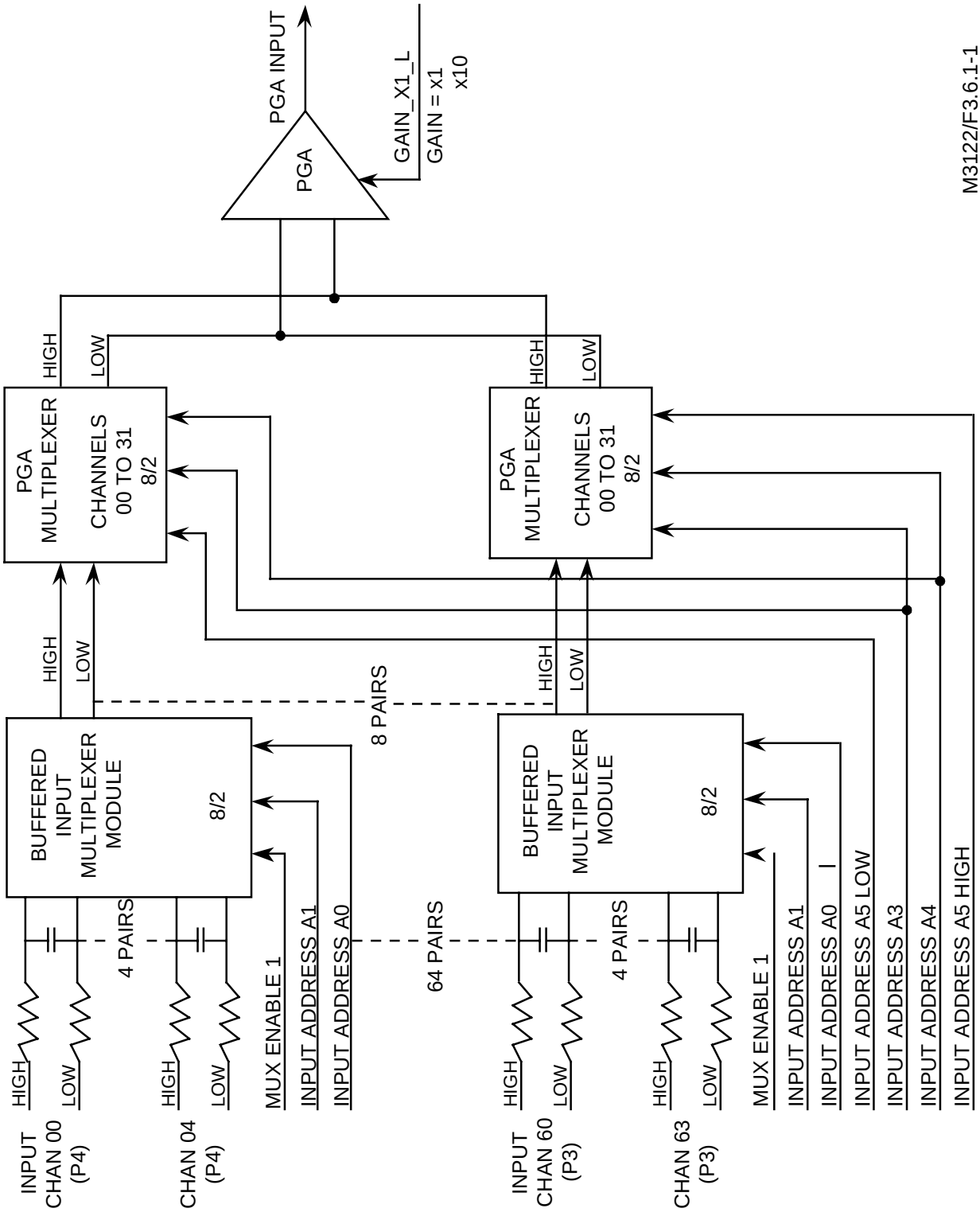


Figure 3.6.1-1. Analog Multiplexers and PGA

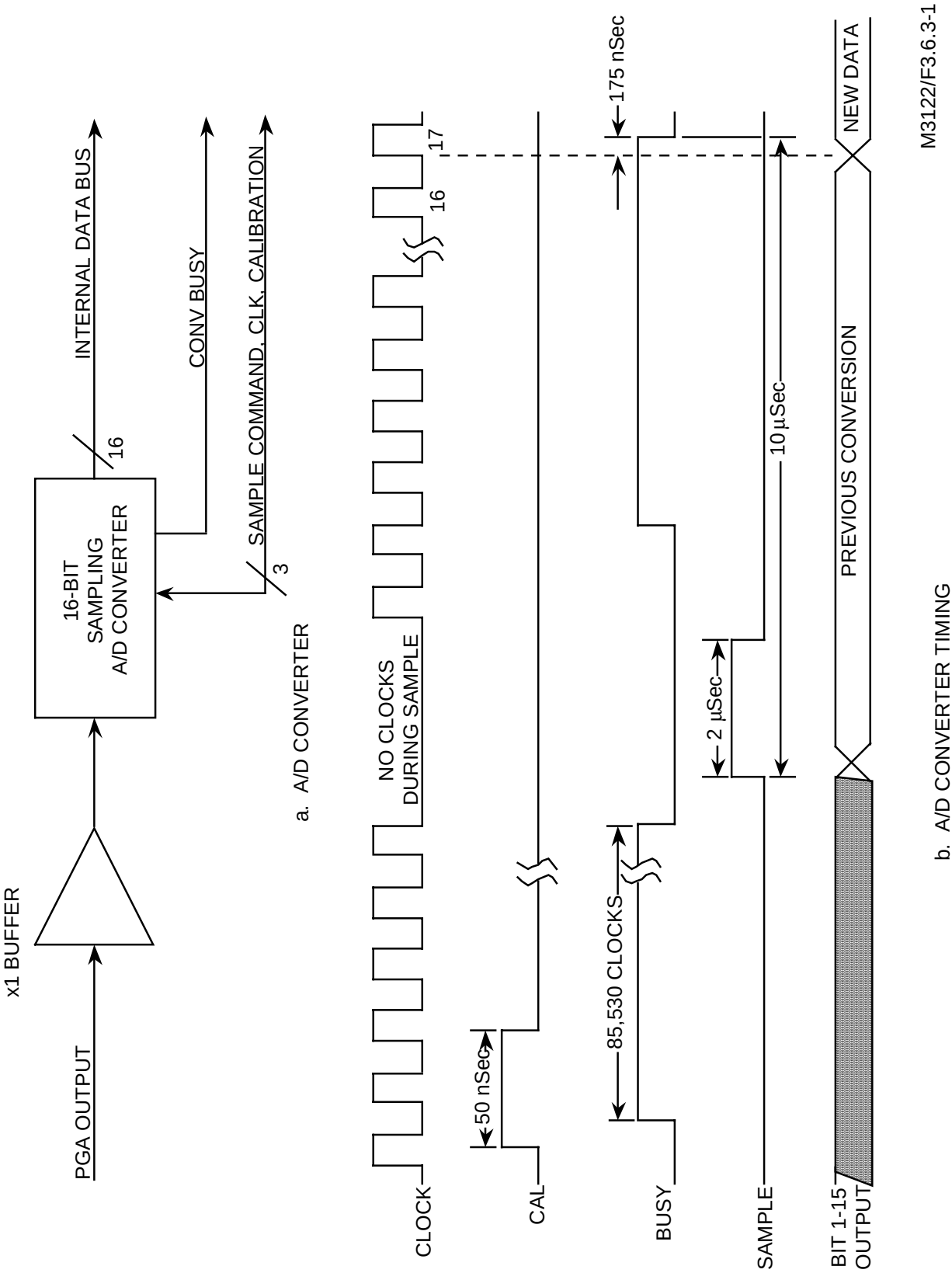


Figure 3.6.3-1. A/D Converter and Timing

SECTION 4

PROGRAMMING

4.1 INTRODUCTION TO CONTROLLING THE VMIVME-3122 BOARD

VMEbus communication takes place through Control/Status, Configuration, and Data registers which can be jumper located in either the A16 short I/O space, the A24 standard space, or the A32 extended address space. A resident bus interrupter is under program control and can be configured to generate any interrupt request from IRQ1 through IRQ7.

Digitized input data is accumulated in a dual port data buffer which consists of from 16 to 1,024 data words, where each data word contains the 16-bit digitized value of a single analog input channel. Data accumulates in the buffer in selectable blocks of 1, 8, 16, 32, or 64 input channels. Buffer size and block size both are under program control, and the buffer can be read at any time without affecting the scanning sequence.

Data scaling is adjustable with jumper-controlled voltage ranges. Channel gain is software programmable and can be fixed at x1 or x10 or can be set in the Auto Gain mode which uses the gain buffer. A data ready flag can be programmed to occur when the buffer is either full or half-full. An interrupt can be generated simultaneously with the data ready flag, or after a specific number of samples have been acquired.

The analog inputs can be scanned continuously or in triggered data bursts. Bursts (single scans) can be acquired automatically at intervals up to 687 seconds, or can be triggered by an external event. Single channel random access is also supported. Various block size/buffer size combinations are available to add versatility to the board.

References to programming jumpers are made throughout this section. Jumper installation requirements are described in Section 5.

4.2 GENERAL CONTROL FEATURES

4.2.1 Addressing Modes and Board Location

Programmable address jumpers permit the VMIVME-3122 Board to be located in either the short I/O (A16) space, the standard address (A24) space, or the extended address (A32) space.

The board can be located on any 2048-word boundary. Access privilege is jumper-designated as supervisory, nonprivileged, or either supervisory or nonprivileged.

4.2.2 Data Transfers

Data transfers respond to both D8 (EO) and D16 transfers.

Any register or buffer location can be read at any time without affecting the existing scanning sequence.

4.2.3 Reset Operations and Initialization

All Control Registers are reset by a VMEbus system reset. All control registers except Interrupt Control Register (ICR) and Interrupt Vector Register (IVR) are reset by writing to location $000C. Either reset operation initializes the board to the following configurations:

a. Continuous scanning operating mode at 100 kHz rate
b. 64-channel block size (32 for 32-channel option, 16 for 16-channel option)
c. 64-data word buffer size (32 for 32-channel option, 16 for 16-channel option)
d. Automatic gain set to x1
e. Offset binary data coding
f. Self-test LED ON
g. Data Ready flag at end-of-buffer

The Analog-to-Digital Converter (ADC) will go through a calibration cycle on either a system reset or software reset. The user can initiate a calibration cycle by writing to location $000C. The data written to this location is arbitrary. If the automatic gain mode has been selected in the Configuration Control Register, channel gains other than x1 must be programmed as described in Section 4.3.9.

4.2.4 Conventions

a. Hexadecimal Notation: To be consistent with conventional VMEbus development system nomenclature, hexadecimal numbers throughout this document are indicated with the prefix “$” unless otherwise indicated, and are expressed in byte “$XX”, word “$XXXX” or longword “$XXXX XXXX” formats. Decimal numbers are presented without a designating prefix.

b. Logic States: This document uses the convention that a data bit or control line is “SET” when it is in the “1”, or HIGH state, and is “CLEARED” when “0” or LOW.

4.3 CONTROL REGISTERS

Register designations and locations are summarized in Table 4.3-1.

Table 4.3-1. VMIVME-3122 Board Register Map

Register Address (Hex)	Register Designation	DESIG	Access
$0000	Board Identification Register	BIR	R
$0002	Control and Status Register	CSR	R/W
$0004	Configuration Control Register	CCR	R/W
$0006	Rate Control Register	RCR	R/W
$0008	Interrupt Control Register	ICR	R/W
$000A	Interrupt Vector Register	IVR	R/W
$000C	Software Reset Command	SRC	W
$000E	Software Trigger Command	STC	W
$0010	Auto Gain	GAIN	R/W
$0012 to 001E	Reserved	-	N/A
$0020	Interval Timer 0 Register	TR0	R/W
$0022	Interval Timer 1 Register	TR1	R/W
$0024	Data Counter Register	DCR	R/W
$0026	Timer Control Register	TCR	W
$0028 to $007E	Reserved	-	NA
$0080 to $087E	Data Buffer	BUFF	R/W
$0880 to $0FFE	Scratch Pad Memory	RAM	R/W

M3122/T4.3-1

4.3.1 Board ID Register (BIR)

The Board ID Register is a fixed, read only data register. The contents of this register identifies the VMIVME-3122. The board ID for the VMIVME-3122 is $2EXX, where XX is defined in Table 4.3.1-2.

Table 4.3.1-1. Board ID Register Bit Map

Board ID Register (0ffset $0000) Read Only, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
0	0	1	0	1	1	1	0

Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
0	0	0	0	0	0	BIR 1	BIR 0

M3122/T4.3.1-1

Table 4.3.1-2. Board ID Register Channel Options

VMIVME-3122 (Options)	Number of Channels	Condition	BIR 1	BIR 0
X0X	64	High Performance	0	0
X1X	32	High Performance	0	1
X2X	16	High Performance	1	0
X3X	64	Standard Performance	0	0
X4X	32	Standard Performance	0	1
X5X	16	Standard Performance	1	0

M3122/T4.3.1-2

4.3.2 Control and Status Register (CSR)

Table 4.3.2-1. Control and Status Register Bit Map

Control and Status Register (0ffset $0002) Read/Write, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
LED Off	Data FMT	Tmode 1	Tmode 0	32b TMR	Flag	0	0

Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
CAL CMPLT	Data RDY	Armed	Triged	0	0	0	0

M3122/T4.3.2-1

Control And Status Register Bit Definitions

LED Off - A logical 1 written to this bit location causes the front panel status LED to be turned off. A logical 0 written to this bit location causes the front panel status LED to be turned on. (Default is logic 0.)

Data FMT - A logical 1 written to this bit location causes data to be stored in two's complement format. A logical 0 written to this bit location caused data to be stored in offset binary format. (Default is logic 0.)

Tmode [1:0] - Trigger Mode control bits. This field is used to select the trigger event as shown in Table 4.3.2-2. (Default is logic 00.)

Table 4.3.2-2. Trigger Event Modes

Selected Trigger Event	Tmode 1	Tmode 0
Software Trigger Command	0	0
External Trigger	0	1
Interval Timer Trigger	1	0
Reserved	1	1

M3122/T4.3.2-2

32b TMR - A logical 1 written to this bit location causes Interval Timer 1 and Interval Timer 0 to be configured as a 32-bit interval timer. A logical 0 written to this bit location enables only Interval Timer 0, providing a 16-bit interval counter. (Default is logic 0.)

Flag - A logical 1 written to this bit location causes the Data RDY flag to be activated at the middle of the data buffer. A logical 0 written to this location causes the Data RDY flag to be activated at the end of the data buffer. (Default is logic 0.)

CAL CMPLT - This bit is read only. A logical 1 indicates that the ADC calibration is complete. This bit is cleared at the beginning of an ADC calibration sequence initiated by a VMEbus reset, or a Software Reset Command.

Data RDY - This bit is read only. A logical 1 indicates that the scan is complete and the data buffer is ready to be read. This bit is cleared on any read access to addresses $0080 - $0FFE.

Armed - This bit is read only. A logical 1 indicates that the current scan mode is armed. This is cleared by a valid trigger, a VMEbus reset, or a Software Reset Command.

Triged - This bit is read only. A logical 1 indicates that a valid trigger has been received and the current scan mode is active. This bit is cleared by scan completion, a VMEbus reset, or a Software Reset Command.

4.3.3 Configuration Control Register (CCR)

Table 4.3.3-1. Configuration Control Register Bit Map

Configuration Control Register (Offset $0004) Read/Write, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
Bufc 4	Bufc 3	Bufc 2	Bufc 1	Bufc 0	I Source	Gmode1	Gmode 0

Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
Smode 1	Smode 0	Groupc 5	Groupc 4	Groupc 3	Groupc 2	Groupc 1	Groupc 0

M3122/T4.3.3-1

Configuration Control Register Bit Definitions

Bufc [4:0] - Buffer Configuration control bits. This field is used to configure the available buffer size/block size combinations.

Groupc [5:0] - Channel group control bits. This field is used to select which group of channels will be active for scanning. It is also used to enter the desired channel in Random Access mode. If the buffer field is loaded with $00, $03, $07, $0C, $11, or $16 the entire buffer will be filled with the channel indicated by the group field. This is similar to Random Access, except the entire buffer is filled and not just the first location. Examples on how to use the Configuration Control Register are shown in the following paragraphs.

I Source - A logical 1 written to this bit location causes a VMEbus interrupt request, when enabled, to be generated by the Data Counter. This allows an interrupt request to be generated when a programmed number of conversions have been completed. A logical 0 written to this location causes a VMEbus interrupt request, when enabled, to be generated by the Data RDY flag. This allows an interrupt request to be generated at the middle or the end of the data buffer. (Default is logic 0.)

Gmode [1:0] - Gain Mode control bits. This field is used to configure the channel gains as shown in Table 4.3.3-2. Fixed gains apply to all active channels. In Auto Gain mode the gain programmed into the channel x Auto Gain location is applied to channel x. (Default is logic 00.)

Table 4.3.3-2. Gain Mode Channel Gains

Gain Mode	Gmode 1	Gmode 0
Fixed x1	0	0
Fixed x10	0	1
Auto Gain Mode	1	X

M3122/T4.3.3-2

Smode [1:0] - Scan Mode configuration control bits. This field is used to configure either the Auto Scan mode, the Single Scan mode, or the Random Access mode as shown in Table 4.3.3-3. In Auto Scan mode the scan is re-armed and triggered each time the end of the buffer is reached. When the end of the buffer is reached in Single Scan mode, the scan is terminated until the next trigger event. In Random Access mode, the scan is disabled. At each trigger event a single channel, indicated by Groupc [5..0], is converted and the data placed in buffer location 0 (offset address $0080).

Table 4.3.3-3. Scan Mode Configuration

Scan Mode	Smode 1	Smode 0
Auto Scan mode	0	0
Single Scan mode	0	1
Random Access mode	1	X

M3122/T4.3.3-3

4.3.3.1 Examples on Using Configuration Control Register (CCR)

The VMIVME-3122 has a buffer size of 1024 Words that can be accessed via the VMEbus. The configuration of this buffer may be manipulated using the Configuration Control Register located at Offset $0004.

There are three terms used throughout this manual when discussing the configuration of the data buffer. The terms are:

Buffer size: The VMEbus always has access to the entire set of 1024-words, but the user may program the number of buffer locations that will be updated when the VMIVME-3122 makes a scan of the selected inputs.

Possible values: 16, 32, 64, 128, 256, 512, 1024.

Block size: The Block size is the number of active channels that will be measured whenever the VMIVME-3122 makes a scan of the selected inputs.

Possible values:

1, 8, 16 whenever the buffer size = 16.
1, 8, 16, 32 whenever the buffer size = 32.
1, 8, 16, 32, 64 whenever the buffer size = 64 or larger.

Active Channels: The group of active channels that will be measured whenever the VMIVME-3122 makes a scan of the selected inputs.

Possible values:

Any channel whenever the block size = 1.
0-7, 8-15, 16-23, 24-31, 32-39, 40-47, 48-55, 56-63 whenever the block size = 8.
0-15, 16-31, 32-47, 48-63 whenever the block size = 16.
0-31, 32-63 whenever the block size = 32.
0-63 whenever the block size = 64.

The user may find the following to be of help when programming the buffer configuration of the VMIVME-3122.

The following legend applies.

1: This bit must be set to 1.
0: This bit must be set to 0.
I: This bit must be set as described under interrupt source.
G: The bit shown must be set as described under gain settings.
S: The bit shown must be set as described under scan mode.
C: The bits shown are utilized whenever a single channel is active, insert the channel number in HEX in these places.
X: The bit shown is a don't care, it may be set to a 1 or a 0.
A: Valid for 64 channel option.
B: Valid for 32 channel option.
C: Valid for 16 channel option.

Buffer Size 16 Words

The following values will be used whenever programming the VMIVME-3122 to fill a buffer of 16 words with data from a single channel. The user must specify the desired channel in the lower six bits of the register.

Block size of 1. 0000 0IGG SSCC CCCC

The following values will be used whenever programming the VMIVME-3122 to fill a buffer of 16 words with data from a block of 8 active channels. The user must specify which block of channels are active in the lower three bits of the register.

Block size of 8:

0000 1IGG SSXX X000	channels 0 through 7 are active.	(A,B,C)
0000 1IGG SSXX X001	channels 8 through 15 are active.	(A,B,C)
0000 1IGG SSXX X010	channels 16 through 23 are active.	(A,B)
0000 1IGG SSXX X011	channels 24 through 31 are active.	(A,B)
0000 1IGG SSXX X100	channels 32 through 39 are active.	(A)
0000 1IGG SSXX X101	channels 40 through 47 are active.	(A)
0000 1IGG SSXX X110	channels 48 through 55 are active.	(A)
0000 1IGG SSXX X111	channels 56 through 63 are active.	(A)

The following values will be used whenever programming the VMIVME-3122 to fill a buffer of 16 words with data from a block of 16 active channels. The user must specify which block of channels are active in the lower three bits of the register.

Block size of 16:

0001 0IGG SSXX X00X channels 0 through 15 are active. (A,B,C)
0001 0IGG SSXX X01X channels 16 through 31 are active. (A,B)
0001 0IGG SSXX X10X channels 32 through 47 are active. (A)
0001 0IGG SSXX X11X channels 48 through 63 are active. (A)

Buffer Size 32 Words

The following values will be used whenever programming the VMIVME-3122 to fill a buffer of 32 words with data from a single channel. The user must specify the desired channel in the lower six bits of the register.

Block size of 1. 0001 1IGG SSCC CCCC

The following values will be used whenever programming the VMIVME-3122 to fill a buffer of 32 words with data from a block of 8 active channels. The user must specify which block of channels are active in the lower three bits of the register.

Block size of 8:

0010 0IGG SSXX X000 channels 0 through 7 are active. (A,B,C)
0010 0IGG SSXX X001 channels 8 through 15 are active. (A,B,C)
0010 0IGG SSXX X010 channels 16 through 23 are active. (A,B)
0010 0IGG SSXX X011 channels 24 through 31 are active. (A,B)
0010 0IGG SSXX X100 channels 32 through 39 are active. (A)
0010 0IGG SSXX X101 channels 40 through 47 are active. (A)
0010 0IGG SSXX X110 channels 48 through 55 are active. (A)
0010 0IGG SSXX X111 channels 56 through 63 are active. (A)

The following values will be used whenever programming the VMIVME-3122 to fill a buffer of 32 words with data from a block of 16 active channels. The user must specify which block of channels are active in the lower three bits of the register.

Block size of 16:

0010 1IGG SSXX X00X channels 0 through 15 are active. (A,B,C)
0010 1IGG SSXX X01X channels 16 through 31 are active. (A,B)
0010 1IGG SSXX X10X channels 32 through 47 are active. (A)
0010 1IGG SSXX X11X channels 48 through 63 are active. (A)

The following values will be used whenever programming the VMIVME-3122 to fill a buffer of 32 words with data from a block of 32 active channels. The user must specify which block of channels are active in the lower three bits of the register.

Block size of 32:

0011 0IGG SSXX X0XX channels 0 through 31 are active. (A,B)
0011 0IGG SSXX X1XX channels 32 through 63 are active. (A)

Buffer Size 64 Words

The following values will be used whenever programming the VMIVME-3122 to fill a buffer of 64 words with data from a single channel. The user must specify the desired channel in the lower six bits of the register.

Block size of 1. 0011 1IGG SSCC CCCC

The following values will be used whenever programming the VMIVME-3122 to fill a buffer of 64 words with data from a block of 8 active channels. The user must specify which block of channels are active in the lower three bits of the register.

Block size of 8:

0100 0IGG SSXX X000 channels 0 through 7 are active. (A,B,C)
0100 0IGG SSXX X001 channels 8 through 15 are active. (A,B,C)
0100 0IGG SSXX X010 channels 16 through 23 are active. (A,B)
0100 0IGG SSXX X011 channels 24 through 31 are active. (A,B)
0100 0IGG SSXX X100 channels 32 through 39 are active. (A)
0100 0IGG SSXX X101 channels 40 through 47 are active. (A)
0100 0IGG SSXX X110 channels 48 through 55 are active. (A)
0100 0IGG SSXX X111 channels 56 through 63 are active. (A)

The following values will be used whenever programming the VMIVME-3122 to fill a buffer of 64 words with data from a block of 16 active channels. The user must specify which block of channels are active in the lower three bits of the register.

Block size of 16:

0100 1IGG SSXX X00X channels 0 through 15 are active. (A,B,C)
0100 1IGG SSXX X01X channels 16 through 31 are active. (A,B)
0100 1IGG SSXX X10X channels 32 through 47 are active. (A)
0100 1IGG SSXX X11X channels 48 through 63 are active. (A)

The following values will be used whenever programming the VMIVME-3122 to fill a buffer of 64 words with data from a block of 32 active channels. The user must specify which block of channels are active in the lower three bits of the register.

Block size of 32:

0101 0IGG SSXX X0XX channels 0 through 31 are active. (A,B)
0101 0IGG SSXX X1XX channels 32 through 63 are active. (A)

The following values will be used whenever programming the VMIVME-3122 to fill a buffer of 64 words with data from a block of 64 active channels. The user must specify which block of channels are active in the lower three bits of the register.

Block size of 64:

0101 1IGG SSXX XXXX channels 0 through 63 are active. (A)

Buffer Size 128 Words

The following values will be used whenever programming the VMIVME-3122 to fill a buffer of 128 words with data from a single channel. The user must specify the desired channel in the lower six bits of the register.

Block size of 1. 0110 0IGG SSCC CCCC

The following values will be used whenever programming the VMIVME-3122 to fill a buffer of 128 words with data from a block of 8 active channels. The user must specify which block of channels are active in the lower three bits of the register.

Block size of 8:

0110 1IGG SSXX X000 channels 0 through 7 are active. (A,B,C)
0110 1IGG SSXX X001 channels 8 through 15 are active. (A,B,C)
0110 1IGG SSXX X010 channels 16 through 23 are active. (A,B)
0110 1IGG SSXX X011 channels 24 through 31 are active. (A,B)
0110 1IGG SSXX X100 channels 32 through 39 are active. (A)
0110 1IGG SSXX X101 channels 40 through 47 are active. (A)
0110 1IGG SSXX X110 channels 48 through 55 are active. (A)
0110 1IGG SSXX X111 channels 56 through 63 are active. (A)

The following values will be used whenever programming the VMIVME-3122 to fill a buffer of 128 words with data from a block of 16 active channels. The user must specify which block of channels are active in the lower three bits of the register.

Block size of 16:

0111 0IGG SSXX X00X channels 0 through 15 are active. (A,B,C)
0111 0IGG SSXX X01X channels 16 through 31 are active. (A,B)
0111 0IGG SSXX X10X channels 32 through 47 are active. (A)
0111 0IGG SSXX X11X channels 48 through 63 are active. (A)

The following values will be used whenever programming the VMIVME-3122 to fill a buffer of 128 words with data from a block of 32 active channels. The user must specify which block of channels are active in the lower three bits of the register.

Block size of 32:

0111 1IGG SSXX X0XX channels 0 through 31 are active. (A,B)
0111 1IGG SSXX X1XX channels 32 through 63 are active. (A)

The following values will be used whenever programming the VMIVME-3122 to fill a buffer of 128 words with data from a block of 64 active channels. The user must specify which block of channels are active in the lower three bits of the register.

Block size of 64:

1000 0IGG SSXX XXXX channels 0 through 63 are active. (A)

Buffer Size 256 Words

The following values will be used whenever programming the VMIVME-3122 to fill a buffer of 256 words with data from a single channel. The user must specify the desired channel in the lower six bits of the register.

Block size of 1. 1000 1IGG SSCC CCCC

The following values will be used whenever programming the VMIVME-3122 to fill a buffer of 256 words with data from a block of 8 active channels. The user must specify which block of channels are active in the lower three bits of the register.

Block size of 8:

1001 0IGG SSXX X000	channels 0 through 7 are active.	(A,B,C)
1001 0IGG SSXX X001	channels 8 through 15 are active.	(A,B,C)
1001 0IGG SSXX X010	channels 16 through 23 are active.	(A,B)
1001 0IGG SSXX X011	channels 24 through 31 are active.	(A,B)
1001 0IGG SSXX X100	channels 32 through 39 are active.	(A)
1001 0IGG SSXX X101	channels 40 through 47 are active.	(A)
1001 0IGG SSXX X110	channels 48 through 55 are active.	(A)
1001 0IGG SSXX X111	channels 56 through 63 are active.	(A)

The following values will be used whenever programming the VMIVME-3122 to fill a buffer of 256 words with data from a block of 16 active channels. The user must specify which block of channels are active in the lower three bits of the register.

Block size of 16:

1001 1IGG SSXX X00X	channels 0 through 15 are active.	(A,B,C)
1001 1IGG SSXX X01X	channels 16 through 31 are active.	(A,B)
1001 1IGG SSXX X10X	channels 32 through 47 are active.	(A)
1001 1IGG SSXX X11X	channels 48 through 63 are active.	(A)

The following values will be used whenever programming the VMIVME-3122 to fill a buffer of 256 words with data from a block of 32 active channels. The user must specify which block of channels are active in the lower three bits of the register.

Block size of 32:

1010 0IGG SSXX X0XX	channels 0 through 31 are active.	(A,B)
1010 0IGG SSXX X1XX	channels 32 through 63 are active.	(A)

The following values will be used whenever programming the VMIVME-3122 to fill a buffer of 256 words with data from a block of 64 active channels. The user must specify which block of channels are active in the lower three bits of the register.

Block size of 64:

1010 1IGG SSXX XXXX	channels 0 through 63 are active.	(A)

Buffer Size 512 Words

The following values will be used whenever programming the VMIVME-3122 to fill a buffer of 512 words with data from a single channel. The user must specify the desired channel in the lower six bits of the register.

Block size of 1. 1011 0IGG SSCC CCCC

The following values will be used whenever programming the VMIVME-3122 to fill a buffer of 512 words with data from a block of 8 active channels. The user must specify which block of channels are active in the lower three bits of the register.

Block size of 8:

1011 1IGG SSXX X000	channels 0 through 7 are active.	(A,B,C)
1011 1IGG SSXX X001	channels 8 through 15 are active.	(A,B,C)
1011 1IGG SSXX X010	channels 16 through 23 are active.	(A,B)
1011 1IGG SSXX X011	channels 24 through 31 are active.	(A,B)
1011 1IGG SSXX X100	channels 32 through 39 are active.	(A)
1011 1IGG SSXX X101	channels 40 through 47 are active.	(A)
1011 1IGG SSXX X110	channels 48 through 55 are active.	(A)
1011 1IGG SSXX X111	channels 56 through 63 are active.	(A)

The following values will be used whenever programming the VMIVME-3122 to fill a buffer of 512 words with data from a block of 16 active channels. The user must specify which block of channels are active in the lower three bits of the register.

Block size of 16:

1100 0IGG SSXX X00X	channels 0 through 15 are active.	(A,B,C)
1100 0IGG SSXX X01X	channels 16 through 31 are active.	(A,B)
1100 0IGG SSXX X10X	channels 32 through 47 are active.	(A)
1100 0IGG SSXX X11X	channels 48 through 63 are active.	(A)

The following values will be used whenever programming the VMIVME-3122 to fill a buffer of 512 words with data from a block of 32 active channels. The user must specify which block of channels are active in the lower three bits of the register.

Block size of 32:

1100 1IGG SSXX X0XX	channels 0 through 31 are active.	(A,B)
1100 1IGG SSXX X1XX	channels 32 through 63 are active.	(A)

The following values will be used whenever programming the VMIVME-3122 to fill a buffer of 512 words with data from a block of 64 active channels. The user must specify which block of channels are active in the lower three bits of the register.

Block size of 64:

1101 0IGG SSXX XXXX channels 0 through 63 are active. (A)

Buffer Size 1024 Words

The following values will be used whenever programming the VMIVME-3122 to fill a buffer of 1024 words with data from a single channel. The user must specify the desired channel in the lower six bits of the register.

Block size of 1. 1101 1IGG SSCC CCCC

The following values will be used whenever programming the VMIVME-3122 to fill a buffer of 1024 words with data from a block of 8 active channels. The user must specify which block of channels are active in the lower three bits of the register.

Block size of 8:

1110 0IGG SSXX X000 channels 0 through 7 are active. (A,B,C)
1110 0IGG SSXX X001 channels 8 through 15 are active. (A,B,C)
1110 0IGG SSXX X010 channels 16 through 23 are active. (A,B)
1110 0IGG SSXX X011 channels 24 through 31 are active. (A,B)
1110 0IGG SSXX X100 channels 32 through 39 are active. (A)
1110 0IGG SSXX X101 channels 40 through 47 are active. (A)
1110 0IGG SSXX X110 channels 48 through 55 are active. (A)
1110 0IGG SSXX X111 channels 56 through 63 are active. (A)

The following values will be used whenever programming the VMIVME-3122 to fill a buffer of 1024 words with data from a block of 16 active channels. The user must specify which block of channels are active in the lower three bits of the register.

Block size of 16:

1110 1IGG SSXX X00X channels 0 through 15 are active. (A,B,C)
1110 1IGG SSXX X01X channels 16 through 31 are active. (A,B)
1110 1IGG SSXX X10X channels 32 through 47 are active. (A)
1110 1IGG SSXX X11X channels 48 through 63 are active. (A)

The following values will be used whenever programming the VMIVME-3122 to fill a buffer of 1024 words with data from a block of 32 active channels. The user must specify which block of channels are active in the lower three bits of the register.

Block size of 32:

1111 0IGG SSXX X0XX channels 0 through 31 are active. (A,B)
1111 0IGG SSXX X1XX channels 32 through 63 are active. (A)

The following values will be used whenever programming the VMIVME-3122 to fill a buffer of 1024 words with data from a block of 64-active channels. The user must specify which block of channels are active in the lower three bits of the register.

Block size of 64:

1111 1IGG SSXX XXXX channels 0 through 63 are active. (A)

4.3.4 Rate Control Register (RCR)

Table 4.3.4-1. Rate Control Register Bit Map

Rate Control Register (Offset $0006) Read/Write, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
0	Rate 14	Rate 13	Rate 12	Rate 11	Rate 10	Rate 09	Rate 08

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Rate 07	Rate 06	Rate 05	Rate 04	Rate 03	Rate 02	Rate 01	Rate 00

M3122/T4.3.4-1

Rate Control Register Definitions

Rate [14:0] - Sample Rate configuration bits. This field is used to program a variable sample rate as shown in the equation below. (Default is $0000.)

Sample Rate = 100 kHz (for $0000 <= rate [] <=$007A)
Sample Rate = (12.5 MHz ÷ (rate[] + 3)) (for $007A <= rate [] <= $7FFF)

An example for a sampling rate of 80 kHz would be:

Rate [] +3 = 12.5 MHz/sampling rate
Rate [] = (12.5E6/80E3) -3
Rate [] = 153.25 decimal = $0099 HEX

4.3.5 Interrupt Control Register (ICR)

Table 4.3.5-1. Interrupt Control Register Bit Map

Interrupt Control Register (Offset $0008) Read/Write, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
1	1	1	1	1	1	1	1

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
0	0	0	0	0	ILVL 2	ILVL1	ILVL0

M3122/T4.3.5-1

Interrupt Control Register Definitions

ILVL [2:0] - Interrupt Level Configuration bits. This field is used to select the VMEbus interrupt request level as shown in Table 4.3.5-2. This register is not affected by a software reset command (Default is logic 000).

Table 4.3.5-2. VMEbus Interrupt Request Levels

VMEbus Interrupt Level	ILVL 2	ILVL 1	ILVL
Interrupts are disabled	0	0	0
IRQ 1	0	0	1
IRQ 2	0	1	0
IRQ 3	0	1	1
IRQ 4	1	0	0
IRQ 5	1	0	1
IRQ 6	1	1	0
IRQ 7	1	1	1

M3122/T4.3.5-2

4.3.6 Interrupt Vector Register (IVR)

Table 4.3.6-1. Interrupt Vector Register Bit Map

Interrupt Vector Register (Offset $000A) Read/Write, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
1	1	1	1	1	1	1	1

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
IVECT 7	IVECT 6	IVECT 5	IVECT 4	IVECT 3	IVECT 2	IVECT 1	IVECT 0

M3122/T4.3.6-1

Interrupt Vector Register Bit Definitions

IVECT [7:0] - Interrupt Vector (Status/ID). (Default is $00). Contents of the Interrupt Vector register are supplied as a data byte (D07 through D00) on the data bus during the board's Interrupt Acknowledge Cycle. The function of the Interrupt Vector is determined by the system user. This register is not affected by a software reset command.

4.3.7 Software Reset Command (SRC)

The Software Reset Command allows the user to reset the board by writing arbitrary data to this location. The Software Reset Command will initiate an ADC calibration cycle and set the board in the initialized state described in Section 4.2.3.

Table 4.3.7-1. Software Reset Command Bit Map

Software Reset Command (Offset $000C) Read/Write, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
X	X	X	X	X	X	X	X

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
X	X	X	X	X	X	X	X

X = Don't Care M3122/T4.3.7-1

4.3.8 Software Trigger Command (STC)

This register works in conjunction with the CSR to allow software triggered modes of operation, such as Random Access. If both trigger mode bits are cleared in the CSR, a write to this command register causes the scan sequence to begin. The data written to this register is arbitrary (see Table 4.3.8-1).

Table 4.3.8-1. Software Trigger Command Bit Map

Software Trigger Command (Offset $000E) Read/Write, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
X	X	X	X	X	X	X	X

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
X	X	X	X	X	X	X	X

X = Don't Care M3122/T4.3.8-1

4.3.9 Gain RAM (Gain)

Table 4.3.9-1. Gain RAM Bit Map

Gain RAM (Offset $0010) Read/Write, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
1	1	1	1	1	1	1	1

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
0	0	0	0	0	0	0	GAIN

M3122/T4.3.9-1

Gain RAM Bit Definitions

GAIN - A logical 1 written to this bit location at address offset $0010 causes a gain of 10 to be used for channel indicated by Groupc [5:0] in CCR when Auto Gain mode is selected. A logical 0 written to this bit location at address offset $0010 causes a gain of 1 to be used for channel indicated by Groupc [5:0] in CCR when Auto Gain mode is selected. The procedures for loading the Gain RAM are listed below:

a. Select the channel desired in the CCR Groupc [5:0] bits i.e., CH0 = 00000, CH1 = 00001, CH2 = 00010.

b. Set the Bufc [4:0] bits to all zeros.

c. Write the desired gain to location $0010.

d. Repeat steps 1 to 3 for the remaining channels.

4.4 TIMER/COUNTER CONTROL GENERAL CHARACTERISTICS

Interval timing and data counting capabilities are provided by a triple 16-bit programmable timer/counter (Intel 8254) which is controlled by the Timer/Counter Registers at board addresses $0020 to $0026. Interval Timer Register TR0 is driven by an 6.25 MHz clock, and TR1 is driven by the output of TR0. The Data Counter Register (DCR) operates independently of the two timers, and is used to monitor the progress of data through the buffer. Operating modes and data transfers for all three counters are controlled by the Timer Control Register (TCR).

All timer/counter data transfers are 8 bits wide and use data bits D0 to D7. Two data transfers are required to read or write each 16-bit counter, with the least significant byte transferred first and the most significant byte transferred second. The control word determines the type of transfer, and must be written to the timer/counter before each data transfer. Table 4.4.6-1 lists the data transfer sequences for the timers and counter. Details concerning the Intel 8254 counter and programming requirements can be obtained from Intel. However, the information in this manual should be adequate.

4.4.1 Timer/Counter Registers

The Timer/Counter Registers control three 16-bit counters, two of which are available for adjusting the time between scans in the timed-burst operating mode, and one of which can provide an interrupt at a specific data word count. These registers are described in sections to come.

4.4.2 Interval Timer Register 0 (TR0)

Table 4.4.2-1. Interval Timer Register 0 Bit Map

Interval Timer Register 0 (Offset $0020) Read/Write, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
1	1	1	1	1	1	1	1

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
B07	B06	B05	B04	B03	B02	B01	B00

M3122/T4.4.2-1

4.4.3 Interval Timer Register 1 (TR1)

Table 4.4.3-1. Interval Timer Register 1 Bit Map

Interval Timer Register 1 (Offset $0022) Read/Write, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
1	1	1	1	1	1	1	1

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
B07	B06	B05	B04	B03	B02	B01	B00

M3122/T4.4.3-1

4.4.4 Data Counter Register (DCR)

Table 4.4.4-1. Data Counter Register Bit Map

Data Counter Register (Offset $0024) Read/Write, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
1	1	1	1	1	1	1	1

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
B07	B06	B05	B04	B03	B02	B01	B00

M3122/T4.4.4-1

Data Counter Register Bit Definitions

The Data Counter Register (DCR) can be programmed to provide a data word count directly, or to generate an interrupt when a specific number of A/D conversions have occurred.

Data Counter Control: The data counter can generate an interrupt after a predetermined number of data words have been stored in the buffer. The counter can be read directly to monitor the data count. To use the counter to generate an interrupt:

a. Load the data counter with the required data count (Table 4.4.6-1)
b. Set the source control bit D10 in the CCR (Table 4.5.2-1) to "one". (This disables the Midscan/Endscan interrupt.)
c. Enable the interrupt as described in Section 4.7.
d. Initiate the scanning operation.

Table 4.4.6-1 shows the sequence required for reading the data counter directly. The data counter can be accessed at any time, regardless of which operating mode is selected. Because the counter counts down, the value read is the remaining data count.

4.4.5 Timer Control Register (TCR)

Table 4.4.5-1. Timer Control Register Bit Map

Timer Control Register (Offset $0026) Write Only, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
1	1	1	1	1	1	1	1

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
B07	B06	B05	B04	B03	B02	B01	B00

M3122/T4.4.5-1

4.4.6 Scan Interval Timer

By operating in the "timed-burst mode", the data buffer can be scanned (filled) repetitively at specific intervals, or a single scan can be initiated after the first interval. See Figure 4.4.6-1 for a functional block diagram of the Interval Timer circuitry. The timed-burst mode is selected as follows:

a. Single Scan/Burst CCR D07 = 1
CCR D06 = 0

b. Interval Timer enabled CSR D13 = 1

When operating in this mode, a buffer scan will occur at the end of the time interval programmed into the timer.

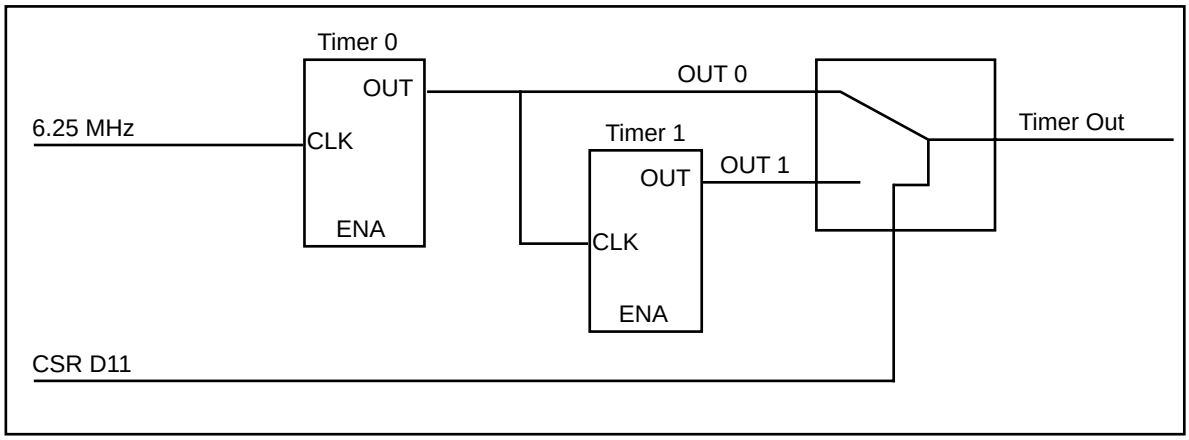


Figure 4.4.6-1. VMIVME-3122 Timer Functional Block Diagram

If CSR D11 is cleared, Timer 0's output is selected as the timer's output and the product of the timer's output will be:

Formula for 16-bit Timer: T0 = Desired Time/.000000160
Where: T0 = Timer 0's 16-bit value in decimal (1 to 65,535).
Timer = Period of time out in µs up to 10.4856 ms.

If CSR D11 is set, then Timer 1's output is selected as the timer's output and the output of Timer 0 is used as the clock for Timer 1. The period of the timer's output will be:

Formula for 2 Cascaded 16-bit Timers: Desired Time/.000000160 = T1 X T0

Where: Time = Period of Timer up to 687.1948 s.
T0 = Timer 0's 16-bit value in decimal (1 to 65,535).
T1 = Timer 1's 16-bit value in decimal (1 to 65,535).

Programmed Timer Intervals that take less than the time required to fill the buffer can cause unpredictable operation and should be avoided.

The time in microseconds, required to fill a buffer is reciprocal of the sampling rate times the buffer word size. For example, a 64-word buffer and 100 kHz sampling rate fills in 640 µs.

Table 4.4.6-1. Timer/Counter Data Transfer Sequences

Operation	Load Sequence	Register Address	Register Name	Transferred Data, D00-D07(Note 2)	XFR Mode
Load Timer 0	1	$26	Control Word	$34 (Select Timer)	Write
	2	$20	TMR 0 LS Byte	Least Significant Byte	Write
	3	$20	TMR 0 MS Byte	Most Significant Byte	Write
Load Timer 1 (Note 1)	1	$26	Control Word	$74 or $78 (Note 3)	Write
	2	$22	TMR 1 LS Byte	Least Significant Byte	Write
	3	$22	TMR 1 MS Byte	Most Significant Byte	Write
Load Data Counter	1	$26	Control Word	$B4	Write
	2	$24	CNTR LS Byte	Least Significant Byte	Write
	3	$24	CNTR MS Byte	Most Significant Byte	Write
Read Timer 0	1	$26	Control Word	$00 (Latch Timer Value)	Write
	2	$26	Control Word	$34 (Select Timer)	Write
	3	$20	TMR 0 LS Byte	Least Significant Byte	Read
	4	$20	TMR 0 MS Byte	Most Significant Byte	Read
Read Timer 1 (Note 1)	1	$26	Control Word	$40	Write
	2	$26	Control Word	$74 or $78 (Note 3)	Write
	3	$22	TMR 1 LS Byte	Least Significant Byte	Read
	4	$22	TMR 1 MS Byte	Most Significant Byte	Read
Read Data Counter	1	$26	Control Word	$80	Write
	2	$26	Control Word	$B4	Write
	3	$24	CNTR LS Byte	Least Significant Byte	Read
	4	$24	CNTR MS Byte	Most Significant Byte	Read

M3122/T4.4.6-1

NOTES:

1. CSR control bit D11 must be set to “one” to include Timer 1 in the interval timer (see text). The 32-bit timer is configured as:

	Timer 1 (Bits 31 to 16)		Timer 0 (Bits 15 to 00)		
MSB	MS Byte	LS Byte	MS Byte	LS Byte	LSB

2. Timer values $0001 0000, $0001 0001, and $0001 are invalid.

3. A Timer 1 control word of $0074 will produce repetitive data bursts at the programmed interval. A control word of $0078 will limit the acquisition to a single data burst at the end of the first interval. The single burst can be repeated by reloading the timer 1 load sequence.

4.4.7 Data RAM (BUFF)

Table 4.4.7-1. Data RAM Bit Map

Data RAM (Offset $0080 - $087E) Read/Write, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
B15	B14	B13	B12	B11	B10	B09	B08

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
B07	B06	B05	B04	B03	B02	B01	B00

M3122/T4.4.7-1

Data RAM Bit Definitions

B[15:0] - ADC data. B15 is MSB, B00 is LSB

4.4.8 Scratch Pad RAM (Scratch)

Table 4.4.8-1. Scratch Pad RAM Bit Map

Scratch Pad RAM (Offset $0880 - $7FFE) Read/Write, Byte,Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
D15	D14	D13	D12	D11	D10	D09	D08

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
D07	D06	D05	D04	D03	D02	D01	D00

M3122/T4.4.8-1

Scratch Pad Ram Definitions

D[15:0] - User-Defined

4.5 DATA ORGANIZATION AND CONTROL

4.5.1 Data Word

The contents of each word location in the data buffer is a data word, and represents the 16-bit digitized value of a single analog input channel.

4.5.2 Scaling and Coding

Table 4.5.2-1 shows the data word scaling and coding for channel gains of x1 and x10.

Data bit D15 is the most significant bit and D00 is the least significant bit. Coding is straight binary or offset binary if CSR bit D14 is cleared, and is two's complement if CSR bit D14 is set.

Table 4.5.2-1. ADC Data Format

ADC Data Coding (Gain = x1)			
	Unipolar Range	**Straight Binary**	
Input	**0 to +10 V**	**D15**	**D00**
Full Scale	+9.99985 V	1111 1111 1111 1111	
Half Full Scale	+5.00000 V	1000 0000 0000 0000	
Zero	+0.00000 V	0000 0000 0000 0000	
	Bipolar Range	**Offset Binary**	
Input	**±10 V**	**D15**	**D00**
+Full Scale	+9.99969 V	1111 1111 1111 1111	
+Half Full Scale	+5.00000 V	1100 0000 0000 0000	
Zero	0.00000 V	1000 0000 0000 0000	
-Half Full Scale	-5.00000 V	0100 0000 0000 0000	
-Full Scale	-10.00000 V	0000 0000 0000 0000	
	Bipolar Range	**Two's Complement**	
Input	**±10 V**	**D15**	**D00**
+Full Scale	+9.99969 V	0111 1111 1111 1111	
+Half Full Scale	+5.00000 V	0100 0000 0000 0000	
Zero	0.00000 V	0000 0000 0000 0000	
-Half Full Scale	-5.00000 V	1100 0000 0000 0000	
-Full Scale	-10.00000 V	1000 0000 0000 0000	

	LSB Bit Weight Versus Input Gain	
Input Range	**Gain = x1**	**x10**
0 to +5 V, ±2.5V	76.2939 µV	7.62939 µV
0 to +10 V, ±5 V	152.588 µV	15.2588 µV
±10 V	305.176 µV	30.5176 µV

M3122/T4.5.2-1

NOTE

THE BOARD MUST BE RECALIBRATED IF THE RANGE IS CHANGED FROM THE FACTORY CONFIGURATION OF ±10 V.

4.5.3 Data Block

A complete set of digitized values for all active input channels is a data block, and it can consist of 1, 8, 16, 32, or 64 channels. Block size is controlled by bits D05 - D00 in the CCR, as shown in Table 4.3.3-2.

Data words within a block are organized according to how the Group Configuration bits in the CCR are programmed. Table 4.3.3-2 lists the combinations of buffer and block size available.

4.5.4 Data Buffer/RAM

The data buffer contains from 1 to 64 data blocks, and is located at board address $0080. The size of the buffer is controlled by the Buffer Configuration Control bits D11 to D15 in the CCR. The buffer can be adjusted from 16 to 1,024 data words in six binary increments. A single update of all locations in the buffer is a data scan, and is executed at the user-defined sampling rate or the 100 kHz default rate.

Data blocks within the buffer are organized with the first block located at the lowest word address in the buffer, and with the data word in the last block located at the highest address. Total on-board RAM size is 2048 words. Memory locations $0880 through $0FFE may be used as scratch pad memory. Also, data buffer memory not used for storage of scanning input data may be used as on-board scratch pad memory.

4.5.5 Gain Selection

A fixed channel gain of x1 or x10 can be software programmable for all channels, or can be assigned individually for each channel. The automatic gain mode provides program control of the gain of each channel. For automatic gain control, a gain code for each channel is loaded into gain RAM. The gain is used as each channel is selected and digitized.

4.6 OPERATING MODES

The VMIVME-3122 Board can be programmed to scan the input channels continuously, to read input channels individually, or to acquire data in timed or synchronized bursts.

Table 4.3.3-3 summarizes the various operating modes, all of which are described in this section. The default settings assume a 64 channel option. If a 32- or 16-channel option is used, substitute 32 or 16 wherever 64 channels is mentioned.

4.6.1 Auto Scanning

This default operating mode is selected by a reset operation, or by clearing both CCR mode control bits. All active channels are scanned continuously in this mode, and any channel can be read at any time without affecting the scanning operation.

To set the board for Auto Scanning, either do a reset operation or write $5800 to the CCR (relative address $0004). The indicated CCR code also establishes the following conditions:

a. 64-word buffer
b. 64-channel block size
c. Interrupt on data ready flag if interrupt is enabled
d. Fixed gain x1

4.6.2 Single Scan

The Single Scan operating mode samples all the active channels one time and stops. The scan sequence will not start again until the selected trigger mode is initiated. The Single Scan mode can be triggered by a software command, external trigger, or by the interval timer. The steps to program single scan in each of these cases is described below.

Single Scan Software Triggered

Write $8000 to CSR (relative address $0002). This enables the software trigger. The indicated CSR code also establishes the following conditions:

a. LED turned off
b. Data stored in offset binary format
c. Interval timer configured as 16-bit counter
d. Data ready flag activated at end of data buffer

Write $5840 to CCR (relative address $0004). This sets the scan mode to single scan. the indicated CCR code also establishes the following conditions:

a. Buffer size of 64 words
b. Block size of 64 channels
c. Interrupt on data ready flag if interrupt is enabled
d. Fixed gain x1

The previous two steps set the board up for single scan software trigger. To initiate the scan process, write to relative board address $000E. The data written to this register is arbitrary.

Single Scan External Trigger

Write $9000 to CSR (relative address $0002). This enables the External Trigger. The indicated CSR code also establishes the following conditions:

a. LED turned off
b. Data stored in offset binary format
c. Interval Timer configured as 16-bit counter
d. Data ready flag activated at end of data buffer

Write $5840 to CCR (relative address $0004). This sets the scan mode to Single Scan. The indicated CCR code also establishes the following conditions:

a. Buffer size of 64 words
b. Block size of 64 channels
c. Interrupt on data ready flag if interrupt is enabled
d. Fixed gain x1

The board is now in the Single Scan External Trigger mode. The single scan of all active channels will start on the HIGH to LOW transition of the EXT STRT L input at the P2 connector. The EXT STRT L signal should stay LOW for 250 nsec to ensure proper operation.

Single Scan Interval Timer

Set-up timer register for TR0, write $A000 to CSR (relative address $0002). This enables the Interval Timer Trigger. The indicated CSR code also establishes the following conditions:

a. LED turned off
b. Data stored in offset binary format
c. Interval Timer configured as 16-bit counter
d. Data ready flag activated at end of data buffer

Write $5840 to CCR (relative address $0004). This sets the scan mode to Single Scan. The indicated CCR code also establishes the following conditions:

a. Buffer size of 64 words
b. Block size of 64 channels
c. Interrupt on data ready flag if interrupt is enabled
d. Fixed gain x1

A single scan of all active channels will occur each time the Interval Timer's time period expires.

4.6.3 Random Access

The Random Access operating mode samples one user-selected channel. The channel selection is done by programming CCR bits 5-0 with the binary representation of the channel number. The digitized channel data is stored at location $0080.

Random Access Software Trigger

Write $8000 to CSR (relative address $0002). This enables the software trigger. The indicated CSR code also establishes the following conditions:

a. LED turned off
b. Data stored in offset binary format
c. Interval timer configured as 16-bit counter
d. Data ready flag activated at end of the data buffer

Write $5880 to CCR (relative address $0004). This sets the scan mode to random access for channel 0. The indicated CSR code also establishes the following conditions:

a. Buffer size of 64 words
b. Block size of 64 channels
c. Interrupt on data ready flag if interrupt is enabled
d. Fixed gain x1

The above two steps set the board up for random access software trigger. To initiate the channel conversion process, write to relative board address $000E. The data written to this register is arbitrary.

Random Access External Trigger

Write $9000 to CSR (relative address $0002). This enables the External Trigger. The indicated CSR code also establishes the following conditions:

a. LED turned off
b. Data stored in offset binary format
c. Interval Timer configured as 16-bit counter
d. Data ready flag activated at end of data buffer

Write $5880 to CCR (relative address $0004). This sets the scan mode to Random Access. The indicated CCR code also establishes the following conditions:

a. Buffer size of 64 words
b. Block size of 64 channels
c. Interrupt on data ready flag if interrupt is enabled
d. Fixed gain x1

The board is now in the random access external trigger mode. The conversion of the selected channel will start on the high to low transition of the EXT STRT L input at the P2 connector. The EXT STRT L signal should stay LOW for 250 nsec to ensure proper operation.

Random Access Interval Timer

Write $A000 to CSR (relative address $0002). This enables the Interval Timer Trigger. The indicated CSR code also establishes the following conditions:

a. LED turned off
b. Data stored in offset binary format
c. Interval timer configured as 16-bit counter
d. Data ready flag activated at end of data buffer

Write $5880 to CCR (relative address $0004). This sets the scan mode to Random Access. The indicated CCR code also establishes the following conditions.

a. Buffer size of 64 words
b. Block size of 64 channels
c. Interrupt on data ready flag if interrupt is enabled
d. Fixed gain x1

The selected channel will be sampled and digitized each time the Internal Timer's time period expires.

4.6.4 Synchronizing Multiple VMIVME-3122 Boards

Multiple VMIVME-3122 Boards can be synchronized together by connecting the TRIG OUT L output from P2 of a synchronizing "master" to the EXT STRT L input of all slave boards.

As many as 16 boards in a single chassis can be synchronized in this manner, thereby providing up to 1,024 synchronized input channels and the simultaneous sampling of like numbered channels on all boards.

4.7 BUS INTERRUPTER

An interrupt can be generated when the data buffer is filled or half-filled, or after a specific number of A/D conversions have been completed (Section 4.6). The interrupt response is established through the Interrupt Control and Interrupt Vector registers which are shown in Sections 4.3.8 and 4.3.9. During VMEbus system reset operation, the Interrupt Control Register is cleared to “$FF00” and the Interrupt Vector Register is preset to “$FF00”.

4.8 TYPICAL PROGRAMMING EXAMPLES

The following examples of VMIVME-3122 programming illustrate typical applications for various operating modes.

4.8.1 Example 1

Auto Scan, fixed gain x1, buffer size = 64, Block size = 8, channels 16-23, Data Ready flag at end of buffer, 100 kHz sample rate, interrupts disabled, offset binary format.

Step 1. Reset board by writing arbitrary data to location $000C. This causes the board to go into Auto scan, 100 kHz sample rate, interrupt disabled, and Data Ready flag at end OD buffer.

Step 2. Write $4002 to CCR (location $0004). This puts the board in auto scan, Fixed gain x1, buffer size = 64, Block size = 8, and channels 16-23 available for sampling.

Step 3. Write $8000 to CSR (location $0002). This causes the data ready flag to be set at the end of the data buffer and offset binary format.

Step 4. Write $0000 to RCR (location $0006). This sets a 100 kHz sample rate.

Step 5. Write $FF00 to ICR (location $0008). This disables interrupts.

4.8.2 Example 2

Single scan, software trigger, auto gain, buffer size = 16, block size = 16, channels 00-15, data ready flag at end of buffer, 30 kHz sample rate, IRQ1 interrupt enabled, offset binary format.

Step 1. Write $0240 to CCR. This establishes Single Scan, Auto Gain, Buffer size, Block size, and Channel Group.

Step 2. Write $8000 to CSR. This establishes Software Trigger, Data Ready Flag at the end of the Buffer, and Offset Binary Format.

Step 3. Write $19E to RCR. This establishes a 30 kHz sample rate.

Step 4. Write $FF01 to ICR. This establishes interrupt IRQ1 enabled.

Step 5. Write vector to IVR at relative address $0010, enter gain for each channel. Gain of 1 is $FF00, gain of 10 is $FF01. Increment Group c [5:0] Channel Pointer for each channel.

Step 6. Write arbitrary Data to relative address $000E. This starts the Single Scan process.

NOTE:
YOU MUST HAVE INTERRUPT SERVICE ROUTINE SET-UP AT DESIRED VECTOR

4.8.3 Example 3

Example of Random Access, Interval Timer Trigger (timer set to 29.55 seconds), Unity Gain (x1), Channel 15, and Two's Complement Data.

Step 1. Write $0000 to SRC (location $000C)
Issue software reset command by writing arbitrary data.

Step 2. Poll CSR (location $0002) until D06 is set.
This detects when the previous command has finished executing.

Step 3. Write $5840 to CCR (location $0004)
Command board to single scan mode.

Step 4. Poll CSR (location $0002) until D06 is set.
This detects when the previous command has finished executing.

Step 5. Write $0034 to TCR (location $0026)
This selects timer 0 for initialization.

Step 6. Write $0024 to TR0 (location $0020)
This loads LSB of interval timer 0.

Step 7. Write $00F4 to TR0 (location $0020)
This loads MSB of interval timer 0.

Step 8. Write $0078 to TCR (location $0026)
This selects timer 1 for initialization.

Step 9. Write $008B to TR0 (location $0022)
This loads LSB of interval timer 1.

Step 10. Write $000B to TR0 (location $0022)
This loads MSB of interval timer 1.

Step 11. Read channel 0's converted data (location $0080)
This clears the CSR's Data Ready Bit at D06.

Step 12. Write $E800 to CSR (location $0002)
This establishes Interval Timer Trigger and a Two's Complement data format. This timer is started at this point.

Step 13. Write $588F to CCR (location $0004)
This establishes random access scan mode, channel 15, and unity gain.

Step 14. Read Channel 15's converted data (location $0080)
This reads Channel 15's converted data.

Channel 15 will be sampled approximately 29.55 seconds after the timers are set up in step 12. The data will be in Two's Complement format at location $0080.

NOTE: $0B8B x $F424 x 160 nanoseconds = 29.55 seconds

SECTION 5

CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES

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*****************
*     CAUTION   *
*****************
```

SOME OF THE COMPONENTS ASSEMBLED ON VMIC's PRODUCTS MAY BE SENSITIVE TO ELECTROSTATIC DISCHARGE AND DAMAGE MAY OCCUR ON BOARDS THAT ARE SUBJECTED TO A HIGH ENERGY ELECTROSTATIC FIELD. UNUSED BOARDS SHOULD BE STORED IN THE SAME PROTECTIVE BOXES IN WHICH THEY WERE SHIPPED. WHEN THE BOARD IS TO BE PLACED ON A BENCH FOR CONFIGURING, ETC., IT IS SUGGESTED THAT CONDUCTIVE MATERIAL BE INSERTED UNDER THE BOARD TO PROVIDE A CONDUCTIVE SHUNT.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice about the disposition of the damaged item(s).

5.2 PHYSICAL INSTALLATION

```
*****************
*     CAUTION   *
*****************
```

DO NOT INSTALL OR REMOVE BOARDS WHILE POWER IS APPLIED.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting card guides, slide the board smoothly forward against the mating connector until firmly seated.

5.3 BEFORE APPLYING POWER: CHECKLIST

Before applying power to the VMEbus chassis in which the board is installed, execute the following checklist to ensure that the board has been correctly prepared for operation.

a. Verify that the sections pertaining to programming and configuration, Section 4 and 5, have been reviewed and applied to system requirements. _____

b. Review Section 5.4 and Table 5.4-1 to verify that all jumpers are configured correctly for the application. _____

c. Verify that the I/O cables are properly terminated for the input/output connectors. Refer to Section 5.6 for connector descriptions. _____

d. Physical installation should have been completed as described in Section 5.2. _____

e. Ensure that all system cable connections are correct. _____

5.4 OPERATIONAL CONFIGURATION

VMEbus access modes and analog input configurations are controlled by field replaceable jumpers. This section describes the use of these jumpers, and their effects on board performance. Locations and functions of all VMIVME-3122 jumpers are shown in Figure 5.5-1 and Table 5.4-1. Typical jumper configurations are summarized in Table 5.4-2.

5.4.1 Factory-Installed Jumpers

Each VMIVME-3122 Board is configured at the factory with the specific jumper arrangement shown in Table 5.4-1. The factory configuration establishes the following functional baseline for the VMIVME-3122 board, and ensures that all essential jumpers are installed.

a. Board Identification is located at $0000 in the Short I/O Space, with either Supervisory or Nonprivileged access
b. ±10 V range
c. Differential inputs
d. LOW inputs for channels 31 and 63 are disconnected from COMM and AGND

Table 5.4-1. Programmable Jumper Functions

Jumper IDENT	Function (Installed)	Factory CONFIG
E13-1,2	Access Mode	Installed
E13-3,4	Access Mode	Installed
E11-1,2	Address Mode	Installed
E11-3,4	Address Mode	Installed
E5-1,2	Address Bit A31 = 0	Installed
E5-3,4	Address Bit A30 = 0	Installed
E5-5,6	Address Bit A29 = 0	Installed
E5-7,8	Address Bit A28 = 0	Installed
E5-9,10	Address Bit A27 = 0	Installed
E5-11,12	Address Bit A26 = 0	Installed
E5-13,14	Address Bit A25 = 0	Installed
E5-15,16	Address Bit A24 = 0	Installed
E8-1,2	Address Bit A23 = 0	Installed
E8-3,4	Address Bit A22 = 0	Installed
E8-5,6	Address Bit A21 = 0	Installed
E8-7,8	Address Bit A20 = 0	Installed
E8-9,10	Address Bit A19 = 0	Installed
E8-11,12	Address Bit A18 = 0	Installed
E8-13,14	Address Bit A17 = 0	Installed
E8-15,16	Address Bit A16 = 0	Installed
E6-1,2	Address Bit A15 = 0	Installed
E6-3,4	Address Bit A14 = 0	Installed
E6-5,6	Address Bit A13 = 0	Installed
E6-7,8	Address Bit A12 = 0	Installed
E1-1,2	CH 31 LOW Input Conn to AGND	Removed
E2-1,2	CH 63 LOW Input Conn to AGND	Removed
E7-1,2	Bipolar Analog inputs	Installed
E7-2,3	Unipolar Analog inputs	Removed
E10-1,2	±2.5 V Range Gain Multiplier	Removed
E9-1,2	±2.5 V Range Gain Multiplier	Removed
E12-2,3	±10 V Range	Installed
E12-1,2	±2.5 V, 0 to +5 V, 0 to +10 V Range	Removed
E3-3,2	PGA_H	Installed
E3-1,2	PGA_H Offset CAL	Removed
E4-3,2	PGA_L	Installed
E4-1,2	PGA_L Offset CAL	Removed

M3122/T5.4-1

Table 5.4-2. Typical Jumper Configurations

Example of Addressing Configuration
for: Standard Address Mode;
Supervisory Only;
Address $00D1 F000

Jumper	State	Position
E11-1,2	STD Address Mode	Removed
E11-3,4	STD Address Mode	Removed
E13-1,2	SPVSR	Removed
E13-3,4	SPVSR	Removed
E6-1,2	A15=1	Removed
E6-3,4	A14=1	Removed
E6-5,6	A13=1	Removed
E6-7,8	A12=1	Removed
E8-1,2	A23=1	Removed
E8-3,4	A22=1	Removed
E8-5,6	A21=0	Installed
E8-7,8	A20=1	Removed
E8-9,10	A19=0	Installed
E8-11,12	A18=0	Installed
E8-13,14	A17=0	Installed
E8-15,16	A16=1	Removed
E5-1,2	A31=0	Installed
E5-3,4	A30=0	Installed
E5-5,6	A29=0	Installed
E5-7,8	A28=0	Installed
E5-9,10	A27=0	Installed
E5-11,12	A26=0	Installed
E5-13,14	A25=0	Installed
E5-15,16	A24=0	Installed

M3122/T5.4-2

NOTE

TO BE CONSISTENT WITH CONVENTIONAL VMEbus DEVELOPMENT SYSTEM NOMENCLATURE, HEXADECIMAL NUMBERS IN THIS DOCUMENT ARE DESIGNATED WITH A "$" PREFIX UNLESS OTHERWISE INDICATED. DECIMAL NUMBERS ARE PRESENTED WITHOUT A PREFIX.

5.4.2 Access Modes

Supervisory (privileged) and user (nonprivileged) access is selected by jumper E13. Figure 5.4.2-1 shows the jumper location and access mode.

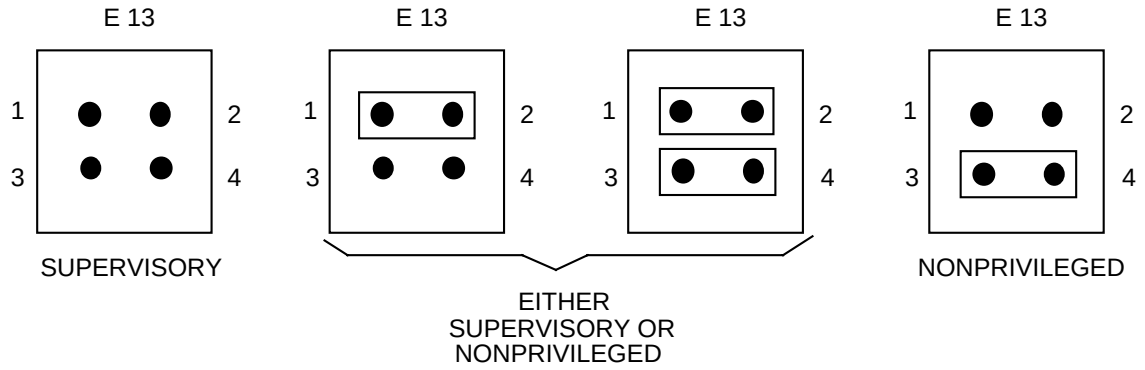


Figure 5.4.2-1. Supervisory and Nonprivileged Access Mode and Jumper Locations

5.4.3 Address Modes

Short I/O, Standard, and Extended Addressing is selected by jumper E11. Figure 5.4.3-1 shows the jumper location and address mode.

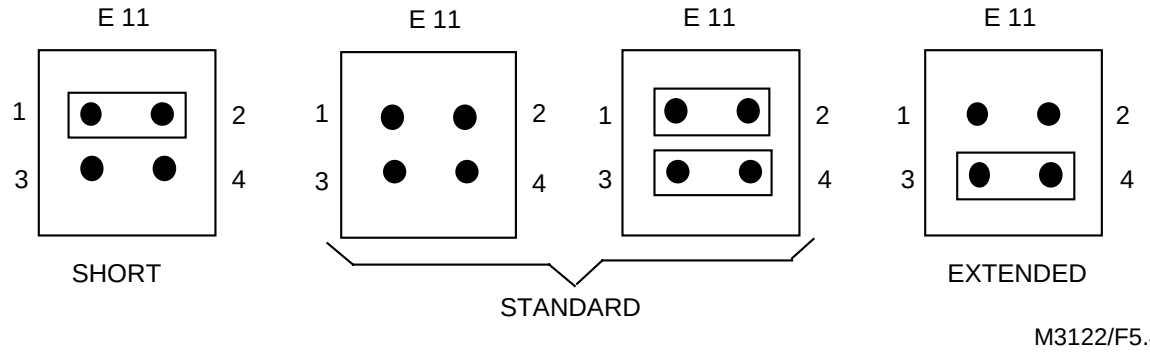
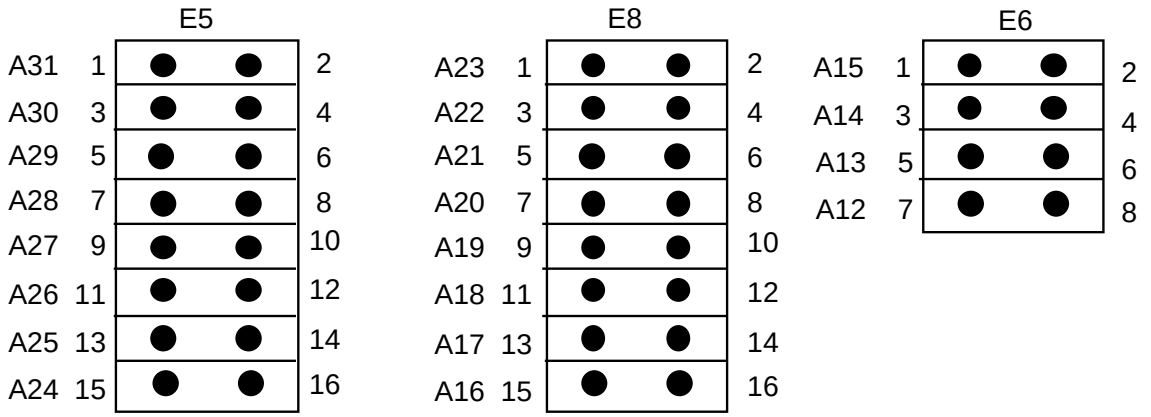


Figure 5.4.3-1. Short I/O, Standard, and Extended Addressing Modes and Jumper Locations

5.4.4 Board Address

The board address is configured by jumpers E5, E8, and E6. The board supports A32/A24/A16 addressing. The jumpers corresponding to the address bits are shown in Figure 5.4.4-1.



M3122/F5.4.4-1

Figure 5.4.4-1 Board Configuration Jumpers

The board address is programmed by installing shorting plugs at all “zero” or LOW address bit positions in jumper blocks E5, E6, and E8, and by omitting the shorting plugs at the “one” or HIGH positions. Address bit A12 is the least significant address bit that can be jumper-selected, and has a weight of 4,096 bytes.

5.4.5 Converter Voltage Range

The A/D Converter voltage range is controlled by jumpers E7, E9, E10, and E12 as shown in Table 5.4-2.

Table 5.4.5-1. A/D Converter Voltage Ranges

ADC Voltage Range *					
Jumper	**±10 V**	**±5 V**	**±2.5 V**	**0 TO +10 V**	**0 TO +5 V**
E12	2,3	1,2	1,2	1,2	1,2
E10	REM	REM	INS	REM	INS
E7	1,2	1,2	1,2	2,3	2,3
E9	REM	REM	INS	REM	INS

***** “INS” = Jumper installed, “REM” = Jumper removed.

M3122/T5.4.5-1

NOTE

THE BOARD MUST BE RECALIBRATED IF THE RANGE IS CHANGED FROM THE FACTORY CONFIGURATION OF ±10 V.

5.4.6 Input Voltage Range

The input voltage range (full scale voltage at the input of each channel) is determined by both the analog input gain and the A/D converter voltage range:

INPUT VOLTAGE RANGE = CONVERTER VOLTAGE RANGE ÷ INPUT GAIN

For example, an input gain of x10 combined with a converter voltage range of ±5 V produces an input voltage range of ±500 mV (±0.5 V).

NOTE

CARE MUST BE EXERCISED NOT TO APPLY INPUT VOLTAGES AND GAIN COMBINATIONS WHICH EXCEED THE CONVERTER VOLTAGE RANGE. FOR EXAMPLE, A GAIN OF 10 WITH AN INPUT VOLTAGE GREATER THAN 1.2 VOLTS EXCEEDS THE MAXIMUM CONVERTER VOLTAGE RANGE. IN THESE CASES, THE DATA RECEIVED WILL NOT BE VALID BUT MAY APPEAR AS VALID DATA.

5.4.7 Input Configurations

The analog inputs can be configured as single-ended, or differential channels, as shown in Table 5.4.7-1. The configurations are selected in groups of four consecutive channels by the positions of jumpers E1 and E2, and by the locations of SIP (single-in-line-package) resistor networks.

Each LOW side input has a 22 M resistor tied to AGND. The purpose of this resistor is to provide floating input protection. If the input lead is not connected, the board will see that channel at ground thru 22 M resistor.

5.4.8 Internal Ground Connections

All pins in the center “B” rows of both input connectors P3 and P4 are connected together to AGND, and provide a ground path and interchannel guards between differential input pairs when 96-wire 0.033-inch ribbon cables are used.

The LOW input for Channel 31 or 63 can be connected to AGND by installing E1-1,2 (Channel 31) or E2-1,2 (Channel 63). Installation of either of these jumpers configures the associated channel as a single-ended input. Each jumper must be removed for differential operation of the associated channel.

5.5 CALIBRATION

Before delivery from the factory, the VMIVME-3122 Board is fully calibrated and conforms to all specifications listed in Section 2. Should recalibration be required, refer to Sections 5.5.1 through 5.5.3, and perform the indicated procedures in the order shown. The locations of test points and adjustments are shown in Figure 5.5-1.

NOTE

THE BOARD MUST BE RECALIBRATED IF THE RANGE IS CHANGED FROM THE FACTORY CONFIGURATION OF ±10 V.

Table 5.4.7-1. Input Configuration Selection

P4 Channel Group	Input Configuration (Note 1)					
	Single-Ended			Differential		
	SIP POS	Jumpers		SIP POS	Jumpers	
	(Note 2)	E1	E2	(Note 2)	E1	E2
00 to 03	RP33	1,2	---	RP1	---	---
04 to 07	RP34	1,2	---	RP3	---	---
08 to 11	RP35	1,2	---	RP5	---	---
12 to 15	RP36	1,2	---	RP7	---	---
16 to 19	RP37	1,2	---	RP9	---	---
20 to 23	RP38	1,2	---	RP11	---	---
24 to 27	RP39	1,2	---	RP13	---	---
28 to 31	RP40	1,2	---	RP15	REM	---
Ch 31 is Single-Ended						

P3 Channel Group	Input Configuration (Note 1)					
	Single-Ended			Differential		
	SIP POS	Jumpers		SIP POS	Jumpers	
	(Note 2)	E1	E2	(Note 2)	E1	E2
32 to 35	RP41	---	1,2	RP17	---	---
36 to 39	RP42	---	1,2	RP19	---	---
40 to 43	RP43	---	1,2	RP21	---	---
44 to 47	RP44	---	1,2	RP23	---	---
48 to 51	RP45	---	1,2	RP25	---	---
2 to 55	RP46	---	1,2	RP27	---	---
56 to 59	RP47	---	1,2	RP29	---	---
60 to 63	RP48	---	1,2	RP31	---	REM
Ch 63 is Single-Ended						

M3122/T5.4.7-1

NOTES:

1. Jumper positions are indicated as:
   - 1,2 Shorting plug between pins 1 and 2.
   - 2,3 Shorting plug between pins 2 and 3.
   - REM Shorting plug removed.
   - --- "Don't care"; shorting plug can be installed or removed.
2. "SIP POS" = "Single-in-line-package position." The indicated position is one of two possible locations for the input SIP. Only one of the two locations is occupied. For example, the SIP for channel group 00 to 03 can be located as either RP33 or RP1.

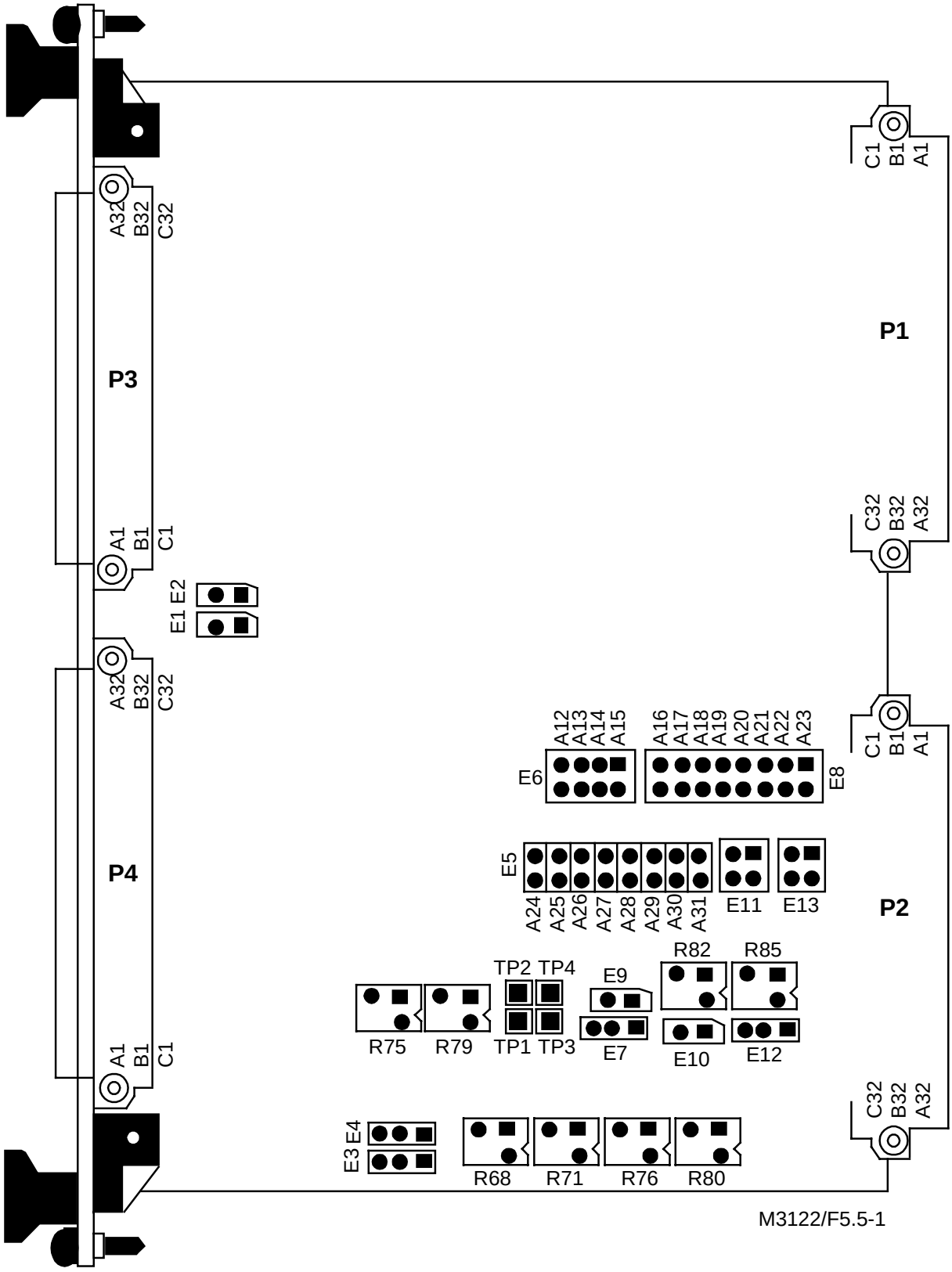


Figure 5.5-1. Locations of Test Points and Adjustments

5.5.1 Equipment Required

a. Digital Voltmeter (DVM)... 1.000 and 10.000 VDC ranges; 5 or more digits; ±0.003 percent of reading measurement accuracy; 10 M minimum input impedance.

b. Digital Voltage Source..... 10.000 VDC ±0.001 VDC voltage source; ±0.003 percent setting resolution and accuracy. 10 maximum source resistance.

c. Chassis..... VMEbus backplane or equivalent, with J1 connector, 68000 Series master controller, +5 ±0.1 VDC, 7 A (reserve current) power supply. One slot allocated for testing the VMIVME-3122 Board.

d. Extender Board ..... VMEbus extender board

e. Grounded input adapter .... 96-pin DIN connector (2 each) i.e., DIN 96CSC WTR4093 with row A connections shorted to row B connections shorted to row C connections. This connector(s) plugs into the VMIVME-3122 P3 and P4 connectors and grounds all VMIVME-3122 inputs for calibration purposes.

f. All channels adapter..... 96-pin DIN connector (2 each) i.e., DIN 96CSC WTR4093 with all row C connections shorted together and to row B and all row A connections shorted together This connector(s) plugs into the VMIVME-3122 P3 and P4 connectors allowing input voltage to be applied to all channels simultaneously.

g. Common mode adapter .. 96-pin DIN connector (2 each) i.e., DIN 96C$C WTR4093 with rows A and C shorted together. This connector(s) plug into the VMIVME-3122 P3 and P4 connectors allowing for common-mode calibration.

NOTE

DO NOT INSTALL OR REMOVE THIS BOARD WITH POWER APPLIED TO THE SYSTEM.

5.5.2 Calibration Procedure

a. Restore all program jumpers to the factory configuration, as shown in Table 5.4-1.
b. Locate the board at an address that is compatible with the VMEbus operating system.
c. Install the VMIVME-3122 Board on an extender board in the VMEbus chassis.
d. Place grounded input adapter in P3 and P4 connectors.
e. Apply power to the chassis backplane. Allow a minimum warm-up interval of ten minutes before proceeding.
f. Write the following data to the indicated board relative address:

Address	Data	Register	Mode
$000C	$C000	S.W. Reset	Reset
$0004	$5800	CCR	Gain x1, Auto Scan

ADC Reference ADJ:

g. Connect the digital voltmeter between TP3 (+) and TP1 (-).
h. Adjust potentiometer R82 for a reading of +10.0000 ± 0.00015 VDC.
i. Move jumper from E12-2,3 to E12-1,2.
j. Adjust potentiometer R85 for a reading of +5.00000 ± 0.00005 VDC.
k. Move jumper from E12-1,2 to E12-2,3.

Offset ADJ:

l. Connect positive lead of DVM to TP4, connect the negative to TP1.
m. Observe meter reading then write $5900 to address $0004.
n. Adjust R76 until meter reads the same value for both $5800 and $5900 written to address $0004.
o. With $5800 written to $0004 read and display board locations $0080 thru $00FE repetitively, at 3 to 5 readings/sec.
p. Adjust R75 until the majority of reading display $8000.
q. Remove grounded input adapter from P3 and P4 connectors.

CM ADJ:

r. Place common-mode adapter in P3 and P4 connectors.
s. Connect positive lead of voltage source to row A on adapter, connect negative lead to row B on adapter and set voltage source output to 0.0000 VDC.
t. With $5800 written to $0004 read and display board locations $0080 thru $00FE repetitively, at 3 to 5 readings/sec.

u. Note the majority of readings. They should be $8000. Set the voltage source to +10.0000 VDC. The majority of reading should still be $8000. If readings differ by more than 1 count, adjust R79 until display reads $8000. Set voltage source to -10.0000 VDC. Adjust R79 if necessary to have display read $8000. Toggle between +10.0000 VDC and -10.0000 VDC and verify display reads $8000.
v. Write $5900 to board address $0004 to set gain to 10.
w. With the voltage source set at 0.0000 VDC, note the majority of reading. Apply +10.0000 VDC and adjust R80 so reading do not differ from 0.0000 VDC reading by more than 3 counts. Do the same with -10.0000 VDC until both voltages produce no more than 3 counts deviation.
x. Repeat steps T through W until both values are correct.
y. Remove voltage source, and common mode calibration adapter.

GAIN ADJ

aa. Place All Channels adapter on P3 and P4. Connect positive lead of voltage source on “A” row and negative lead on “B” row. Rows “B” and “C” should be connected on adapter.
ab. With $5800 written to $0004 read and display board locations $0080 through $00FE repetitively, at 3 to 5 readings/sec.
ac. With the voltage set at -9.9997 VDC, adjust R68 until the majority of display values vary between $0000 and $0001. Due to noise, some channels may read greater than $0001 occasionally.
ad. With the voltage set at +9.9997 VDC, verify that the display values vary between $FFFE and $FFFF.
ae. Repeat steps AC and AD until both values are correct.
af. Write $5900 to board address $0004 to set gain of 10.
ag. With the voltage set at +0.99997 VDC, adjust R71 until the majority of display values vary between $FFFE and $FFFF. Due to noise, some channels may read greater than $0001 occasionally.
ah. With the voltage set at -0.99997 VDC, verify that the display values vary between $0000 and $0001.

5.5.3 Functional Verification

This procedure tests the Programmable Gain Amplifier (PGA), and verifies the integrity of all input channels. Steps *a* through *e* are identical to steps *a* through *e* in Section 5.5.2, and can be omitted if the calibration procedure has been performed within the previous hour, and if power has not been removed from the board.

a. Restore all program jumpers to the factory configuration, as shown in Table 5.4-1.
b. Locate the board at an address that is compatible with the VMEbus operating system.
c. Install the VMIVME-3122 board on an extender board in the VMEbus chassis.
d. Apply power to the chassis backplane. Allow a minimum warm-up interval of ten minutes before proceeding.

e. Connect the digital voltage source to the channel 00 input pins P4-A1 (+) and P4-C1 (-). Using a connector that shorts the “B” row to the “C” row, adjust voltage source output to 0.0000 VDC.
f. Write the following data to the indicated board address:

Address	Data	Register	Mode
$000C	$C000	S.W. RESET	Reset
$0004	$5900	CCR	GX10, Auto Scan

g. Read and display board word location $0080 (input channel 00) repetitively, at 3 to 5 readings /sec.
h. Adjust the voltage source output to +992.19 mVDC, and verify that the displayed value is between $FED0 and $FF30.
i. Write $5800 to address $0004 to set gain = 1.
j. Adjust the voltage source output to +9.9219 VDC, and verify that the displayed value is between $FEFB and $FF05.
k. Refer to the P3 and P4 connector descriptions in Tables 5.5.3-2 and 5.5.3-3 to determine the input pairs used in the remainder of this procedure.
l. Move the digital voltage source test leads to the channel 01 input pins. Connect the positive test lead to the A row pin, and the negative test lead to the C row pin.
m. Change the address of the displayed data to $0082 (input channel 01). Verify that the displayed value is between $FEFA and $FF06.
n. Repeat steps *n* and *o* for the remaining channels 02 through 63. Increase the displayed address by $0002 for each successive channel, to a maximum address of $00FE for channel 63.
o. Functional verification is completed. Remove power from the board. Remove all test connections. Restore the board to the factory configuration, as shown in Table 5.4-1.

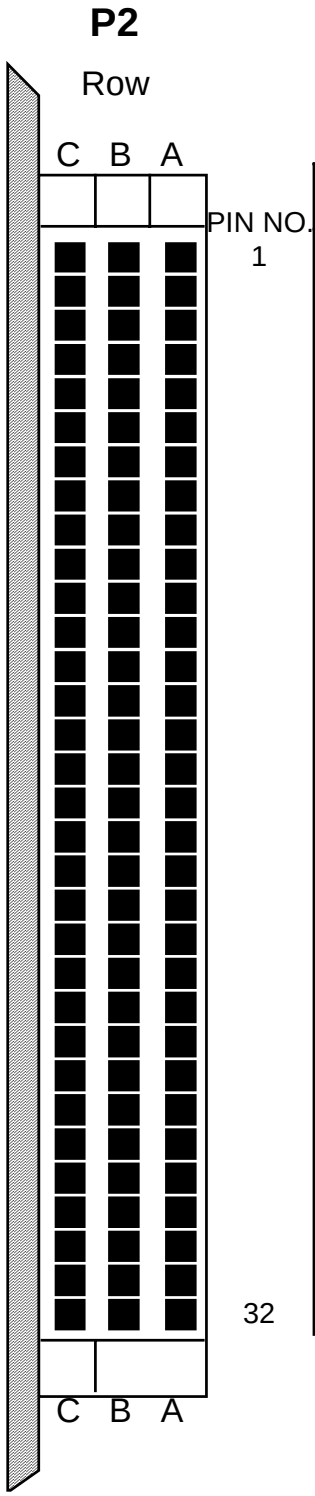
5.6 CONNECTOR DESCRIPTIONS

5.6.1 Connector Functions

Electrical connections to the VMIVME-3122 Board are made through four 96-pin DIN connectors P1 through P4, all of which have the pin configuration shown in Figure 5.6.1-1. P1 connects the VMIVME-3122 Board to the VMEbus backplane, and contains the address, data, and control lines, and all additional signals necessary to control VMEbus functions related to the board.

P2 provides the user pins necessary for external synchronization of the board as well as upper address/data lines. User pin assignments are listed in Table 5.5.3-1.

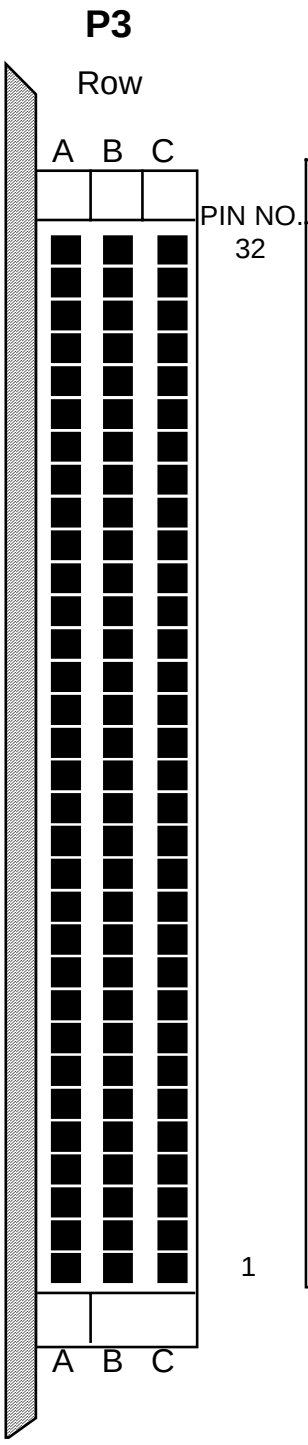
Table 5.5.3-1. P2 Connector Pinout



Pin	Row C	Row B	Row A
01	N/C	+5 V	N/C
02	•	DGND	•
03	•	N/C	•
04	•	A24	•
05	•	A25	•
06	•	A26	•
07	•	A27	•
08	•	A28	•
09	•	A29	•
10	•	A30	•
11	•	A31	•
12	•	DGND	•
13	•	+5 V	•
14			•
15	•		N/C
16	•		•
17	•		•
18	•		•
19	•		•
20	•		•
21	•		•
22	•	DGND	•
23	•		•
24	N/C		•
25	•		•
26	•		N/C
27	•		EXT STRT L
28	•		EXT STRT RTN
29	•		TRIG OUT L
30	•		EN EXT STRT H
31	•	DGND	N/C
32		+5 V	DGND

M3122/T5.5.3-1

Table 5.5.3-2. P3 Connector Pinout

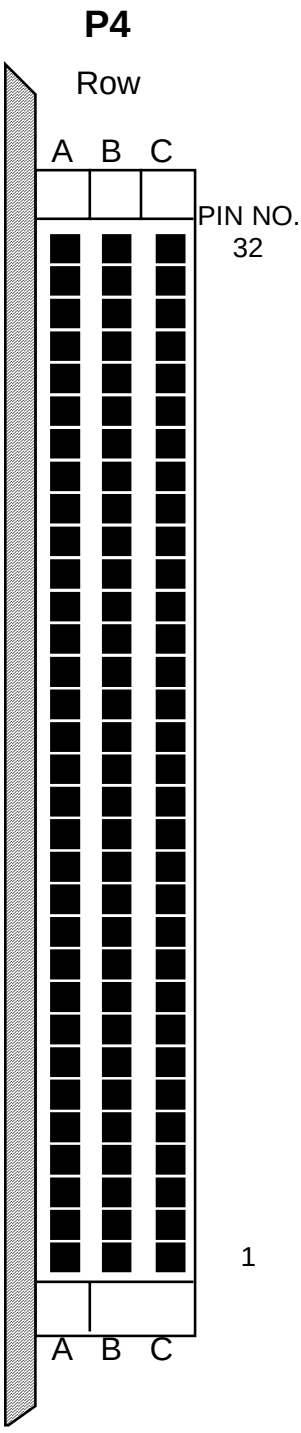


Pin	Row A	Row B	Row C
32	CH 63 HIGH		CH 63 LOW*
31	CH 62 HIGH		CH 62 LOW
30	CH 61 HIGH	AGND	CH 61 LOW
29	CH 60 HIGH		CH 60 LOW
28	CH 59 HIGH	•	CH 59 LOW
27	CH 58 HIGH		CH 58 LOW
26	CH 57 HIGH		CH 57 LOW
25	CH 56 HIGH	•	CH 56 LOW
24	CH 55 HIGH		CH 55 LOW
23	CH 54 HIGH	•	CH 54 LOW
22	CH 53 HIGH		CH 53 LOW
21	CH 52 HIGH		CH 52 LOW
20	CH 51 HIGH		CH 51 LOW
19	CH 50 HIGH	•	CH 50 LOW
18	CH 49 HIGH		CH 49 LOW
17	CH 48 HIGH		CH 48 LOW
16	CH 47 HIGH	AGND	CH 47 LOW
15	CH 46 HIGH		CH 46 LOW
14	CH 45 HIGH		CH 45 LOW
13	CH 44 HIGH	•	CH 44 LOW
12	CH 43 HIGH		CH 43 LOW
11	CH 42 HIGH	•	CH 42 LOW
10	CH 41 HIGH		CH 41 LOW
9	CH 40 HIGH		CH 40 LOW
8	CH 39 HIGH	•	CH 39 LOW
7	CH 38 HIGH		CH 38 LOW
6	CH 37 HIGH		CH 37 LOW
5	CH 36 HIGH	•	CH 36 LOW
4	CH 35 HIGH		CH 35 LOW
3	CH 34 HIGH		CH 34 LOW
2	CH 33 HIGH	AGND	CH 33 LOW
1	CH 32 HIGH		CH 32 LOW

*Channel 31 and 63 LOW inputs can be jumpered individually to AGND.

M3122/T5.5.3-2

Table 5.5.3-3. P4 Connector Pinout



Pin	Row A	Row B	Row C
32	CH 31 HIGH		CH 31 LOW*
31	CH 30 HIGH		CH 30 LOW
30	CH 29 HIGH	AGND	CH 29 LOW
29	CH 28 HIGH		CH 28 LOW
28	CH 27 HIGH	•	CH 27 LOW
27	CH 26 HIGH		CH 26 LOW
26	CH 25 HIGH		CH 25 LOW
25	CH 24 HIGH	•	CH 24 LOW
24	CH 23 HIGH		CH 23 LOW
23	CH 22 HIGH		CH 22 LOW
22	CH 21 HIGH	•	CH 21 LOW
21	CH 20 HIGH		CH 20 LOW
20	CH 19 HIGH		CH 19 LOW
19	CH 18 HIGH	•	CH 18 LOW
18	CH 17 HIGH		CH 17 LOW
17	CH 16 HIGH		CH 16 LOW
16	CH 15 HIGH	AGND	CH 15 LOW
15	CH 14 HIGH		CH 14 LOW
14	CH 13 HIGH	•	CH 13 LOW
13	CH 12 HIGH		CH 12 LOW
12	CH 11 HIGH		CH 11 LOW
11	CH 10 HIGH	•	CH 10 LOW
10	CH 09 HIGH		CH 09 LOW
9	CH 08 HIGH		CH 08 LOW
8	CH 07 HIGH	•	CH 07 LOW
7	CH 06 HIGH		CH 06 LOW
6	CH 05 HIGH		CH 05 LOW
5	CH 04 HIGH	•	CH 04 LOW
4	CH 03 HIGH		CH 03 LOW
3	CH 02 HIGH		CH 02 LOW
2	CH 01 HIGH	AGND	CH 01 LOW
1	CH 00 HIGH		CH 00 LOW

*Channel 31 and 63 LOW inputs can be jumpered individually to AGND.

M3122/T5.5.3-3

5.6.2 Input Modes

Analog inputs are connected to the board through front panel connectors P3 and P4. P4 contains the input pins for Channels 00 to 31, and P3 contains the input pins for Channels 32 to 63. Pin assignments for P3 and P4 are summarized in Tables 5.5.3-2 and 5.5.3-3. The center "B" rows in P3 and P4 are connected together to AGND bus, which can be used as a guard bus for 96-wire cables. Refer to Section 5.4.7 and Table 5.4.7-1 for the selection of **single-ended** or **differential** input configurations.

5.6.3 Input Cables

If 96-wire 0.033-inch ribbon cables or discrete wire type cables are used for the analog inputs, the center row can provide a ground reference to the analog return (AGND) on the board by installing Jumper J3. If 64-wire 0.050-inch ribbon cables are used, "VARI TWIST" or equivalent twisted pair cables are recommended to minimize crosstalk and induced noise. Access to AGND is available in 64-wire cables at pin C32 of P3 and P4 by installing E1-1,2 for P4, or E2-1, 2 for P3.

5.6.4 External Synchronization

External TTL-level synchronization triggers are connected to the EXT STRT L input at the P2 connector (refer to Section 5.4.7). The EN EXT STRT H output is a flag to the triggering device that the VMIVME-3122 is ready to accept an external trigger. To synchronize multiple VMIVME-3122 Boards together, connect the TRIG OUT H output from the designated "master" board to the EXT STRT L input of all boards to be synchronized to the master.

5.7 SYSTEM CONSIDERATIONS

5.7.1 Applications with Signal Conditioning Boards

The VMIVME-3122 Board serves as a multiplexer/digitizer for signal conditioning boards such as the VMIVME-3413 32-Channel Low-Level Input Board. The output connectors on the signal conditioning boards are configured to cable directly to either P3 or P4 on the VMIVME-3122.

When used with signal conditioning boards, the VMIVME-3122 is configured with differential inputs. These applications use either the 500 Hz input filter option, or no filters at all.

5.7.2 Operation with Direct Analog Inputs

When used without signal conditioning input boards, the VMIVME-3122 Board provides direct full scale input ranges from ±250 mV to ±10 V.

The optimum input filter for these applications is the 50 Hz filter, although the 10 Hz filter will provide improved attenuation of power line frequency interference at the expense of decreased common-mode rejection. To minimize the effects of direct

input multiplexing, the inputs on the VMIVME-3122 are buffered using op-amps. The buffers supply a constant low impedance to the Programmable Gain Amplifier (PGA) regardless of the varying source impedance. Use the lowest input gain and the largest block size (see Section 4.4.3) that are practical for the application.

If inputs are obtained directly from remote sources, the grounding scheme used can have a major effect on system performance. Each system has its own unique interference considerations, but the following general guidelines will apply in most cases.

a. Long Input Lines: Long input lines (greater than 10 feet), or inputs from grounded sources (sources which are not floating), should be connected to differential inputs, and overall shields should be extended from the input sources to as close to the board as possible. Single-ended inputs are susceptible to ground loop errors, and should be used only with high-level floating sources.

b. Source Impedance: Use signal sources with the lowest available source impedances. Susceptibility to crosstalk and induced interference increases as the source impedance increases.

c. Floating Signal Sources: The shield from a floating signal source (RTD, strain gage, etc.) should be connected to the LOW (negative) terminal at the source. For low impedance sources (less than 10), or for sources which are protected from interference fields, connect the board end of the shield to analog return (AGND) at the board. For high impedance sources, connect all shield terminals of the sources together, and leave the board ends of the shields open.

d. Grounded Signal Sources: Outputs of grounded sources (sources which are not floating) must be referenced to a common ground which ensures that the input voltage will not exceed the input range (±10 V) of the board. Shields from grounded sources should be connected to the LOW terminal of the sources, and left open at the board.

e. Unused Inputs: Unused inputs within each group of eight channels (0 through 7, 8 through 15, etc.) should be connected to a common ground to avoid interference with active channels. Grounding of unused 8-channel groups is not essential, but will assist in minimizing susceptibility to system noise.

SECTION 6

MAINTENANCE

6.1 MAINTENANCE

This section provides information relative to the care and maintenance of VMIC's products. If the products malfunction, verify the following:

a. Software
b. System configuration
c. Electrical connections
d. Jumper or configuration options
e. Boards fully inserted into their proper connector location
f. Connector pins are clean and free from contamination
g. No components of adjacent boards are disturbed when inserting or removing the board from the VMEbus card cage
h. Quality of cables and I/O connections

User level repairs are not recommended. Contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return.**

6.2 MAINTENANCE PRINTS

User-level repairs are not recommended. The appendix to this manual contains drawings and diagrams for reference purposes only.

ACKNOWLEDGEMENTS

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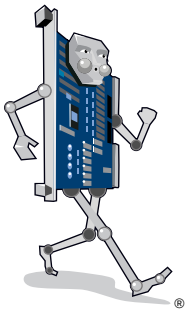

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