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Compensation for TID Damage in SOI Pixel Devices

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We are investigating adaption of SOI pixel devices for future high energy physic(HEP) experiments. The pixel sensors are required to be operational in very severe radiation environment. Most challenging issue in the adoption is the TID (total ionizing dose) damage where holes trapped in oxide layers affect the operation of nearby transistors. We have introduced a second SOI layer - SOI2 beneath the BOX (Buried OXide) layer - in order to compensate for the TID effect by applying a negative voltage to this electrode to cancel the effect caused by accumulated positive holes. In this paper, the TID effects caused by ⁶⁰Co γ -ray irradiation are presented based on the transistor characteristics measurements. The irradiation was carried out in various biasing conditions to investigate hole accumulation dependence on the potential configurations. We also compare the data with samples irradiated with X-ray. Since we observed a fair agreement between the two irradiation datasets, the TID effects have been investigated in a wide dose range from 100 Gy to 2 MGy.

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1 Introduction

The Silicon-On-Insulator (SOI) pixel detectors are being developed for various applications [3]. Applications in high-energy physics experiments require a couple of issues to be cleared. In the SOI devices the total-ionization-dose (TID) effect is substantial in severe radiation environments, where the trapped holes in the insulator affect the operation of the transistors located close by. The annual doses at the inner-most layer in typical HEP experiments are; 158 kGy/y at LHC-ATLAS [1], 1.6 MGy/y at HL-LHC, and 1 kGy/y at ILC-ILD [2].

We are studying TID compensation by using double SOI, where the potential of the middle silicon layer we have introduced additionally is controlled to cancel the effect, e.g., applying negative voltage to the SOI2 (V_{SOI2}) cancels the effects caused by accumulated positive holes [5][6]. The hole accumulation, however, should be dependent on the configuration of the terminal biases applied during irradiation. The purpose of this study is to investigate the compensation dependence on such bias configurations. A general study concerning the influence of biasing during irradiation can be found in Tab .2.

2 Samples

The TID compensation was evaluated by irradiating TrTEG (Transistor Element Group) samples up to 2 MGy with ^{60}Co γ 's. Various types of transistors were fabricated in TrTEG chips for this study.

TrTEG6 has 18 types transistors (L/W values, two gate oxide thicknesses core/IO, body connection schema) for each of NMOS and PMOS, as summarized in Tab. 1. In this note we concentrate on their L/W dependence. TrTEG7 has seven types for each of NMOS and PMOS which were irradiated under various biasing conditions.

Fig.1 illustrates drawings of the TrTEG6 and TrTEG7 chips. The chips were mounted on ceramic chip carriers and wire-bonded for biasing. They were irradiated with ^{60}Co at JAEA (Takasaki) [4]. The total dose ranged from 3 kGy up to 2 MGy for TrTEG6 samples but with all electrode grounded. The TrTEG7 samples were irradiated to 100 kGy but with various biasing conditions, see Tab. 2. In total seven types of biasing conditions were examined. This paper covers four types.

The dose rate was from 0.2 kGy/h up to 10 kGy/h. All samples were kept at room temperature during the irradiation. The samples were brought to University of Tsukuba in four hours in room temperature, then kept at -20 in the refrigerator except during measurement.

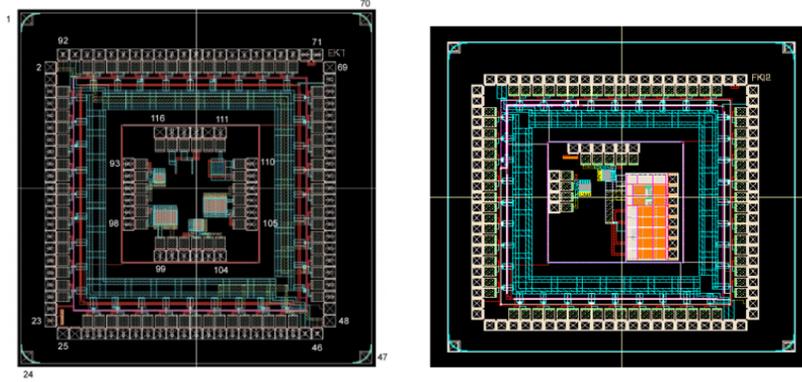


Figure 1: (left) TrTEG6 and (right) TrTEG7. TrTEG6 has 18 types of transistors for each NMOS and PMOS. TrTEG7 samples were irradiated in seven biasing conditions.

Table 1: TrTEG6 transistors parameters

Tr	L [μm]	W [μm]	Gate type	V _{th}	Body-Connection
0	0.2	5	Core	Normal	Floating
1	0.5	5	Core	Normal	Floating
2	1.0	5	Core	Normal	Floating
3	0.2	5	Core	Low	Floating
4	0.5	5	Core	Low	Floating
5	1.0	5	Core	Low	Floating
6	0.35	5	IO	high	Floating
7	0.35	5	IO	Low	Floating
8	0.2	5	Core	Low	Source-Tie
9	0.5	5	Core	Low	Source-Tie
10	1.0	5	Core	Low	Source-Tie
11	0.4	10	Core	Normal	Source-Tie2
12	0.6	6	Core	Normal	Source-Tie2
13	1.0	10	Core	Normal	Source-Tie2
14	0.2	5	Core	Normal	Body-Tie
15	0.5	5	Core	Normal	Body-Tie
16	1.0	5	Core	Normal	Body-Tie
17	1.0	5	IO	Normal	Source-Tie

Table 2: Biasing conditions during TrTEG7 irradiation

	V_s [V]	V_d [V]	V_g [V]	V_{SOI2} [V]
Sample1	0	0	0	0
Sample2	0	0	0	-5
Sample3	0(1.8)	1.8(0)	0(1.8)	-5
Sample4	0(1.8)	1.8(0)	1.8(0)	-5

3 $I_d - V_g$ Curve

We measured $I_d - V_g$ curve to evaluate characteristics of the transistors. The obtained $I_d - V_g$ curves are shown in Fig.2 as a function of dose for typical NMOS and PMOS transistors. The $I_d - V_g$ curve was measured at $V_d = 1.8$ V, $V_s = 0$ V for NMOS, and $V_d = 0$ V, $V_s = 1.8$ V for PMOS with V_{BPW} grounded, V_{BACK} floating, and $V_g = V_s$ for body-tie type transistors. As shown the figure, the $I_d - V_g$ curve shifts negatively as accumulating the dose. Pre-irradiation curve as shown in black as a reference.

Fig. 3 shows the curves of samples irradiated to 200 kGy but with changing the SOI2 voltage(V_{SOI2}) from 0 V to -15 V. By adjusting V_{SOI2} to -10 V the irradiated I-V curve is nearly compensated back to the pre-irradiation curve.

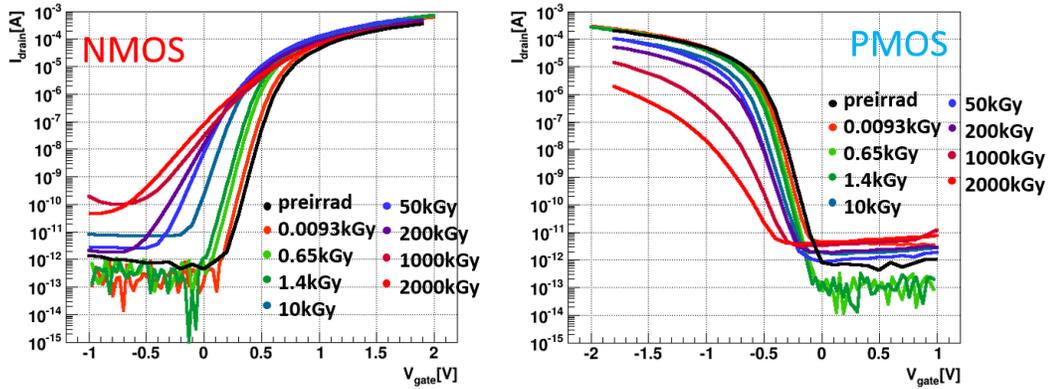


Figure 2: $I_d - V_g$ curves for (left) NMOS and (right) PMOS transistors with $L = 1.0 \mu\text{m}$, $W = 5.0 \mu\text{m}$, Core, Low V_{th} , Source-Tie). They were irradiated with $V_{SOI2} = 0$. Both NMOS and PMOS I-V curves shift negatively as accumulating the dose gradually from pre-irradiation curve (black) to 2 MGy curve (red).

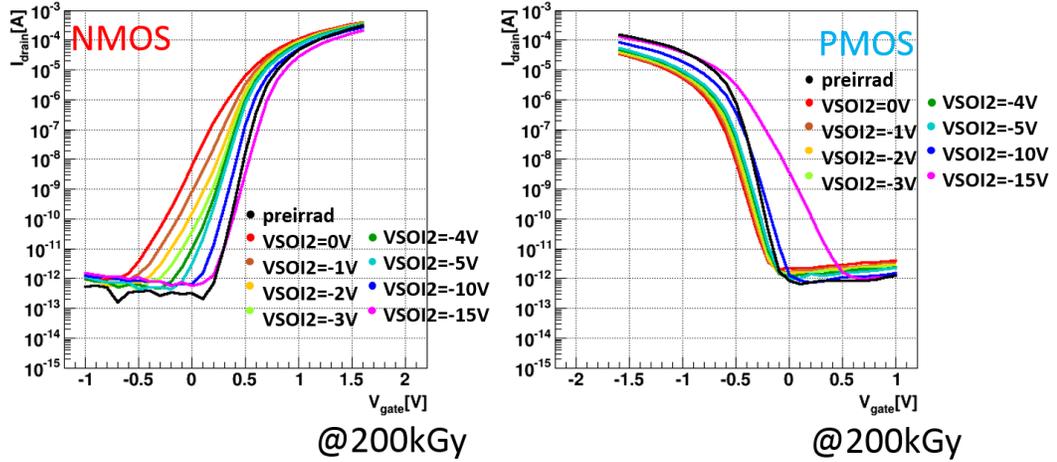


Figure 3: I_d - V_g curves for (left) NMOS and (right) PMOS measured with changing V_{SOI2} voltage from 0 V to -15 V. The samples were irradiated to 200 kGy. The I-V curves shifted by irradiation (0 V, red) are compensated back to the pre-irradiation curves (black) by adjusting V_{SOI2} voltage (for example at -10 V, blue).

4 Threshold V_{th} and trans-conductance g_m

We define two values to evaluate transistor characteristics quantitatively, threshold voltage (V_{th}) and trans-conductance (g_m). The V_{th} is defined as V_g at $I_d = 100$ [nA] W/L (W : gate width, L : gate length). The evolution with the dose of the threshold voltage of a typical transistor is plotted in Fig. 4. The curves are shown for various V_{SOI2} settings applied during measurement (they were grounded during irradiation for these samples). The dotted line indicates the pre-irradiation threshold voltage. By adjusting V_{SOI2} , the threshold voltage can be set back to the pre-irradiation value.

The trans-conductance g_m is defined as $g_m = (\partial I_d / \partial V_g)$. The relative change (dg_m/g_m) as defined in Equation (1) are shown in Fig.5 for some V_{SOI2} voltages. In general NMOS can find an appropriate V_{SOI2} below 500 kGy, while PMOS requires relatively large V_{SOI2} for compensation.

In a recent study [7], we have verified that the large g_m degradation in PMOS can be minimized substantially by adjusting the dose profile in gate fabrication. Further studies are in progress.

$$\frac{dg_m}{g_m} = \frac{g_m(V_{SOI2}, \text{dose}) - g_m(V_{SOI2}, \text{preirrad})}{g_m(V_{SOI2}, \text{preirrad})} \times 100 \quad (1)$$

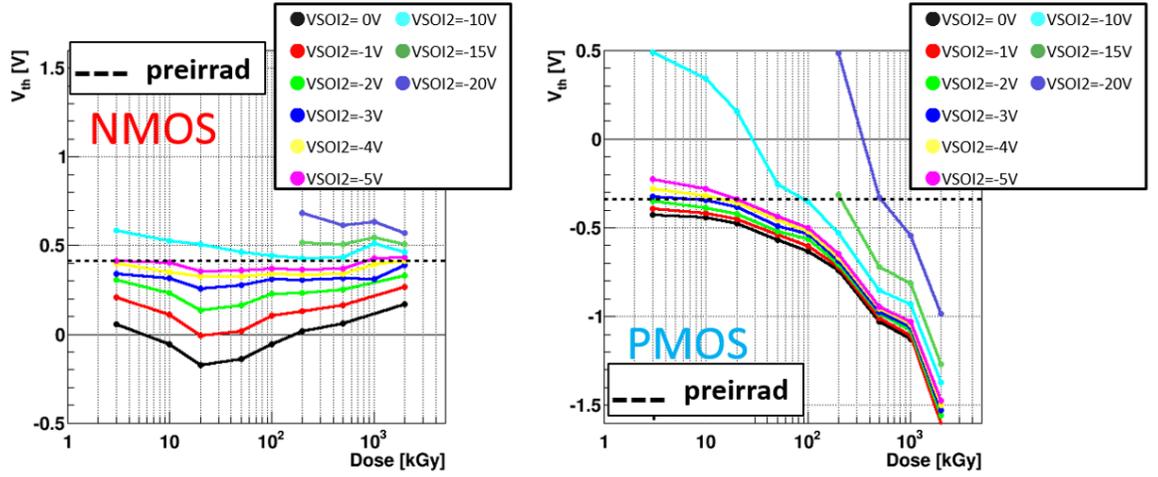


Figure 4: The threshold voltage (V_{th}) shifts are shown for (left) NMOS and (right) PMOS. Without applying V_{SOI2} , they shift negatively and substantially as $V_{SOI2} = 0$ V curve (black) shows. By applying V_{SOI2} , the threshold voltage can be set back to the pre-irradiation value (dotted lined).

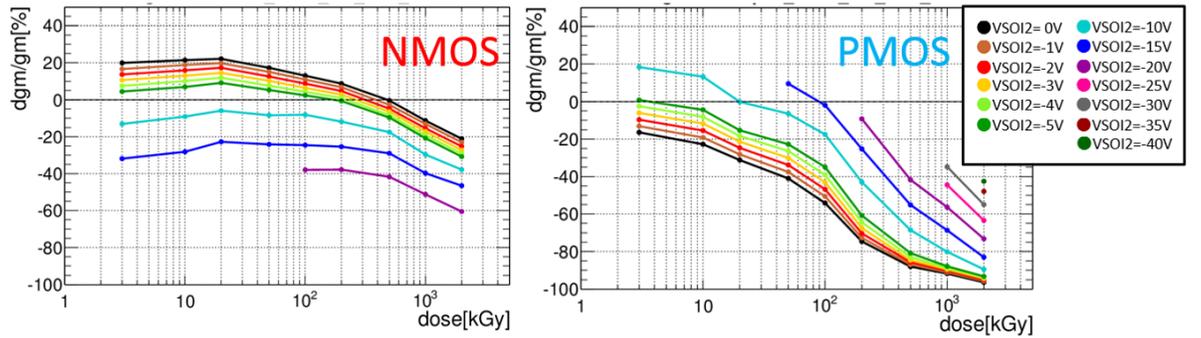


Figure 5: The relative shift (dg_m/g_m) with dose for some V_{SOI2} voltages for (left) NMOS and (right) PMOS. For NMOS, optimum V_{SOI2} can be found for g_m compensation below 500 kGy, while PMOS degradation is substantially and large V_{SOI2} voltage is required. The compensation at large dose (100 kGy or higher) seems become difficult.

5 L-dependence of V_{th} shift

We have evaluated the TID effect dependence on the transistor length L to investigate possible edge effect enhancement in shorter devices. We define ΔV_{th} as $\Delta V_{th} = (V_{th-dose} - V_{th-preirrad}) / V_{th-preirrad}$ for transistors with various L . As shown in Fig. 6, shorter the L , larger the threshold voltage shift caused by TID for both NMOS and PMOS. The L dependence, however, diminishes by applying V_{SOI2} for compensation - the difference among three L values 0.2, 0.5, 1.0 μm is small when compensated.

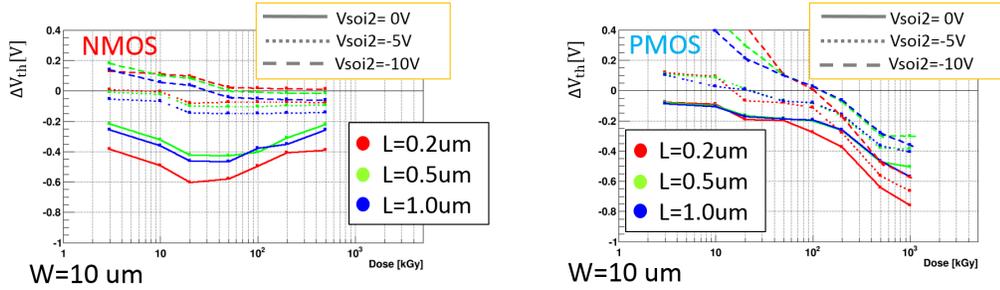


Figure 6: The threshold shift-dependence on the transistor gate length L for (left) NMOS and (right) PMOS. Shorter length ($L = 0.2 \mu\text{m}$, solid red) transistors are more sensitive to TID effect. However, by applying V_{SOI2} for compensation (dotted lines with color), the difference of V_{th} shift among three L values becomes small.

6 V_{th} shift per biasing condition during irradiation

The threshold voltage shifts measured with changing V_{SOI2} (post-irradiation) are shown in Figs. 7 and 8. The data are compared between different biasing conditions during irradiation. The plots are shown only for typical transistors, but all other transistors showed similar tendency. In Fig. 7, the samples were irradiated with all terminals grounded except that V_{SOI2} was either 0 V (green) or -5 V (blue) during irradiation. Fig. 8 is for the case the transistors were either in transistor-Off (green) or in transistor-On (blue) with V_{SOI2} was -5 V during irradiation.

Applying V_{SOI2} during irradiation reduces the threshold shift because hole traps in the oxide are less in the gate side attracted by negative V_{SOI2} . The threshold shifts are smaller if the transistor is on state during irradiation. The effect is more significant for PMOS transistors.

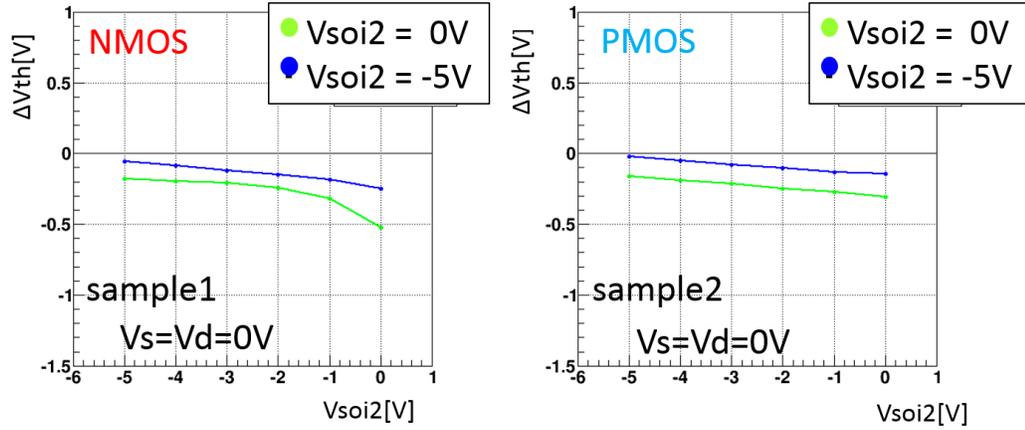


Figure 7: The threshold voltage shifts measured with changing V_{SOI2} for transistors ($L=0.6\ \mu\text{m}$, $W=60\ \mu\text{m}$, Core, NV_{th} , ST2) of (left) NMOS and (right) PMOS. All terminals grounded except V_{SOI2} during irradiation. The shifts for the samples with V_{SOI2} -5 V (blue) during irradiation are reduced compared to the grounded sample (green).

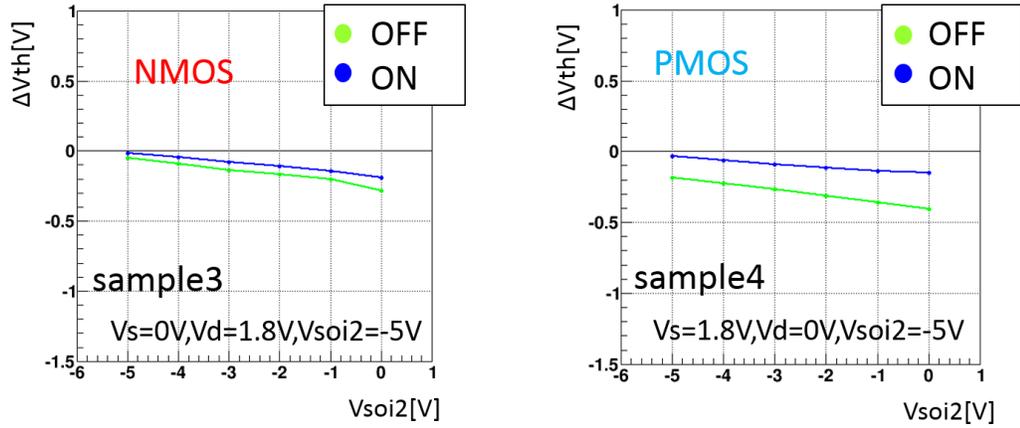


Figure 8: The threshold voltage shifts measured with changing V_{SOI2} . The transistor parameters are identical to Fig. 7. The transistors were either on or off during irradiation with applying V_{SOI2} of -5 V. The on-state (blue) transistors show smaller threshold voltage shift than the off-state (green) transistors.

7 Comparison with X-ray irradiation

While the above samples were irradiated with ^{60}Co covering a high dose range, more systematic irradiation has been performed with X-ray covering a dose as low as 100 Gy and up to 100 kGy. The transistor parameters are summarized in Tab. 3. The irradiation was made on RadTEG samples [8] fabricated on single SOI wafers. There are 8,000 transistors on a wafer. The X-ray irradiation was carried out on a wafer basis, see Fig. 9, with scanning the position uniformly (see Fig. 10).

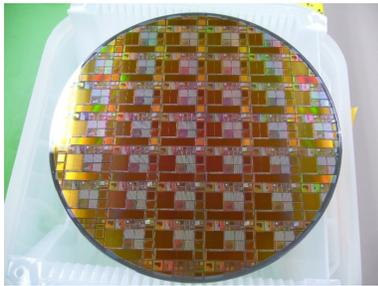


Figure 9: Photo of a wafer of Radiation Test Element Group(RadTEG) [8].

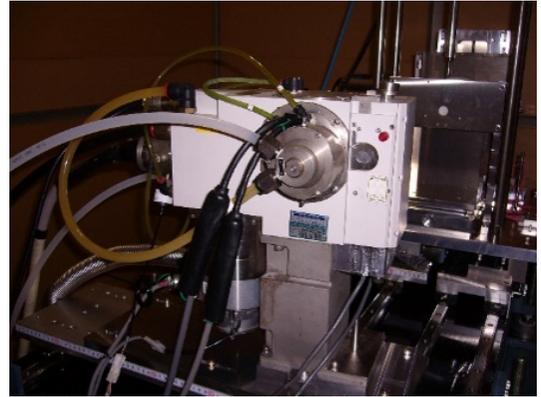


Figure 10: X-ray irradiation using a Mo target with the tube current 100 mA and oltage 40 kV.[8]

Table 3: RadTEG transistor parameters[8]

Gate type	Body-Connection	Max.L/W	Min.L/W	V_{th}	# of Tr
Core	Floating	0.2/0.5	10/10	Low	24
Core	Floating	0.2/0.5	10/10	Normal	24
Core	Source-Tie	0.2/0.2	5/5	Low	18
Core	Source-Tie	0.2/0.63	5/5	Normal	18
Core	Source-Tie2	0.4/1.0	5/5	Low	18
Core	Source-Tie2	0.4/1.0	5/5	Normal	18
Core	Floating(enclosed)	0.35/3.04	5/10	Low	12
Core	Floating(enclosed)	0.35/3.04	5/10	Normal	12
Core	Body-Tie	0.2/0.63	5/5	Normal	12
Core	Body-Tie	0.2/0.63	5/5	Normal	12
IO	Floating	0.35/0.5	10/10	High	24
IO	Floating	0.35/0.5	10/10	Normal	24
IO	Source-Tie	0.2/0.63	10/10	Normal	24
IO	Source-Tie2	0.4/1.0	5/10	Normal	24
IO	Floating(enclosed)	0.35/3.04	10/10	Normal	24
IO	Body-Tie	0.2/0.63	5/5	Normal	12

We compare the V_{th} shifts caused by two types of irradiation sources, see Fig. 11. The transistors having identical parameters are chosen from the TrTEG6 and RadTEG samples. The results from the ^{60}Co irradiation are in fairly good agreement with the

X-ray irradiation results in the overlapping dose region. Since RadTEG covers a lower dose range (down to 93Gy, not shown in this plot), the combined results provide us comprehensive understanding of the TID effects in wider dose range. Note that the BOX thicknesses are 200 nm for single SOI and about 160 nm for double SOI wafers, hence we expect some difference. In addition, the trapped hole fraction is larger with ^{60}Co irradiation than with X-ray [9], which may explain a general tendency that the threshold shifts are slightly larger in ^{60}Co irradiated samples.

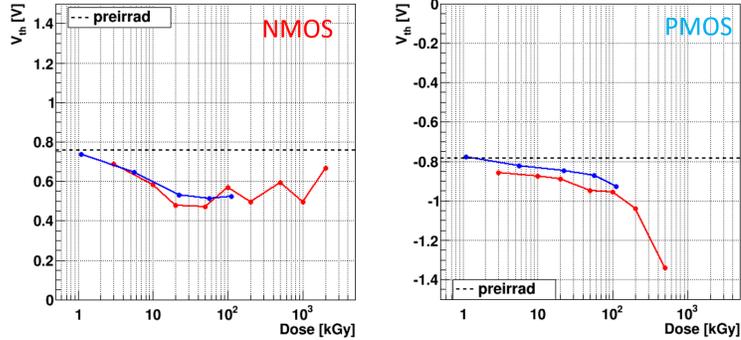


Figure 11: V_{th} shifts of (left) NMOS and (right) PMOS transistors in comparison of γ -ray (red) and X-ray (blue) irradiations.

8 Summary

We have investigated the TID effects in double SOI devices, evaluating changes in $I_d - V_g$ characteristics using TrTEGs. By applying negative voltage to $V_{\text{SOI}2}$, the transistor characteristics are compensated back to the pre-irradiation characteristics, in the dose range typically below 500 kGy. Detailed studies concerning the biasing conditions during irradiation have been presented. Such a dose range is below expected at the ILC pixel detector. The ^{60}Co results are in fairly good agreement with X-ray irradiation, the both datasets covering the dose range from 100 Gy to 2 MGy.

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