A high bandwidth feedback demonstrator system has been developed for proof of concept transverse intra-bunch closed loop feedback control studies at the CERN SPS. This system contains a beam pickup, analog front end receiver, signal processor, back end driver, power amplifiers and kicker structure. The main signal processing functions are performed digitally, using very fast (4GSa/s) data converters to bring the system signals into and out of the digital domain. The digital signal processing function is flexibly implemented in an FPGA allowing for maximum speed and reconfigurability for testing different control algorithms. The signal processor is a modular design consisting of commercial and custom components. This approach allowed for a rapidly-developed prototype to be developed in a short time with limited resources. Initial beam studies at the SPS using the system prior to the CERN long shutdown one (LS1) have been very encouraging. We are planning several key upgrades to the system, including the signal processor.

Introduction and Background

Introduction and Motivation:
- High Intensity LHC beam is known to cause transverse instabilities driven by the electron cloud effect and Transverse Mode Coupled Instabilities (TMC3) in the SPS. This adversely affects operation of the SPS, especially for the planned high luminosity upgrade where beam intensities increase.
- A research and development effort has been undertaken between CERN and SLAC under the auspices of the US LHC Accelerator Research Program (LARP) to develop techniques for mitigating the instabilities using a wide-bandwidth transverse closed-loop feedback system.
- Goal: Achieve feedback control of intra-bunch instabilities.
- This work involves simulation and modeling of the beam and bunch dynamics along with the controller, research and development of high sampling rate digital signal processing electronics (along with low-noise analog front and back ends) and feedback control techniques and development of a wide bandwidth kicker structure (to apply correction fields to the beam).

Work to Date:
- A rapidly developed single-bunch demonstrator system was conceived and developed in 2012. This system was used in Machine Development (MD) studies at the SPS prior to Long Shutdown 1 (LS1).
- The simulation and modeling effort is progressing with work towards developing more detailed models including non-linear effects and system identification formulations and optimal controller topologies.
- The pro.LiS MD measurements were performed using the existing low bandwidth kicker (200MHz), allowing control of only lower-order modes (0, 1).
- The results demonstrated control of mode 0 instabilities for a single bunch.

System Overview

The Feedback Processor

RF Power Amplifiers

Beam Kicker

Demo Processor Support HW - PLL Chassis

Technology Development Roadmap

Upgrade Development Progress For The CERN SPS High Bandwidth Transverse Feedback Demonstration Processor

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Abstract

With this initial success, we are planning to upgrade the system with additional functions and for higher performance. For the immediate future, we are focusing on four areas:
1) Feedback Demo Processor Upgrades
2) RF Power Amplifier Upgrades
3) Beam Kicker Structure Upgrades
4) Demo Processor Support Hardware Upgrades

Long-Term/Ongoing Work:
- Higher sampling rate processing (4GSa/s)
- MBSO Control Techniques (use of multiple beam pickups)
- Multiple Bunch Processing
- Different Digital Filter Structures (IR, FIR)