**Introduction**

The primary function of the ALS timing system is to synchronize and sequence all systems required to deliver beam from the gun through the injection system to the storage ring. In addition, the timing system synchronizes diagnostics to the beam and provides controls for optimizing injection efficiency and selecting the operating mode.

A survey of similar, more modern accelerator timing systems revealed that the most common commercial solution for event-based timing systems was based on Micro Research Finland (MRF) hardware. In particular, NSLS-II had developed EPICS drivers for the MRF hardware in their timing system. MRF hardware was chosen as the platform for the new ALS timing system to accelerate development by leveraging demonstrated commercial hardware with EPICS drivers.

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**Embedded Event Receiver**

An MRF-compatible embedded event receiver was developed by NSLS-II and included in their accelerator instrumentation platform. This platform serves as the Digital Front End (DFE) board in the NSLS-II BPM chassis, which was adapted for use in the new ALS BPMs.

The NSLS-II embedded EVR was modified so that the phase relationship between the EVG event clock and the EVR recovered clock is fixed, permitting synchronous RF-based clock recovery. In the ALS BPM, the recovered clock is used to regenerate the orbit clock that is the reference for the BPM ADC sampling clock. This modified embedded EVR has since been ported to the new ALS Bunch Current Monitor (BCM) system, where it is also used to derive an RF-synchronous reference for the sampling clock.

The embedded EVR was designed to use a Xilinx Virtex-6 series high speed transceiver. However, it is possible to port the design to another Xilinx device family or different FPGA vendor by replacing only the hardware-specific portion of the EVM code. This EVR only requires an FPGA with a high speed serial transceiver supporting transfer rates of 20s the event clock rate (2.5Gb/s for ALS) connected to an SFP port and a local reference clock close enough in frequency to the event clock rate that it can be used as a reference for the transceiver clock recovery PLL.

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**Conclusion**

The ALS timing system upgrade combines mature and widely used commercial hardware with custom hardware for ALS-specific functions and interfaces. This allowed a reduction in the scope of the project while providing a flexible, expandable and event-based timing master.

Leveraging the NSLS-II embedded EVR firmware and MRF/IOC EPICS support greatly accelerated development.

Building the RF-clock recovery into the embedded EVR reduced the number of ERF EVRs and physical connections needed, significantly reducing equipment installation, cost, and maintenance in the long-term.

The embedded EVR can be included in any new instrumentation firmware requiring machine timing.

A flexible and configurable event sequence scheme provides support for existing and future modes of ALS operation. Timestamps are accurate and precisely synchronized across all timing system clients, providing a level of multi-system diagnostic data correlation previously unachievable at ALS.