2005 International Linear Collider Physics and Detector Workshop
and Second ILC Accelerator Workshop
Snowmass, Colorado, August 14-27, 2005

The Vertex Tracker WG Report

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UC Berkeley and LBNL

Convenors:

Marco Battaglia, Massimo Caccia, Yasuhiro Sugimoto

Sub Group Organisers:

SG1 VTX Conceptual Design: **Marc Winter, Su Dong**

SG2 VTX Engineering Design: **Chris Damerell, Leo Greiner**

SG3 VTX Sensor Technology: **Massimo Caccia, Gerhard Lutz**

Snowmass, August 26, 2005

Vertex Tracker Conceptual Design

Definition of physics needs

Physics Benchmarks

Benchmarking **Vertexing**

$e^+e^- \to Z^0H^0$, BR($H^0 \to c\bar{c}$), BR($H^0 \to \tau^+\tau^-$) at $\sqrt{s}$=0.35 TeV

$e^+e^- \to Z^0H^0H^0$, $H^0 \to b\bar{b}$ at $\sqrt{s} = 0.5$ TeV

$e^+e^- \to A^0H^0 \to b\bar{b}b\bar{b}$, at $\sqrt{s} = 1.0$ TeV + ...

Benchmarking **Single Track Impact Parameter**

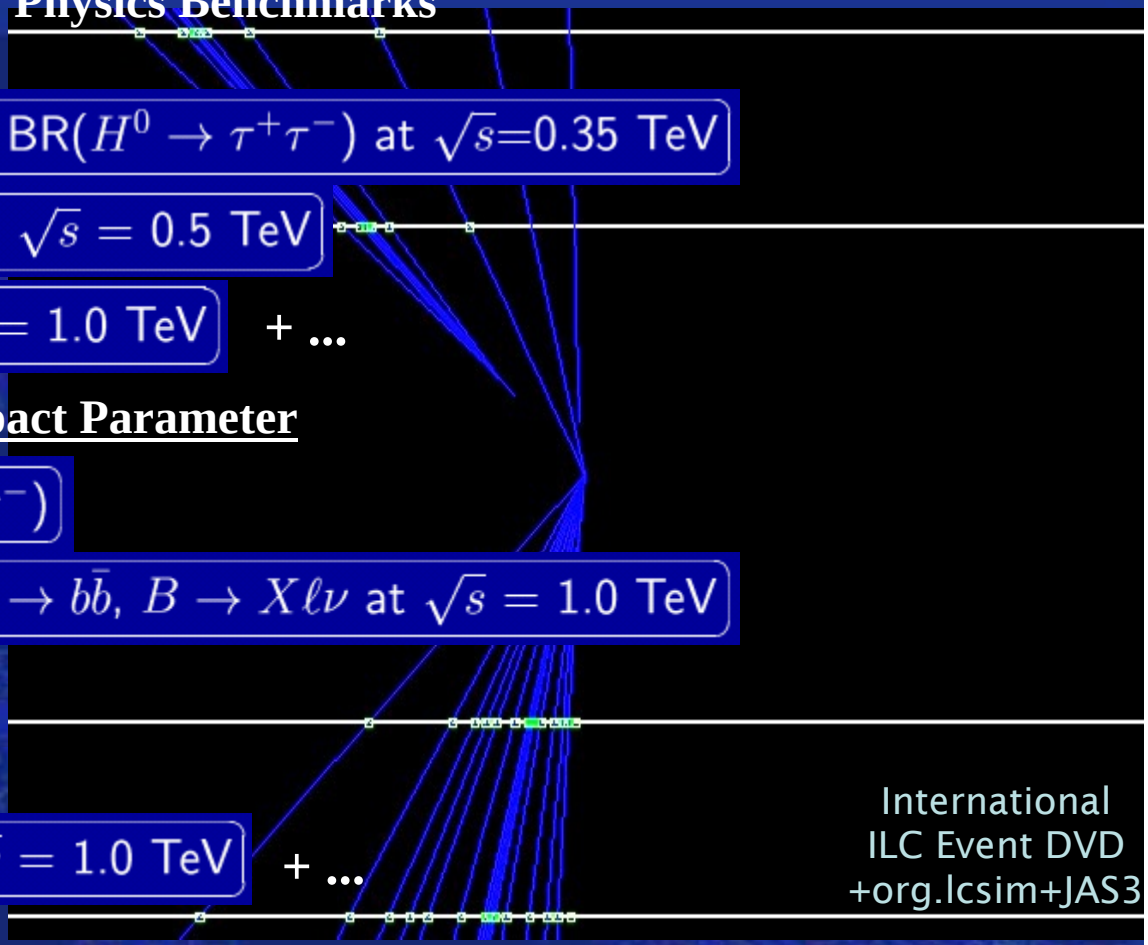
$e^+e^- \to Z^0H^0$, BR($H^0 \to \tau^+\tau^-$)

$e^+e^- \to \chi_2^0\chi_3^0$, $\chi_3^0 \to \chi_1^0Z^0$, $Z^0 \to b\bar{b}$, $B \to X\ell\nu$ at $\sqrt{s} = 1.0$ TeV

Benchmarking **Vertex Charge**

$e^+e^- \to Z^0H^0H^0$, $H^0 \to b\bar{b}$

$e^+e^- \to f\bar{f}$, $f = \tau, b, c$ at $\sqrt{s} = 1.0$ TeV + ...



International
ILC Event DVD
+org.lcsim+JAS3

Definition of running conditions

Constraints from Physics and Machine:
geometry, material budget, point resolution, r/o speed

Dependance of Vertex Tracker on Detector Concept

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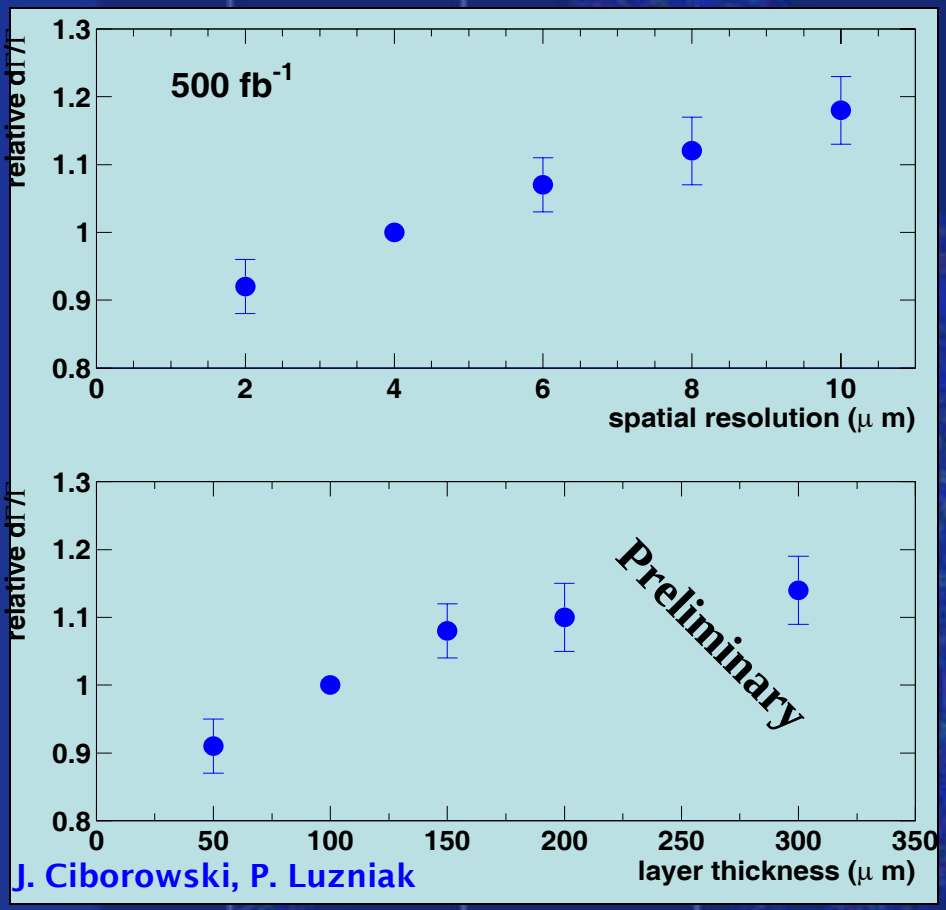
Physics Reactions, Physics Objects Reconstructed by Vertex Tracker

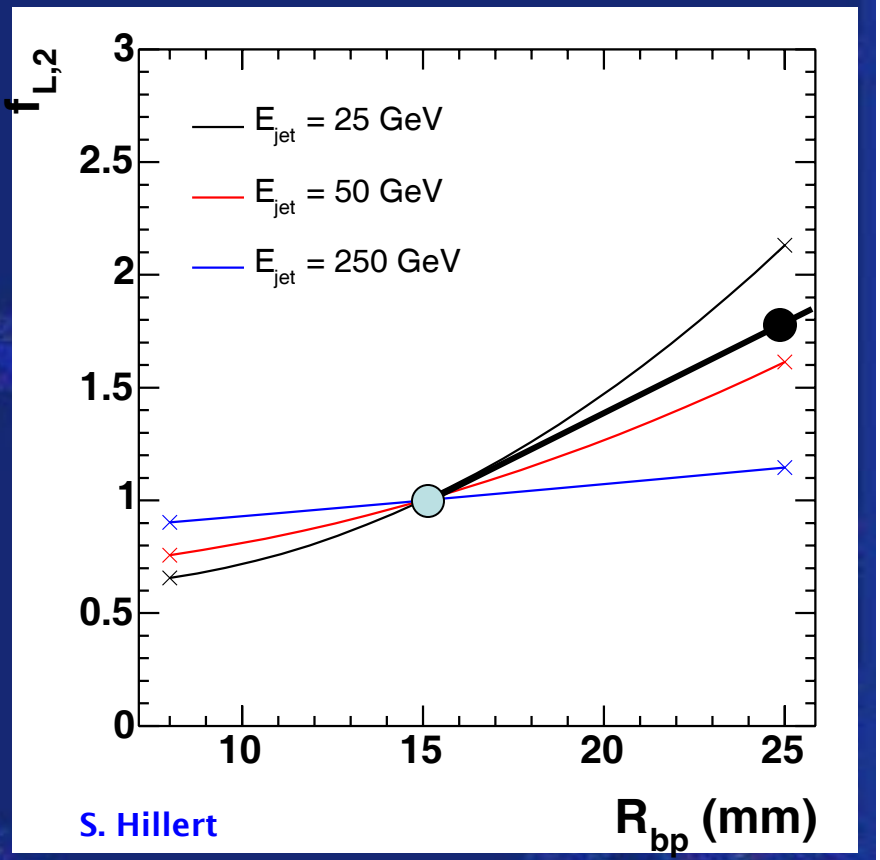
Examples of effects of single point resolution, layer thickness, innermost layer on physics performance (**Preliminary**)

Relative Effect on BR(H→cc) Accuracy of Single Point Resolution, Layer Thickness



J. Ciborowski, P. Luzniak

Relative Effect on Vertex Charge (equivalent Luminosity) of Beam-Pipe Radius

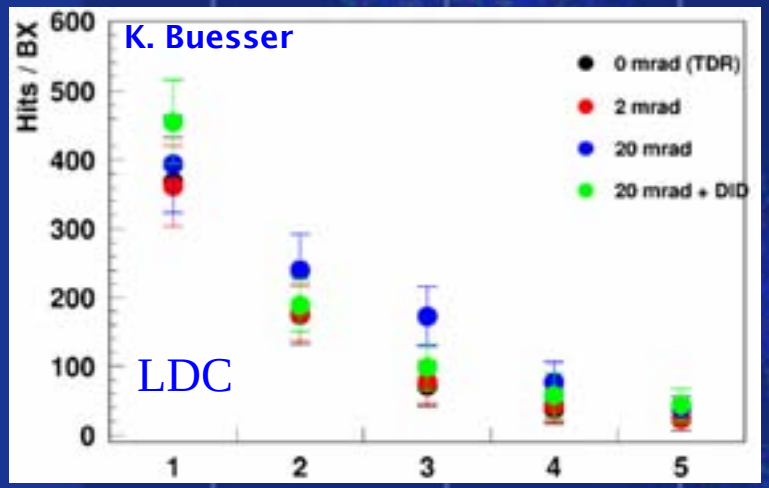


S. Hillert

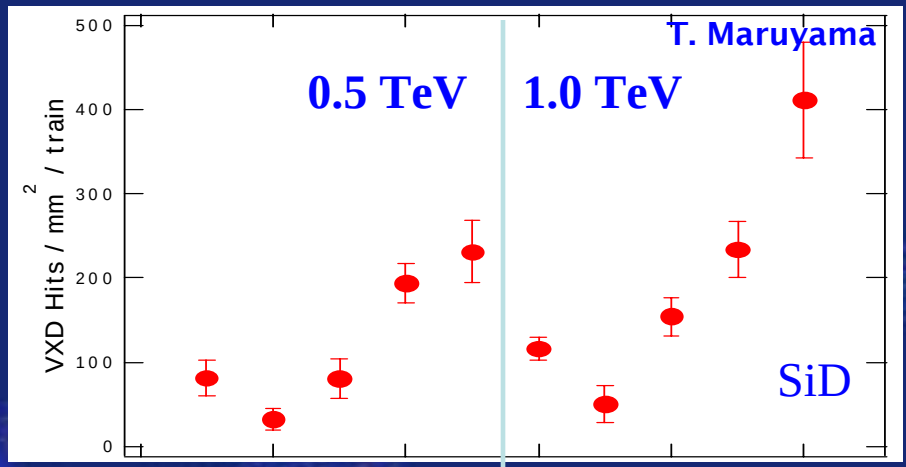
Occupancy from Pair Background

Estimate reference nb. of hits/BX at R_1
+ range of ILC parameters (x2)
+ code uncertainty (x1.2) + safety margin (x1.5)

~400 hits/BX at 0.5 TeV nominal parameters
⇨ need tolerance to > 1000 hits/BX at 1.5 cm



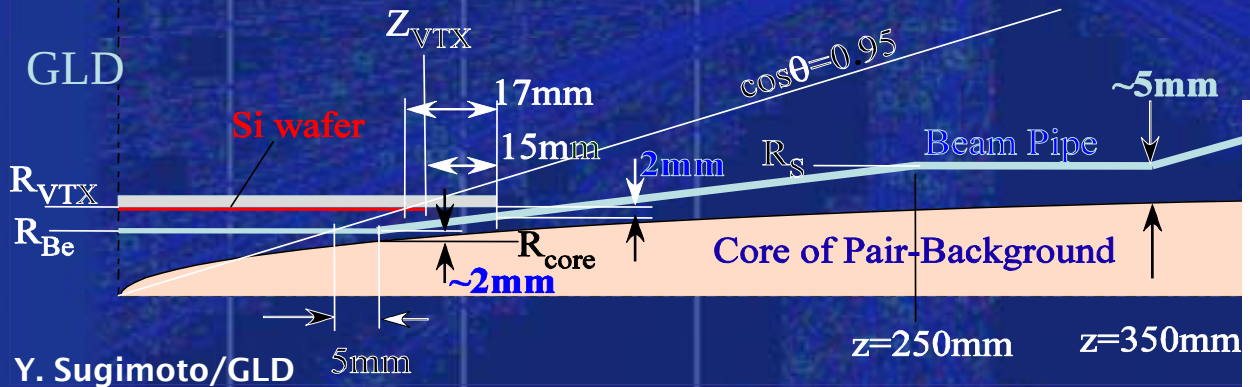
VTX Layer



(+C. Rimbault)

ILC Parameters

Clearance from deflected pair envelope:



Y. Sugimoto/GLD

$$R[cm] = 0.35\sqrt{\frac{N}{10^{10}}\frac{1}{B[Tesla]}z[cm]\frac{1}{\sigma_z[mm]}}$$

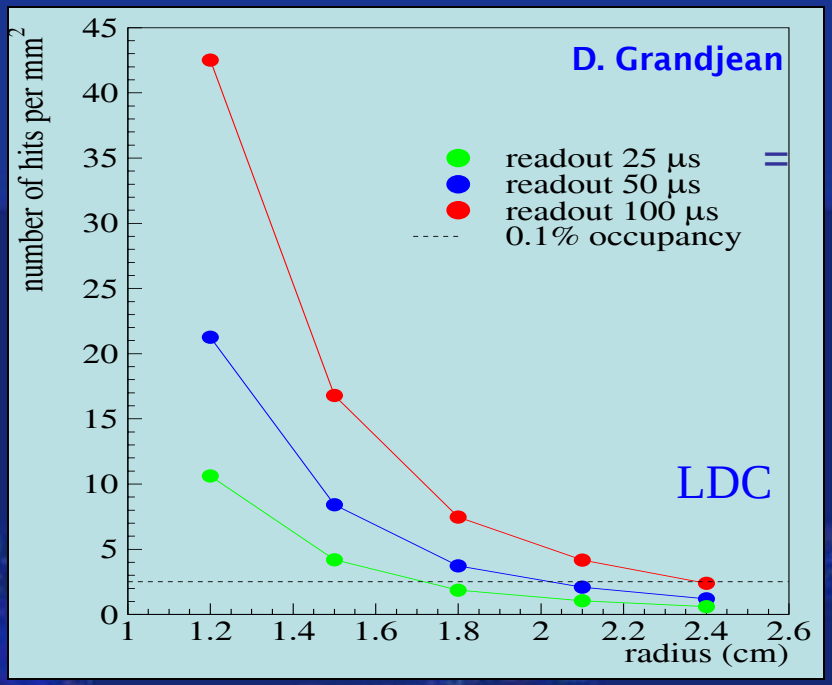
$$z[cm] = 8.3\ R^2 B[Tesla]\sigma_z[mm]\frac{10^{10}}{N}.$$

Background implication for r/o speed

Machine induced background on innermost layer is a prime driver for sensor R&D;

Essential to have continuous guidance from ILC WG4 on background estimates and **needed safety margins;**

Need to consider **other backgrounds sources** such as synchrotron radiation.



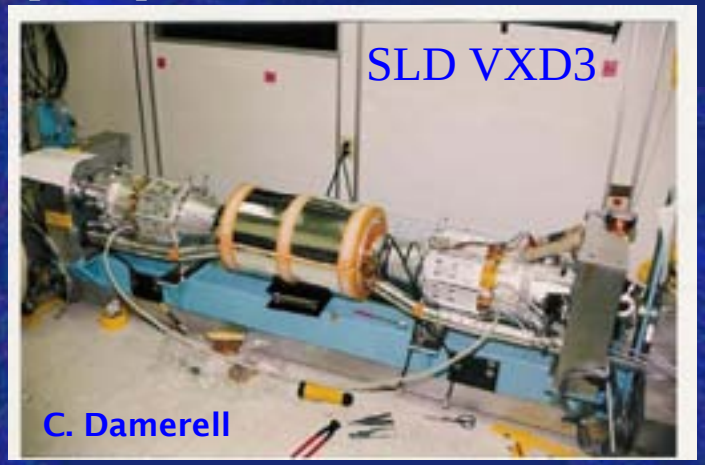
= **80 BX**

ElectroMagnetic Interference

RF leaking out of beam pipe may induce severe pickup in sensitive Si sensors read during bunch train;

Important experience from SLD, but also from TOTEM, HERAB, LHCb;

Proper design of Faraday cage and development of EMI immune architectures for Si sensors; plan test facility at Univ. of Bristol.



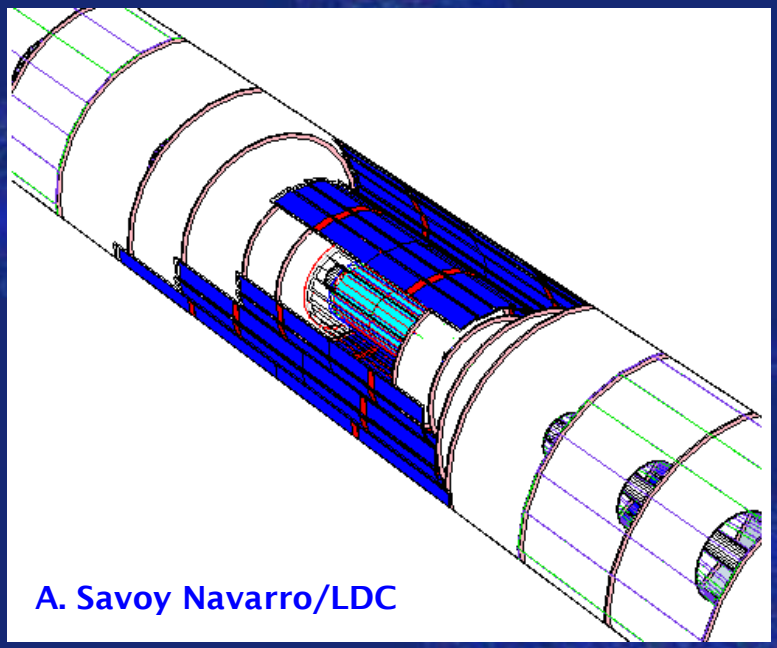
Vertex Tracker and Detector Concepts

Dependence of VTX Design on Detector Concept:
B Field and Innermost Radius;

Number of layers and standalone pattern recognition;

Consider five-layer Vertex Tracker
with R_1=1.4/1.5/2.0 cm and R_5=6.0 cm

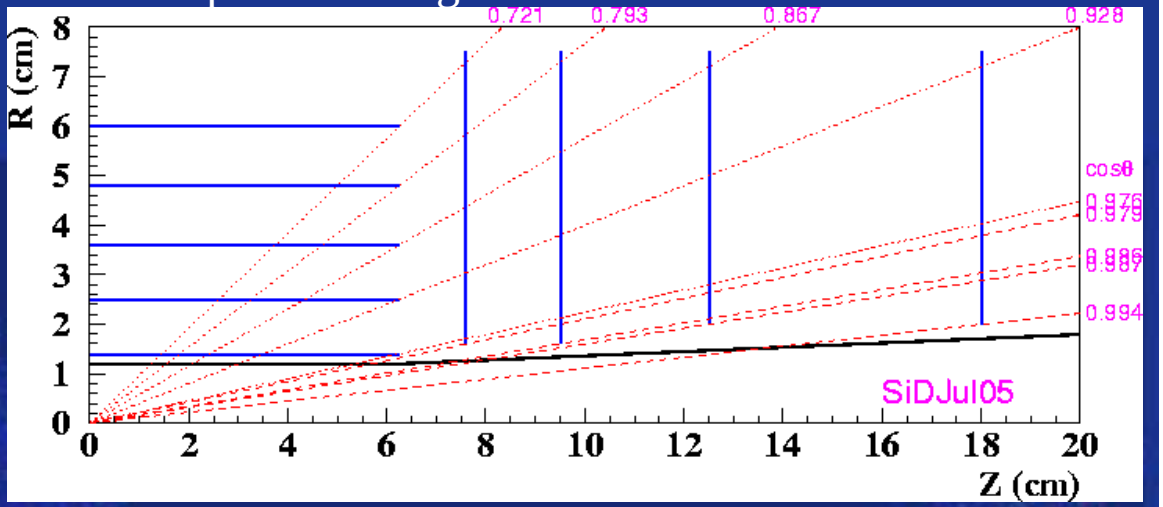
Relation of Vertex Tracker to surrounding Tracking Detectors: Mechanics, Technology, ...
Understand barrel-forward transition in relation to material,



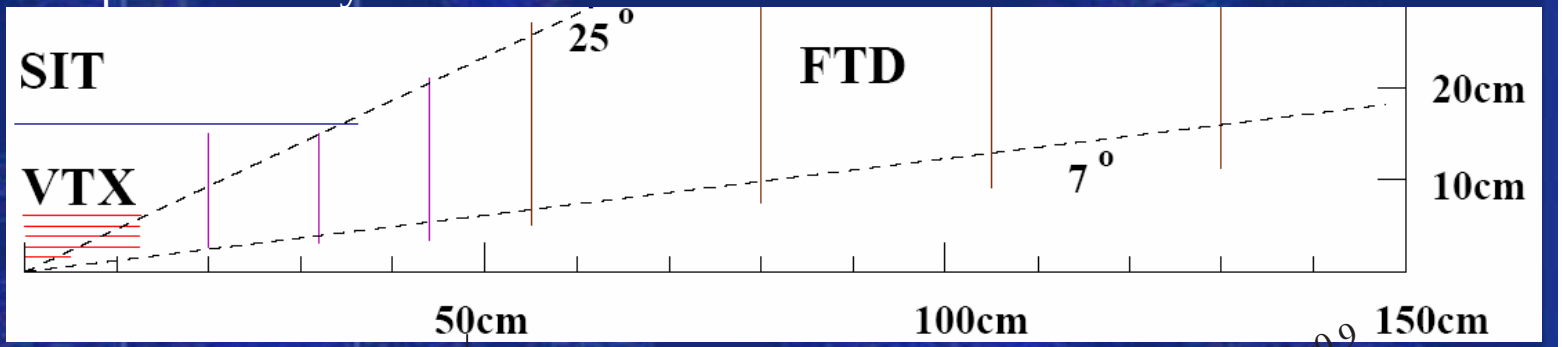
A. Savoy Navarro/LDC

Detector concepts already exploring parameter space of designs:

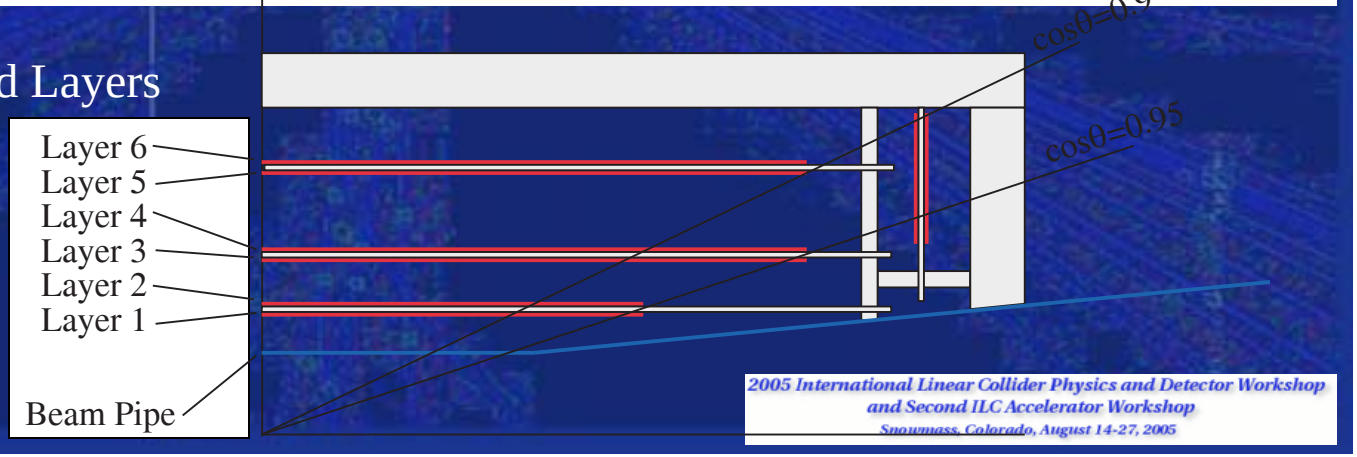
SiD: Short Barrel Equidistant Layers
+ Disks



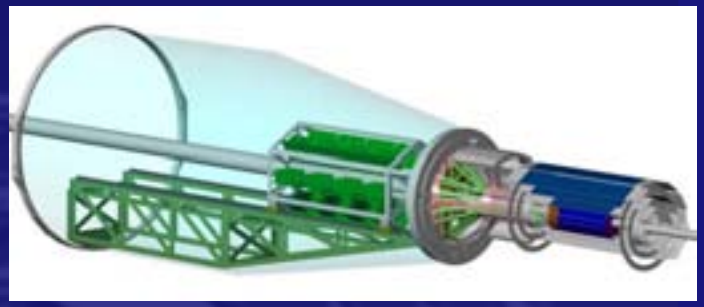
LDC: Long Barrel Equidistant Layers



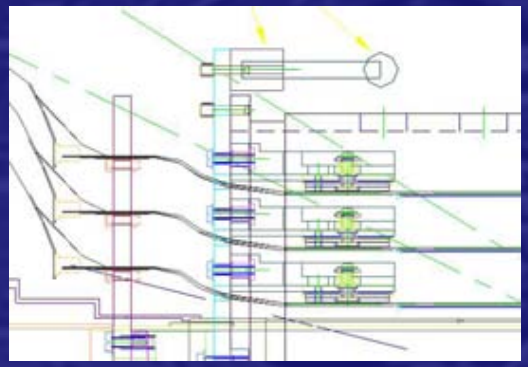
GLD: Long Barrel Grouped Layers



Vertex Tracker Engineering Design



Mechanical support,
Cooling,
Cabling,
Installation and Maintenance,
Alignment

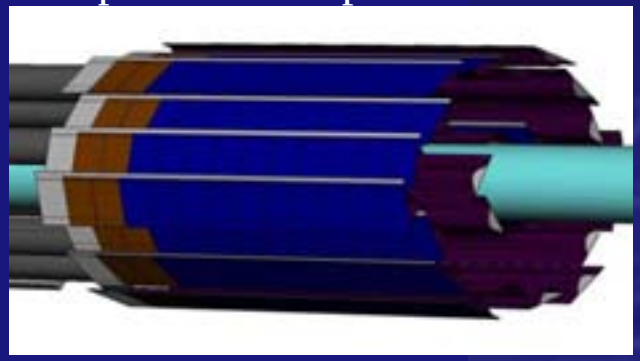


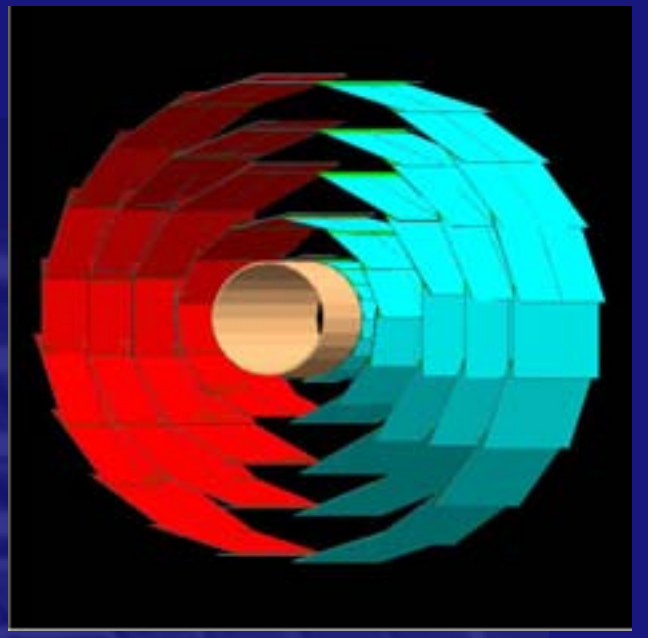
Technology/Architecture dependence of Engineering Design

Vertex Tracker Engineering Design

Challenging target of ~0.1%X_0/layer;

Important extrapolation from experience at SLD VXD3 and present development for STAR VTX upgrade;

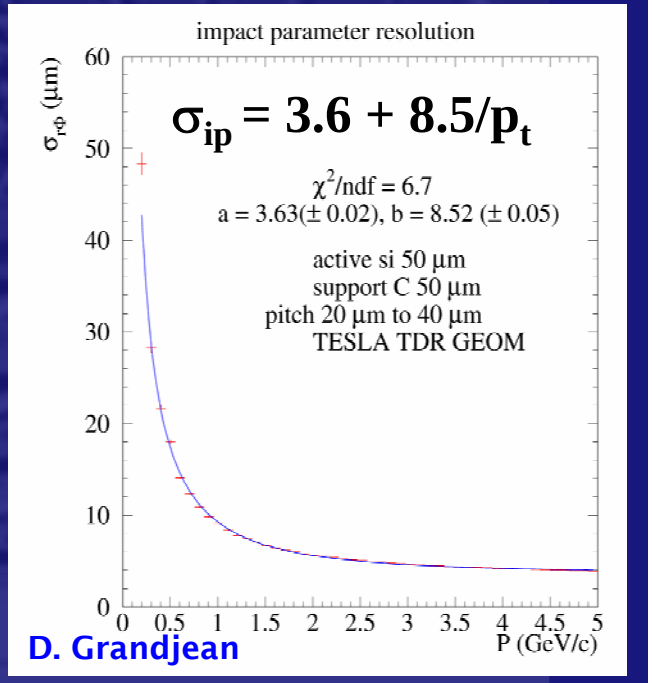




Definition of overall material budget rescaled from VXD3

	SLD VXD3	ILC VTX
Beampipe liner	Ti 50μm 0.14%	Ti 25μm 0.07%
Beampipe	Be 760μm 0.22%	Be 400μm 0.14%
Inner gas shell	Be 560μm 0.16%	0
Ladder/layer	0.41%	0.11%
Outer gas shell	Be mesh 0.48%	0.28%
Cold N2 Gas	0.05%	0.05%
Cryostat coating	Al 500μm 0.58%	0.22%
Cryostat foam	Urethane 0.44%	NilFlam 0.12%

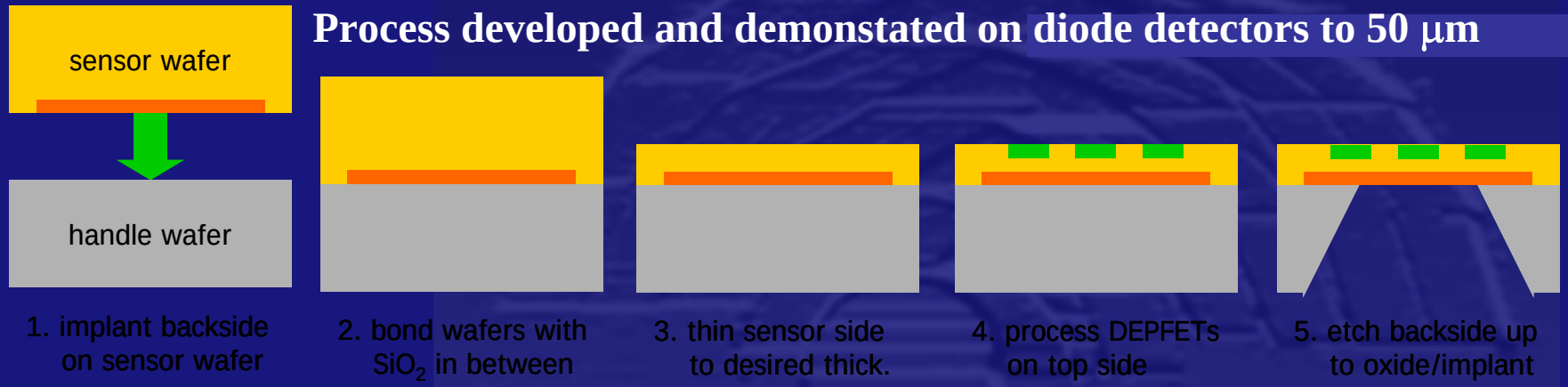
Su Dong/SiD



D. Grandjean

Sensor thinning

DEPFET Detector thinning technology at MPI Munich relies on wafer bonding technology processing of sensor wafer backside before wafer bonding

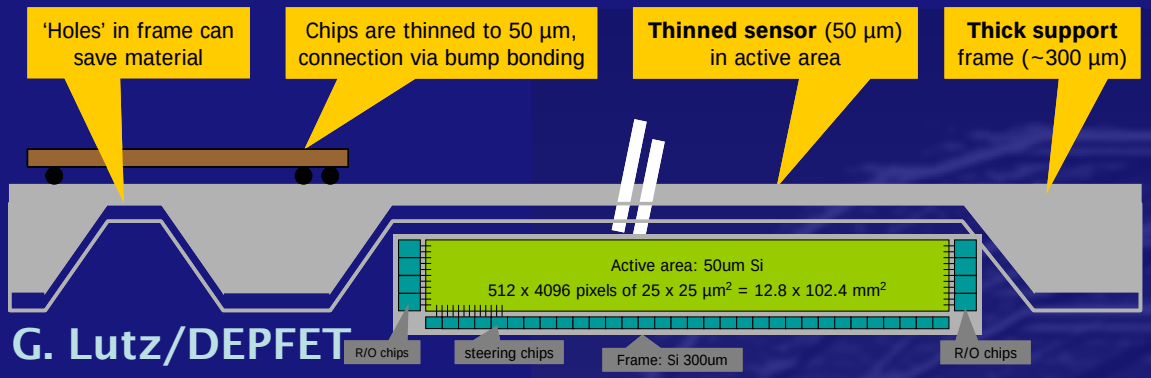


Process developed and demonstated on diode detectors to 50 μm

MIMOSA 5 **CMOS pixel chips backthinned to 50 μm** and to epi layer: **sensors tested after thinning and function**, full procedure assessment and **detailed characterisation currently in progress** for different thicknesses

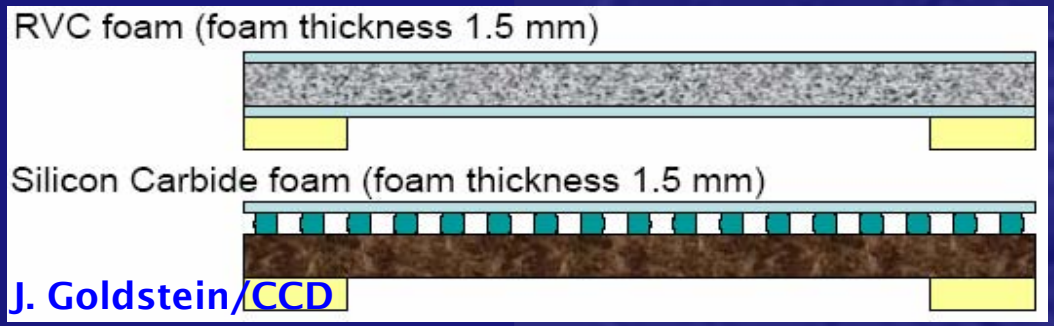
CCD sensors thinned to epi layer (20 μm)

Ladder Designs



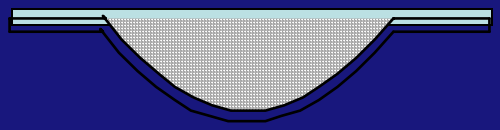
G. Lutz/DEPFET

Thinned Si 50µm	0.05% X_0
Steering Chip 50µm	0.01% X_0
Support frame	0.05% X_0
Total	0.11% X_0



J. Goldstein/CCD

Thinned CCD 20µm	0.02% X_0
RVC +Dummy Si or Si Carbide foam	0.09% X_0
Total	0.11% X_0

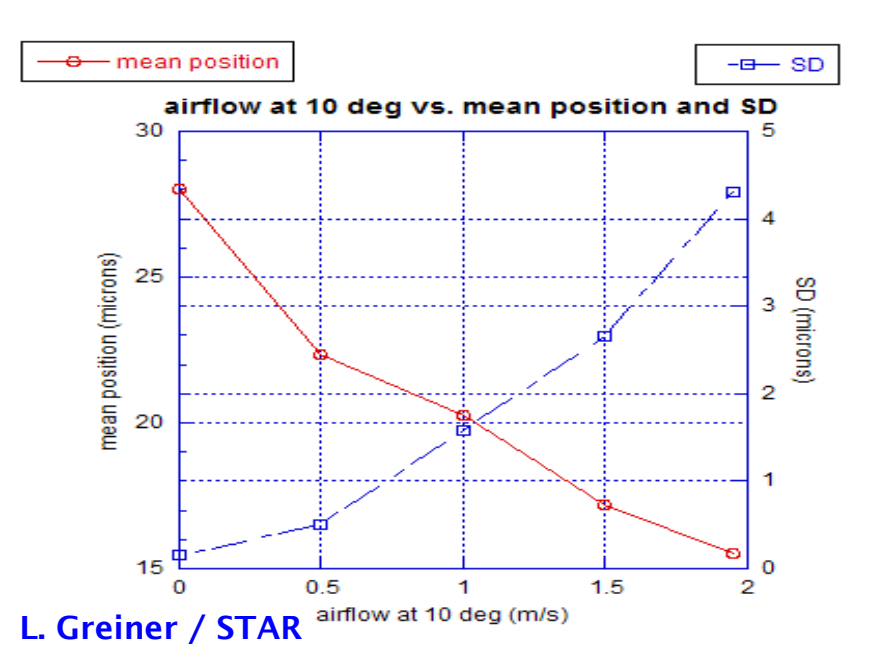


L. Greiner/CMOS

Thinned Si 50µm	0.05% X_0
RVC Fill + CFC 100µm shell	0.08% X_0
Total	0.13% X_0

Cooling

1 m/s airflow should be sufficient to remove power:
STAR VTX tests: power dissipation **67.5 mW/cm²** with **0.8 m/s** airflow ⇨ **+5°C** above ambient T;



Low ILC duty cycle provides **power dissipation reduction** up to 200, dependent on **power cycling**, needs detailed testing;

Cooling airflow effect on ladder position appears manageable by providing mechanical anchor at both ends and parallel air flow;

Choice of Operational temperature depends on technology, architecture, point resolution and backgrounds

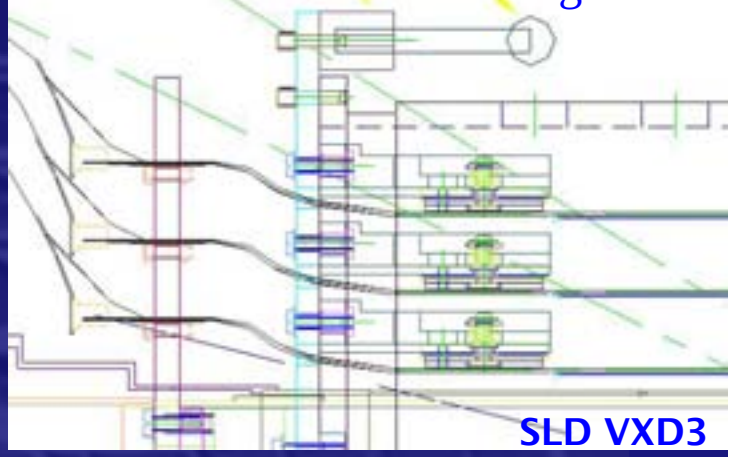
Addition of a light cryostat for cold operation does not represent major burden to overall material budget ~ 0.4% X_0;

Endcap Region Material

	SLD VXD3		SiD VXD
Barrel Endplate	**Be/Fe/gap 3mm**	**1.5%**	**Composite 0.5%**
Barrel support annulus	**Be**	**~2.4%**	**1.0% ?**
Ladder blocks	**Al_2O_3 (smeared)**	**3.0%**	**1.0% ?**
Striplines	**Kapton/Cu**	**0.5%**	**0.2%**
Stripline clamp support	**Be plate w/ holes ~1.0%**		**0**
Stripline connectors	**smear**	**0.14%**	**0**
Cryostat	**Foam**	**0.4%**	**0.4%**

Su Dong/SiD

Guidance from VXD3 design



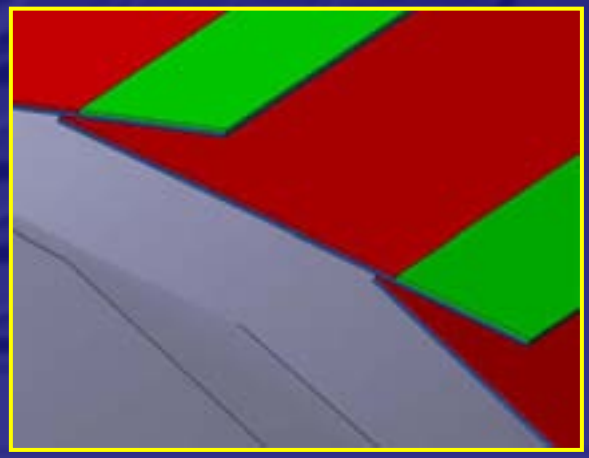
Challenge to reduce Endcap material by innovative design.

Alignment

Internal alignment must provide position with accuracy comparable to single point resolution O(1 μm);

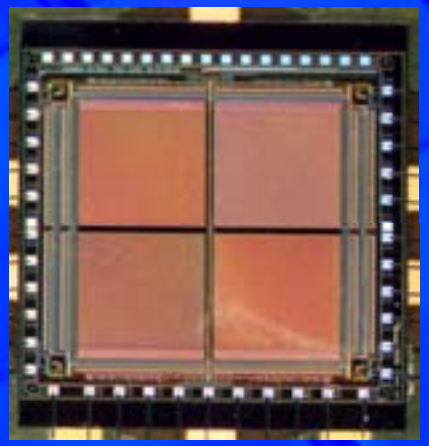
Ladder Survey, track alignment through overlaps, position sensors defining stability periods for integrating tracks for alignment;

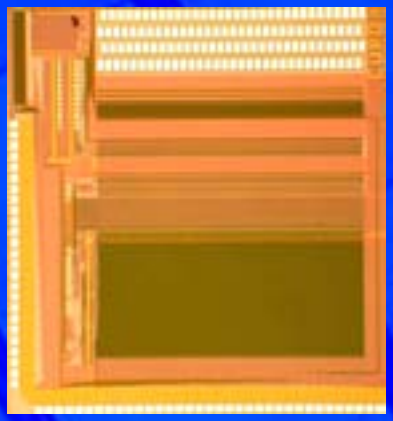
Alignment wrt external tracking detectors.

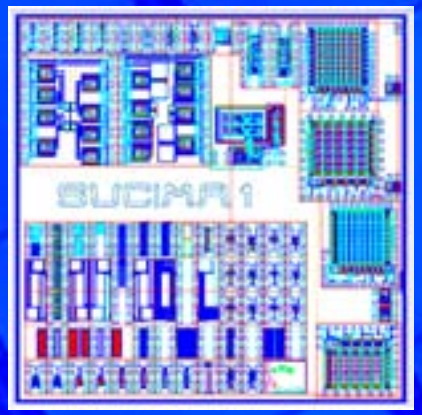


Vertex Tracker Sensor R&D

Review of current R&D







Characterisation of:
Single point resolution, Sensor Thickness,
Read-out Speed, Power Dissipation, Radiation Hardness

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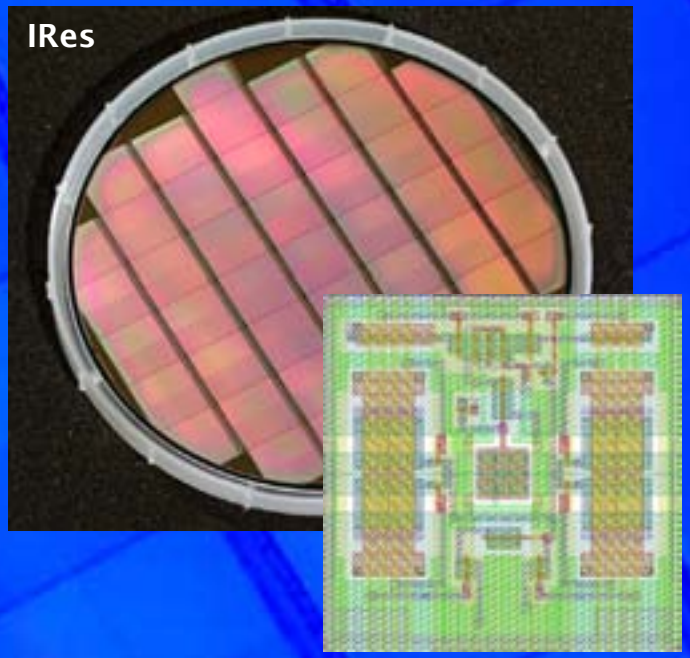
CMOS Pixel Sensors

Europe: IReS-Strasbourg, LPSC-Grenoble, LPCC-Clermont, DAPNIA-Saclay (France), DESY, U. Hamburg, (Germany), LCFI (UK), U. Roma 3, U. Insubria, U. Perugia, U. Pavia (Italy)
US: UC Berkeley, LBNL, Yale U., U. Oregon
Synergies with: STAR/RHIC (LBNL, BNL), CBM/GSI (GSI, U. Frankfurt), BELLE (U.Hawaii), BES applications (LBNL)

Integrate **sensitive cell and electronics in same substrate**

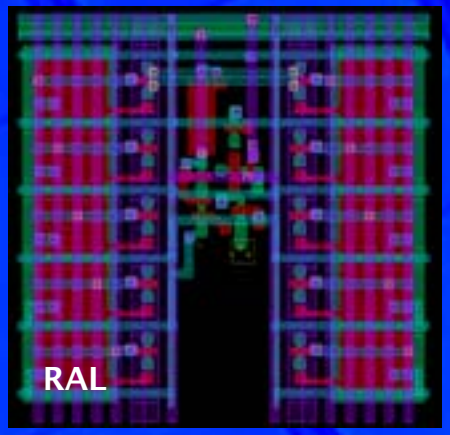
Various architectures developed:

Continuous Read-out:
Fast Column Parallel Architecture

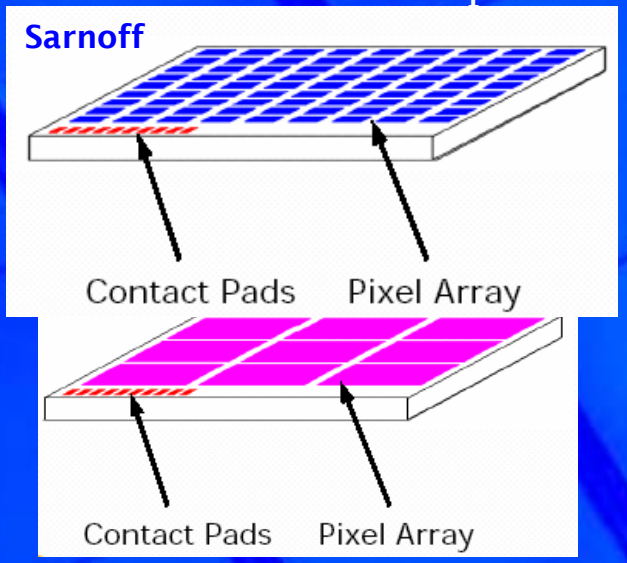


Delayed Read-out

Multi-memory Cell Pixels (FAPS)



Micro-Pixels
Macro-pixels

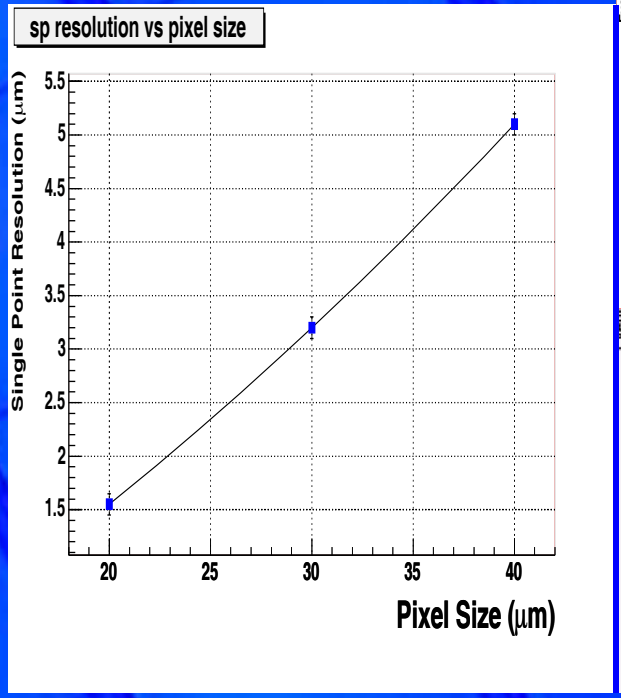


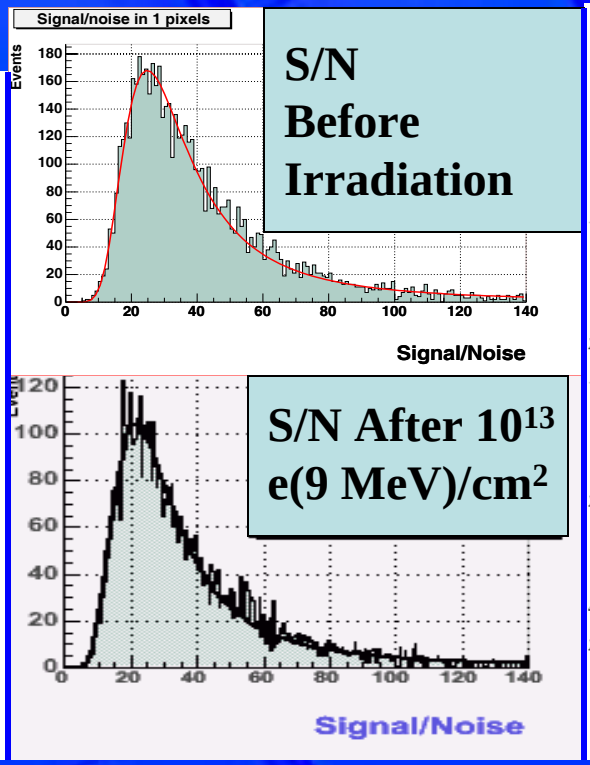
Single point resolution demonstrated down to 1.5μm and 2-hit separation

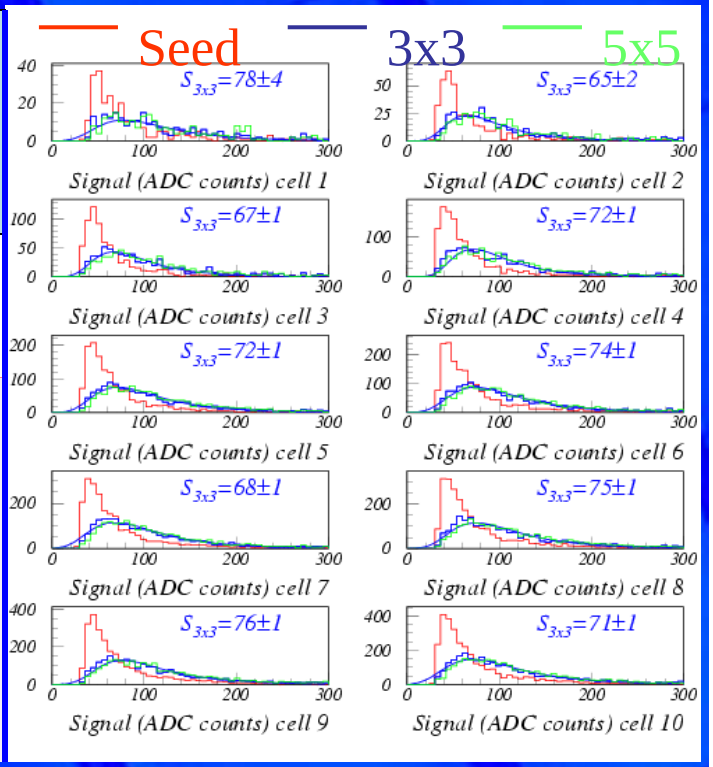
Radiation tolerance: demonstrated with neutrons, $e^{\pm}$(10 MeV), X-Rays, up to doses significantly above ILC

First Results of FAPS with Ru Source successful

100 GeV π Test Beam Results







Pixel architecture integrating CDS works;
current effort mostly devoted to **increase read-out speed**
and achieve **on-chip fast signal digitisation and sparsification**
Air flow sufficient for removing power dissipated
(adopting power cycling: 3-30 W)

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DEPFET Sensors

Europe, Bonn U., Mannheim U., MPI Munich, HLL (Germany)

DEPFET sensor-amplifier structure:
FET transistor on fully depleted and sensitive bulk;

Small size, thick prototypes produced in MPI laboratory with complete silicon technology, **in house capability** to build all ILC VTX sensors;

Prototype Module electronics with nearly full functionality developed and tested with prototype sensors;

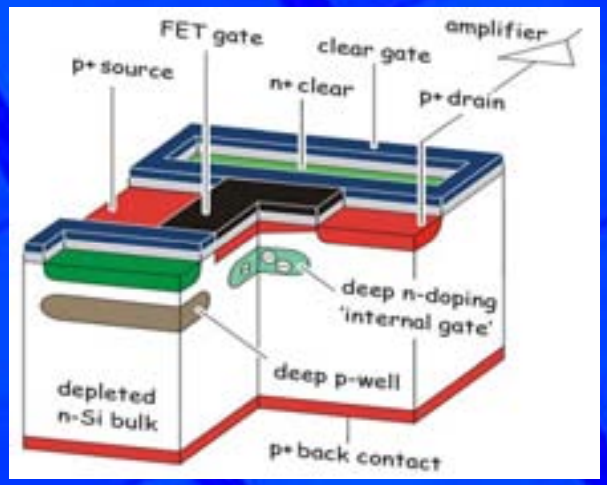
Readout and data sparsification with 20 frames/train;

Radiation hardness to 1 Mrad ^{60}Co tested,
expect good neutron tolerance;

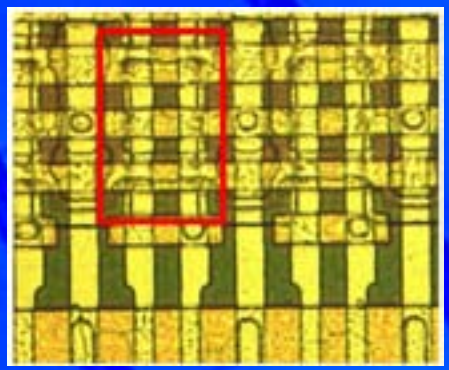
L**ow power consumption** (4W for full detector)
operate at **room temperature** with air flow cooling;

Operation of small size prototypes demonstrated;

Current R&D to obtain fully engineered and tested system.



Micrograph of prototype sensor
(128x64 pixel, double pixel cell 33 x 47 µm^2)

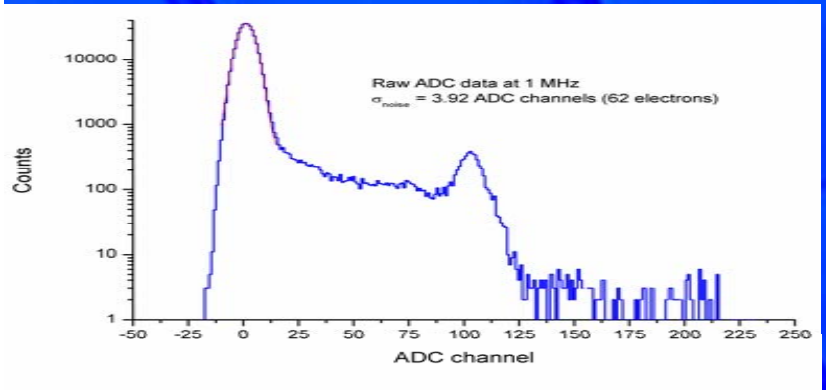


Charge Coupled Devices

Europe: LCFI (UK)
Asia: KEK (Japan)

CCD technology for low mass high resolution detectors established,
need to develop architecture able to cope with cold machine beam structure:

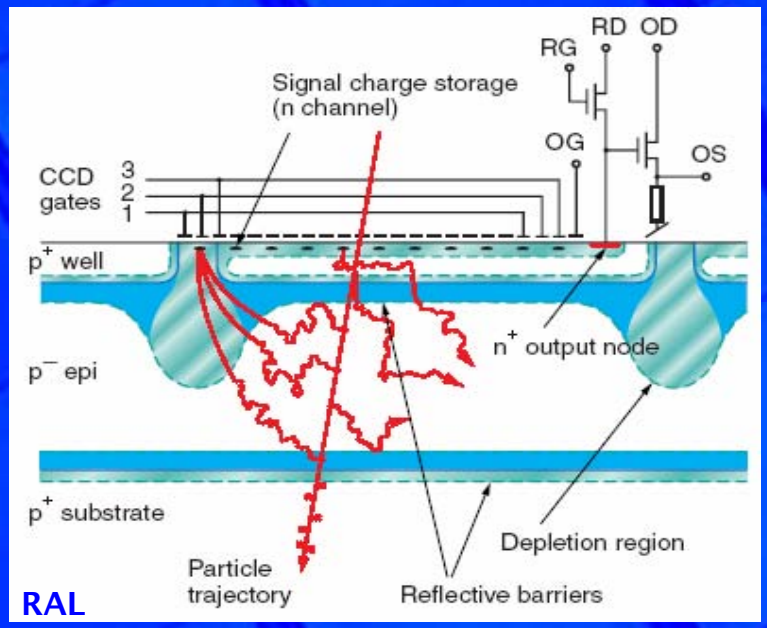
Column Parallel CCD



CPCCD operation demonstrated with
Max. clock frequency 25 MHz and
low voltage clock signal 1.9 V.

New CPCCDs (from e2v) ready Sept. 2005,
include **50 MHz devices**
CCDs with 92 x 15 mm^2 imaging area.
New readout chip under test, including
digitisation, cluster finding and data sparsification.

In-situ Storage Image Sensor (ISIS)



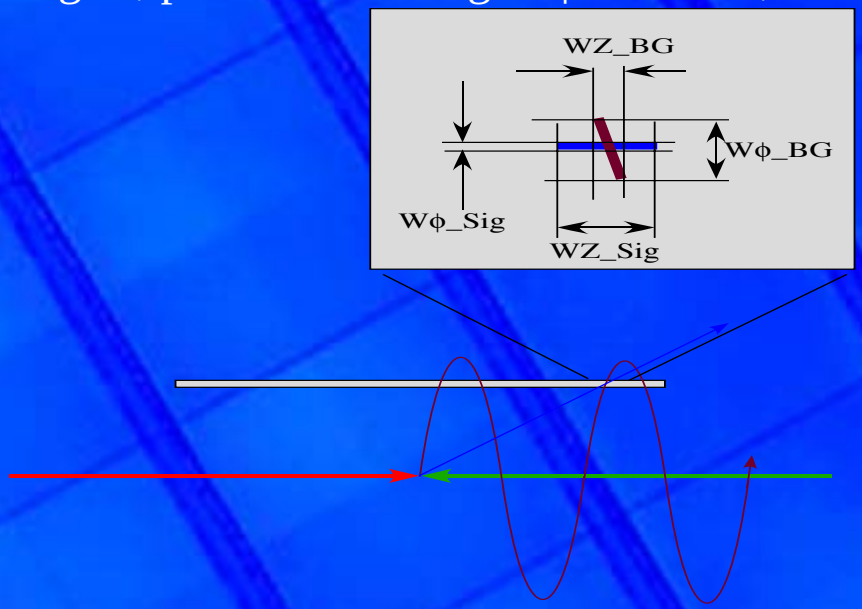
Relaxed **readout in inter-train gap;**
Robust against EMI.
First "proof of principle" device
expected in Sept. 2005 from e2v.

Fine Pixel CCDs

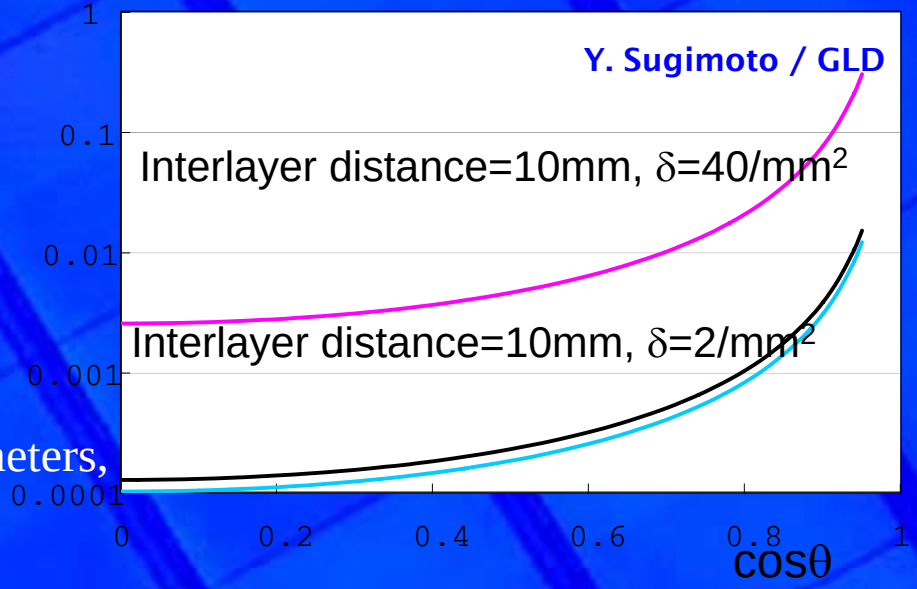
Pixel size ~ 5 x 5 μm²,
~ 20 times "standard" pixel number;
Readout between bunch trains;

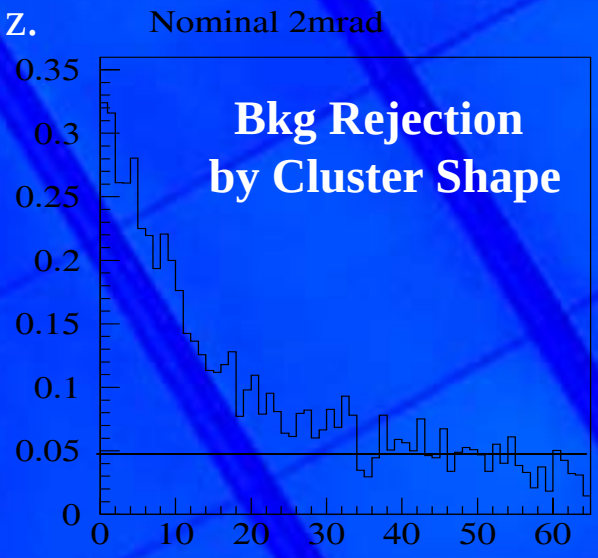
High bkg hit density **δ=40 hits/mm²/train** at
R=2.0cm, B=3 T, nominal 0.5 TeV ILC parameters,

Need to reduce pair bkg using cluster shape:
at large z, pair clusters long in ϕ direction, track clusters in z.



Confusion rate for 1 GeV Track Pattern recognition

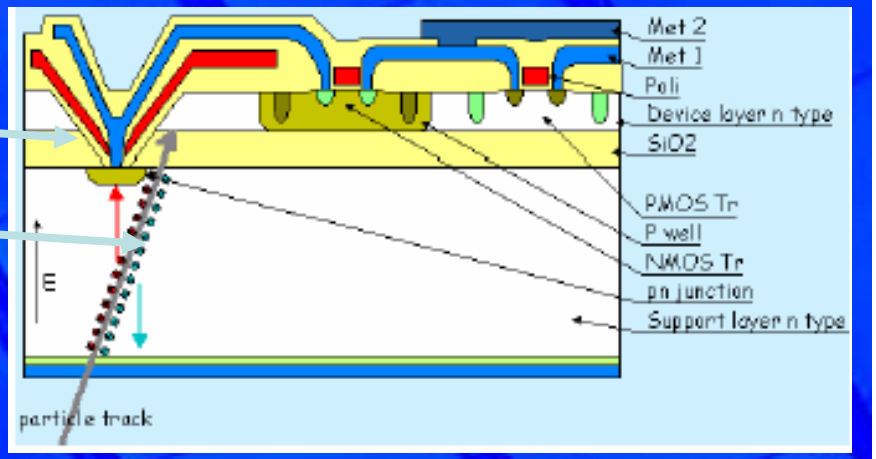


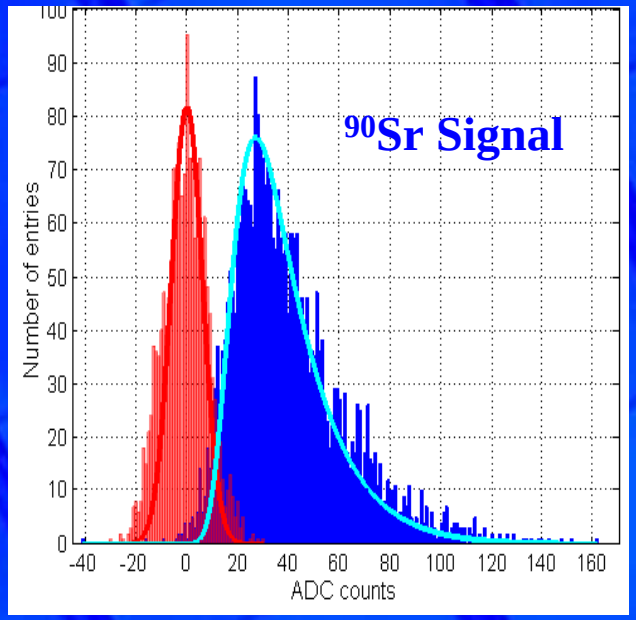


Silicon on Insulator (SoI)

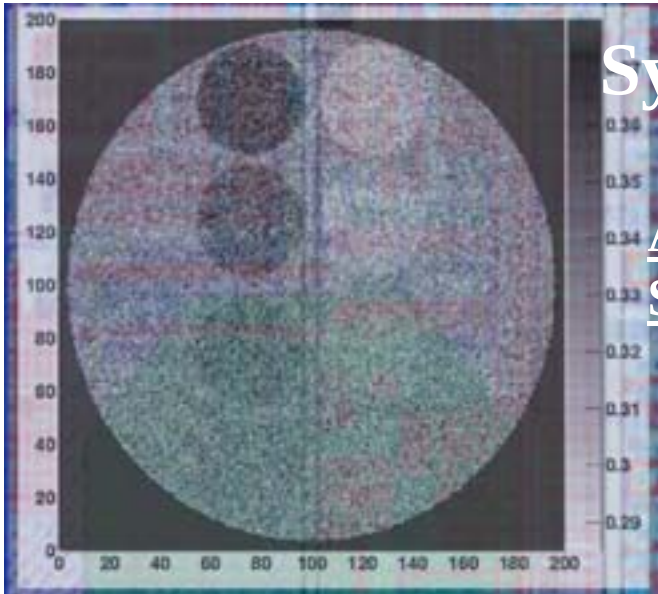
Europe: U. Insubria & INFN (Italy),
IET + AGH (Poland)

CMOS electronics
High resistivity fully depleted
sensitive volume
Not standard process
Development started 3 years ago
Proof of principle accomplished
ILC dedicated development being defined with partner company





Synergies with Pixel Sensor Applications beyond ILC and HEP



Applications of imaging capabilities of position sensitive Si radiation detectors:

Mammography screening, Dental Radiography

Dosimetry of brachytherapy sources

Radiotheraphy beam profilometry

Sensitive element in HPD

Electron Microscopy

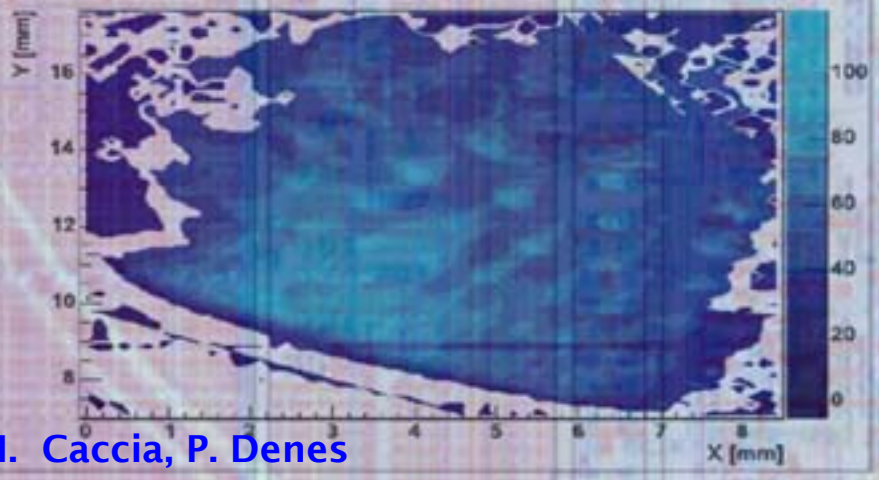
Imaging with crystallography beam

Imaging at Syncrothron Light Sources

Astronomy: solar spectra analysis

Astronomy: X ray spectroscopy imaging

HEP sensors useful as demonstrator; significant R&D synergies with applications; several success stories but significant effort has to be invested.



M. Caccia, P. Denes

2005 International Linear Collider Physics and Detector Workshop and Second ILC Accelerator Workshop
Snowmass, Colorado, August 14-27, 2005

Status of the ILC Vertex Tracker

Detailed studies of Physics reactions, but also of Physics Observables (such as Vtx Charge), are stressing the importance of thin detector layers and small radius of innermost layer. Start of activity of Detector Concepts provides now the tools to re-assess the Physics and Event Reconstruction requirements on well-defined benchmarks with realistic detector description, simulation and reconstruction software.

Different technologies have been developed to the point of proving that they fulfill single point resolution requirements and thinning to match the sensor material budget;

Vertex Tracker optimisation based on a large number of parameters intercorrelated and not yet fully understood: essential to pursue many options to find optimal solution in terms of performance, reliability and cost;

If different technologies are able to provide comparable performance, the two detectors should choose different Vertex detectors to minimise risks.

R&D Priorities for the ILC Vertex Tracker

Develop architecture(s) in the different technologies able to deliver performance for 1st layer: readout speed is the major critical issue;

Produce and test detector-size chips with full functionality;

Characterise detector performance for ILC-like environment (Radiation hardness, Occupancy, EMI sensitivity, ...);

Develop operational full ladder equipped with detectors and characterise it in terms of mechanical stability, power dissipation, material budget;

Important to keep and promote R&D on full range of different technologies;

Vertex Tracker R&D community confident it will achieve a baseline in four years: full ladder characterised in beam test;

Plan to build Vertex Tracker for ILC startup and then consider upgrades for higher luminosity and centre-of-mass operation possibly involving different technology or architecture.

Organising the International Vertex Tracker R&D Effort

Very significant sensor R&D effort across the three regions;

There are several areas where collaboration of groups, pursuing sensor R&D in parallel, will be highly beneficial, develop ILC VTX web page;

Development of ladder prototypes, cooling test, EMI tests, ...;

Common LCIO standard for raw and cluster data persistency:
share lab and test beam data, analysis and reconstruction tools,
validate digitised simulated events;

Collaboration during this Snowmass Workshop opening the way towards integrating activities in a larger international collaborative effort on Vertex Tracker design and R&D;

Define contact persons within the ILC Vertex Tracker community to Detector Concepts and MDI groups;

Ensure and strengthen connection with WWS R&D Panel;

Summary in Snowmass proceedings will contain first assessment of R&D directions, priorities and activities with common authorship, prepare document on test beams;

Review costs for R&D and construction based on model common with Detector Concepts;

Progress towards **White Paper on ILC Vertex Tracker R&D** by LCWS06 in March.