Beam-based Feedback Systems

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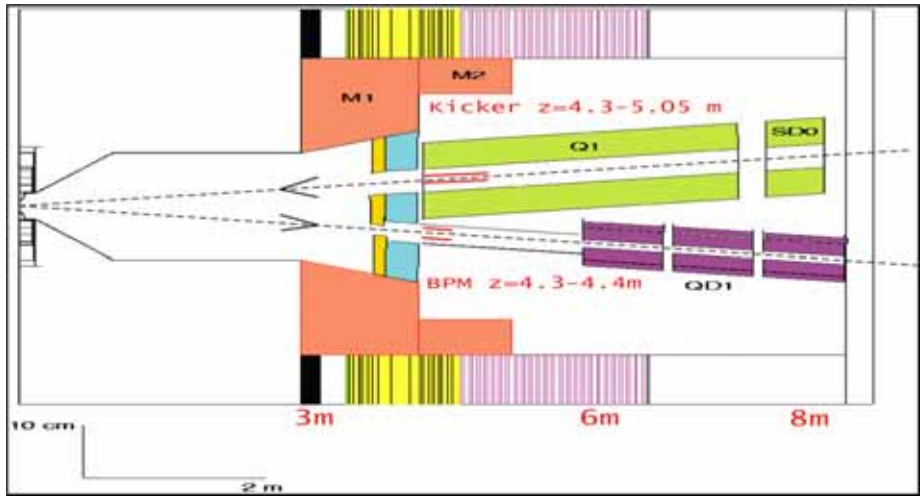
ILC Beam-based Feedback/Feedforward Systems

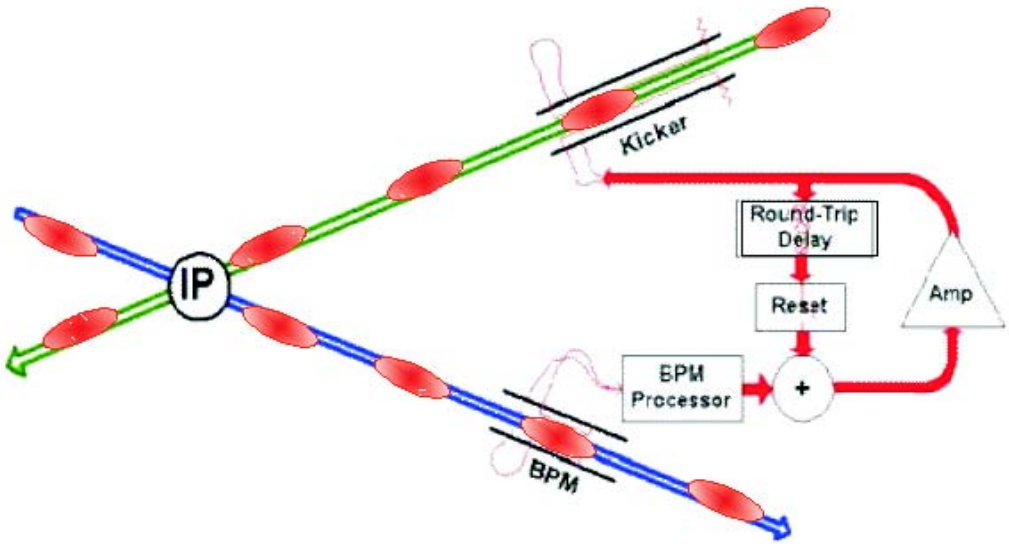
- **Intra-train (bunch-bunch) feedback at IP: 3 MHz**
- **Pulse-pulse feedback at IP: 5 Hz**
- **Orbit feedbacks upstream in BDS + in linac: < 1Hz**
- **Corrections to beam position and/or angle**
- **IP FBs: most critical in vertical dimension in order to make nanometre-sized beams collide**
- **Feed-forwards: DR → linac, linac →IP**

Critical Feedback/Feedforward Components

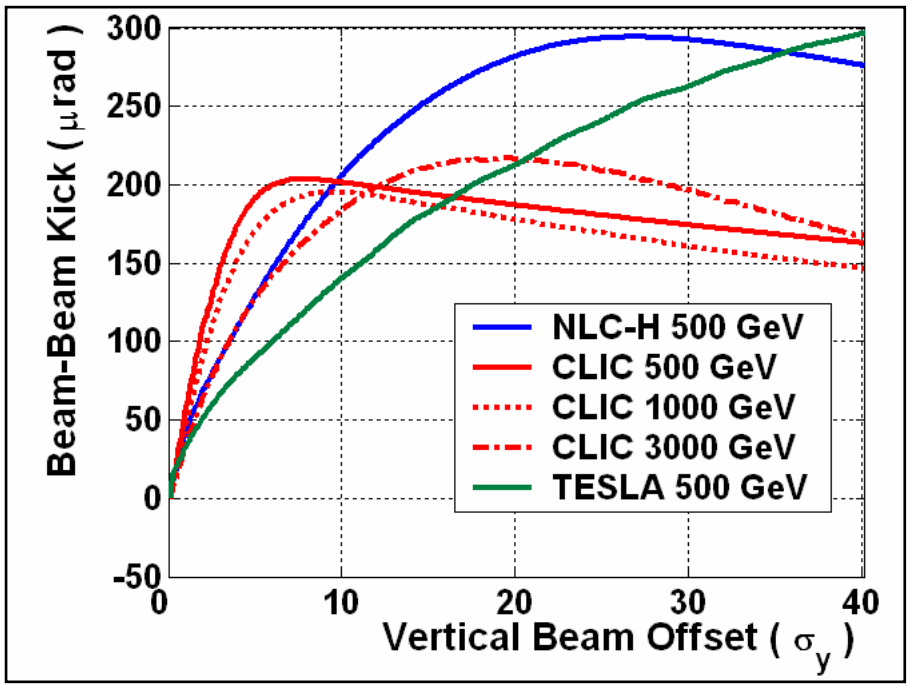
- BPMs
- BPM signal processor
- Feedback processor
- Amplifier
- Kicker



- Intra-train FB at IP:



IP Intra-train Beam Feedback



Kicker needs to provide up to 100 nanoradian deflections

→ amplifier power < 100W

For BPM (say) 4m downstream of IP:

for beam offsets < 50 sigma_y beam position signal < c. 1mm

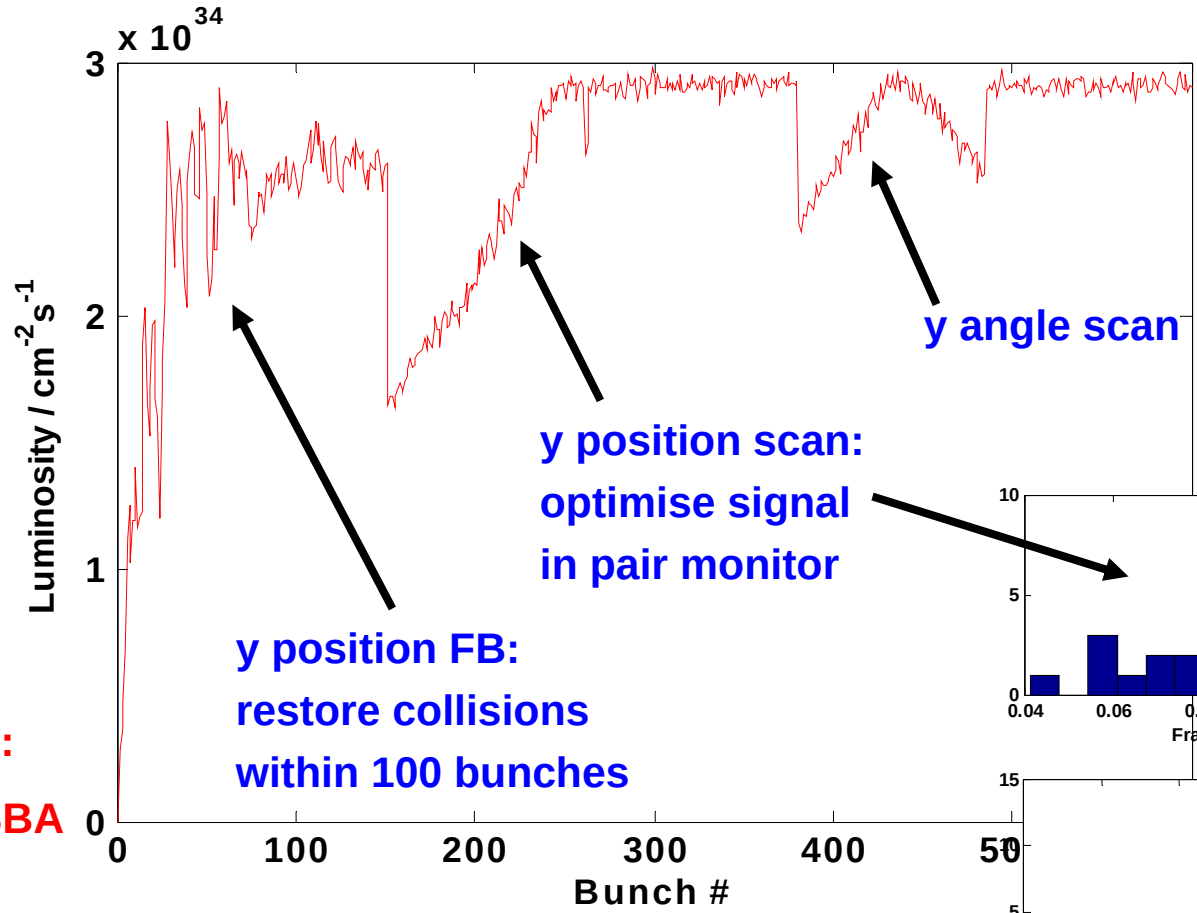
→BPM resolution of order 10 microns is adequate

→stripline or cavity BPMs ok

→cavity BPM needs <<300ns time resolution

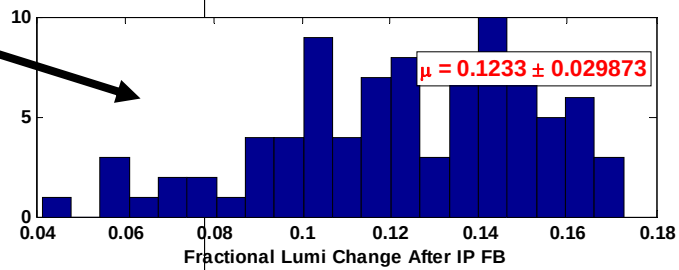
Intra-train Feedback Performance

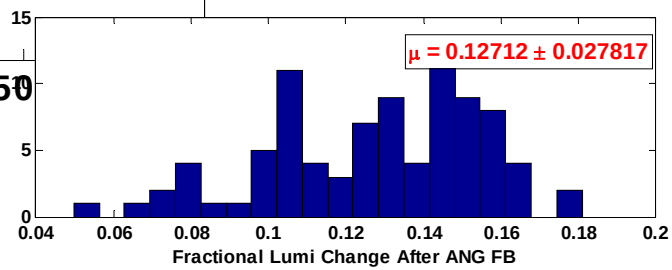
(White)



OPTIMAL LUMINOSITY

ILC IR1 (20 mrad)





1 seed:

post-BBA

+ GM

+ wakes

FONT Prototype Intra-train Analogue Feedback Systems

- **NLCTA: 65 MeV beam, 170ns train, 87ps bunch spacing**

FONT1 (2001-2):

First demonstration of closed-loop FB: latency 67ns

10/1 beam position correction

FONT2 (2003-4):

Improved demonstration of FB: latency 54ns

real time charge normalisation with logarithmic amplifiers

beam flattener to straighten train profile

solid-state amplifier

- **ATF: 1.3 GeV beam, 56ns train, 2.8ns bunch spacing**

FONT3 (2004-5):

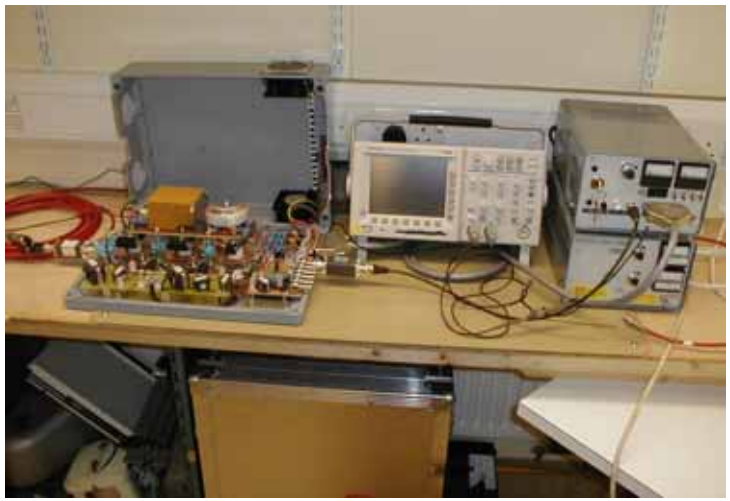
Ultra-fast demonstration of FB: latency 23 ns

3 stripline BPMs

high-power solid-state amplifier

FONT: kicker driver amplifiers

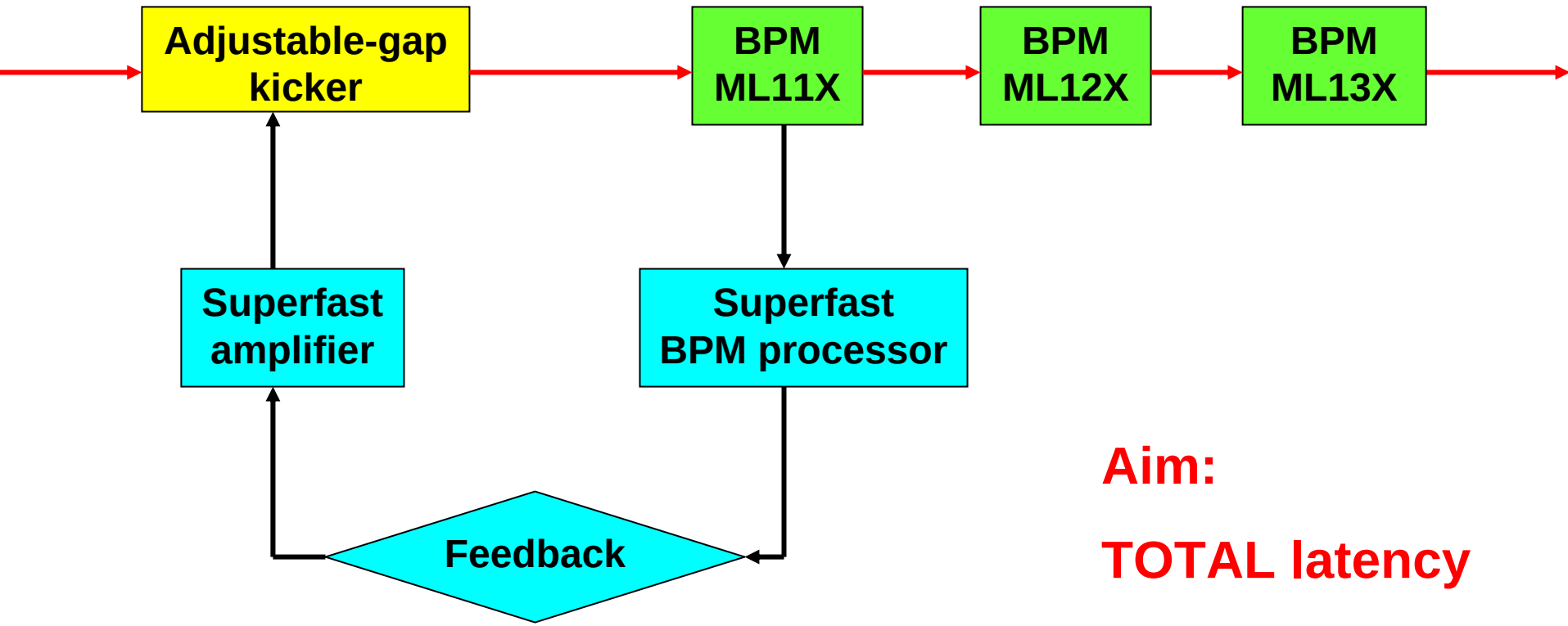
FONT1 3-stage tube amplifier



FONT3 PCB amplifer + FB

Same drive power as needed for ILC

FONT3 outline



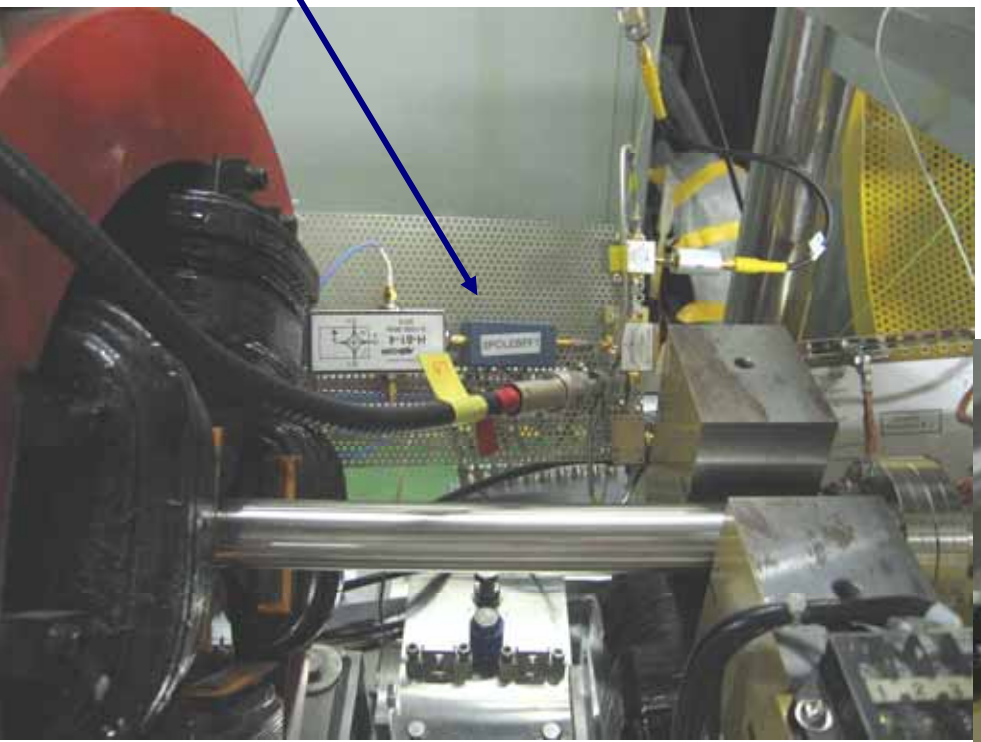
Aim:

TOTAL latency

< 20 ns

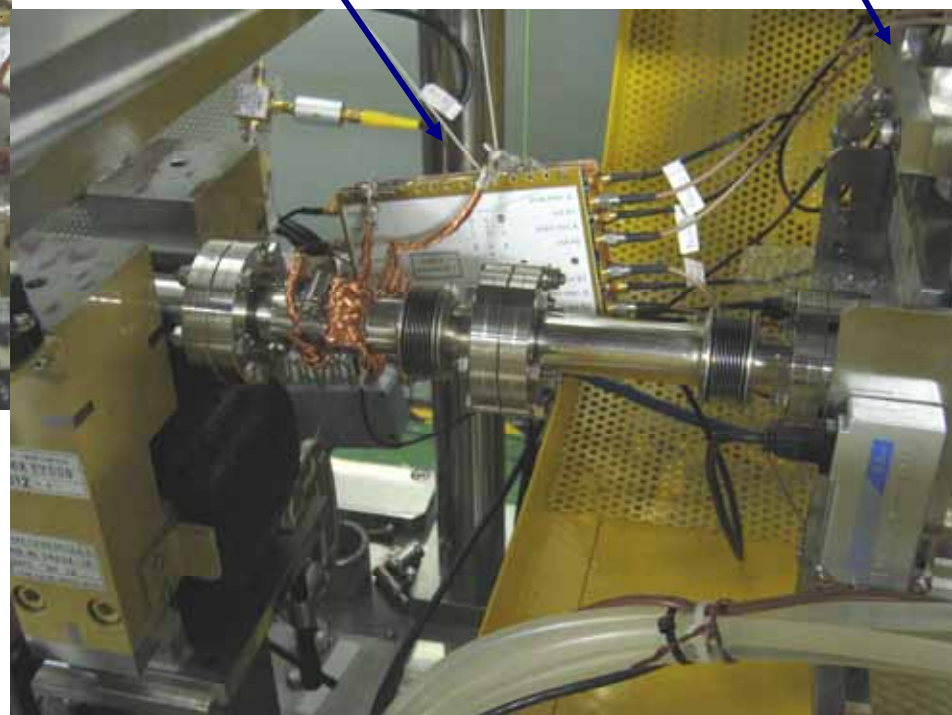
FONT3: BPM processor + amplifier/feedback installation in ATF beamline

BPM processor board



FEATHER kicker

Amplifier/FB board



BPM

Philip Burrows

FONT3: latency budget

- **Time of flight kicker – BPM: 4ns**
- **Signal return time BPM – kicker: 6ns**

  Irreducible latency: 10ns

- **BPM processor: 5ns**
- **Amplifier + FB: 5ns**

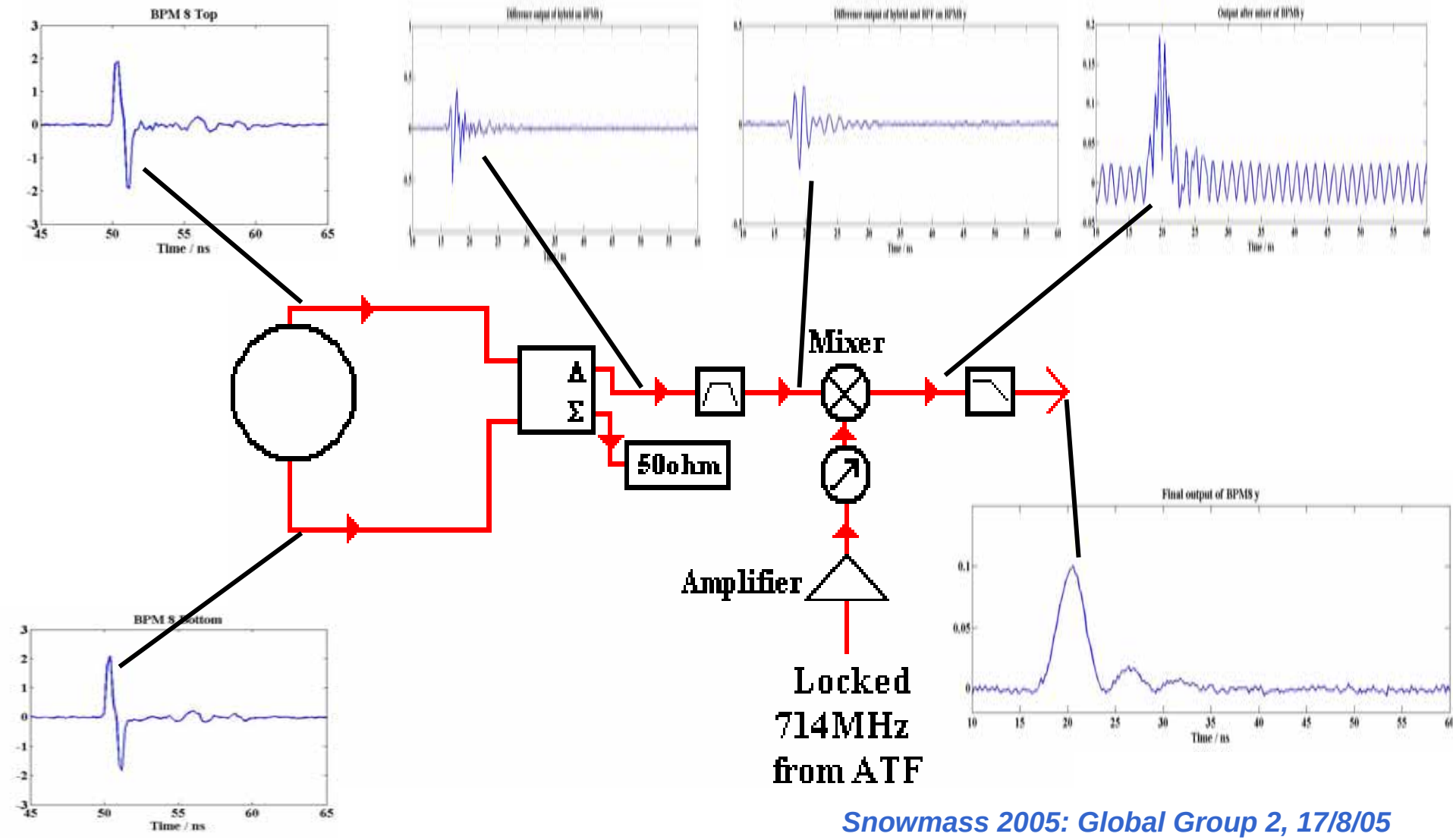
  Electronics latency: 10ns

- **Total latency budget: 20ns**

Will allow 56/20 = 2.8 periods during bunchtrain

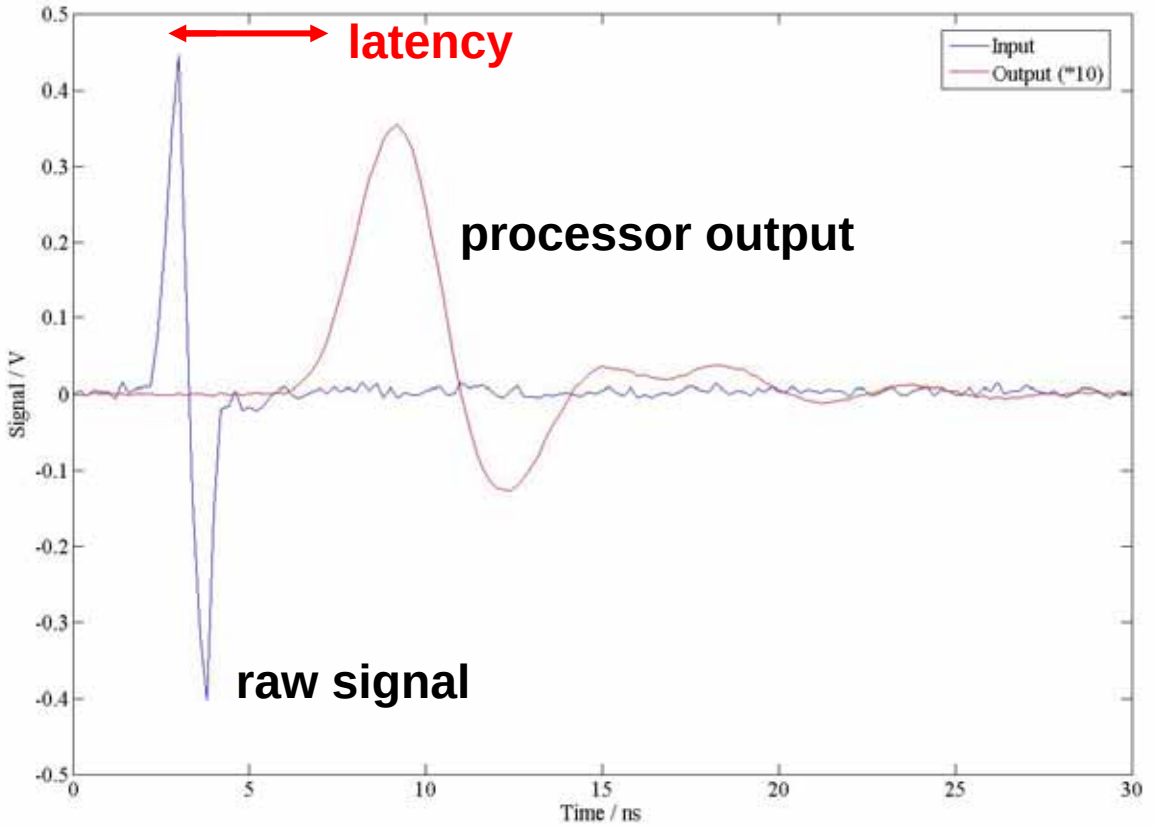
FONT3: BPM processor tests (Molloy)

(single-bunch, December 2004 beam tests)

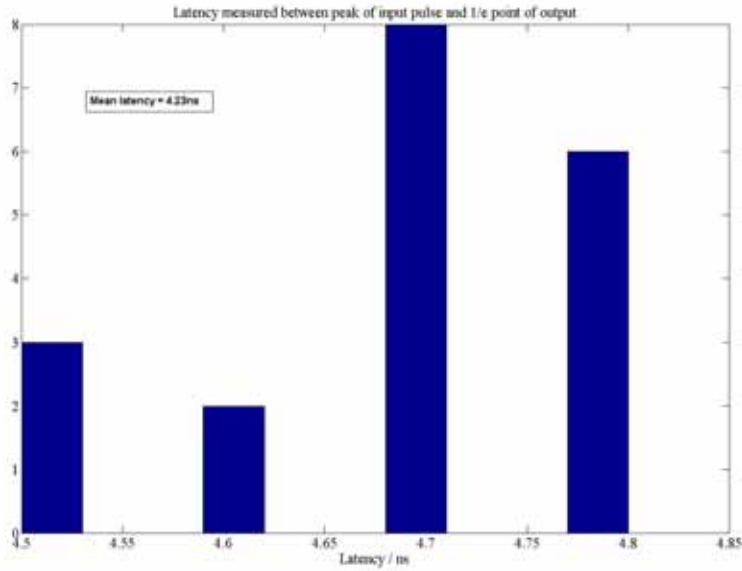


FONT3: BPM processor latency measurement

(single bunch, March 17 2005 beam tests)

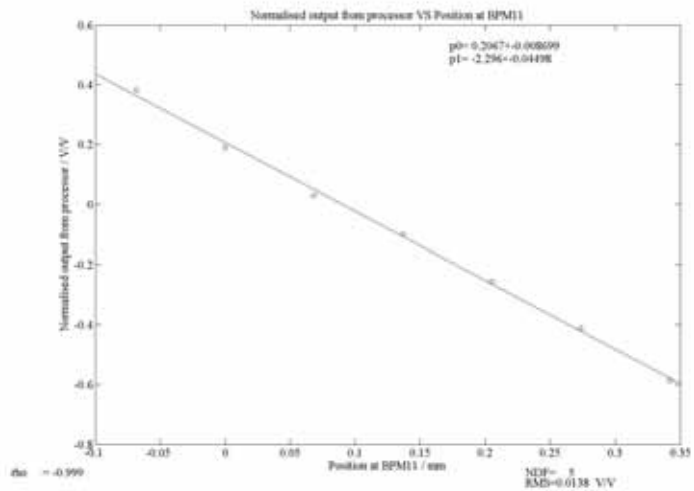


Distribution of latency:



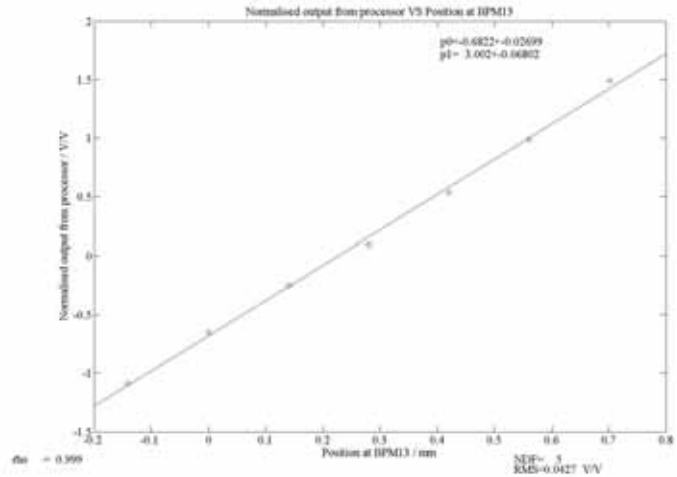
Latency 4.3 ns

FONT3: BPM scale calibration using correctors
(20-bunch data, March 17 2005 beam tests)

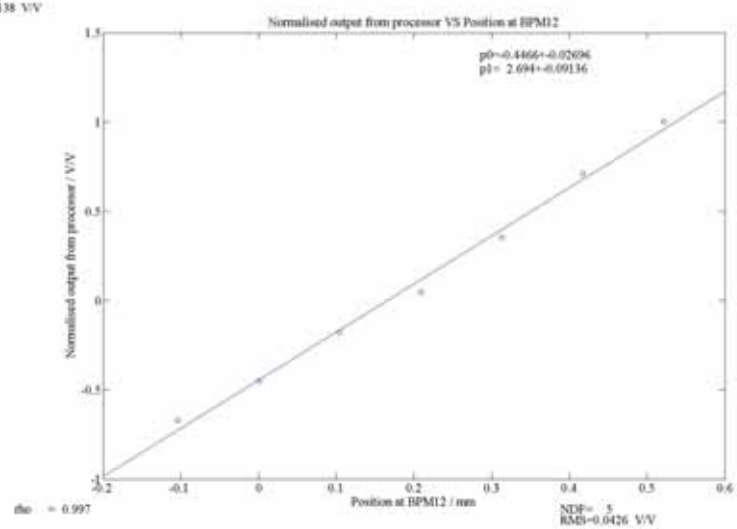


BPM11

BPM12



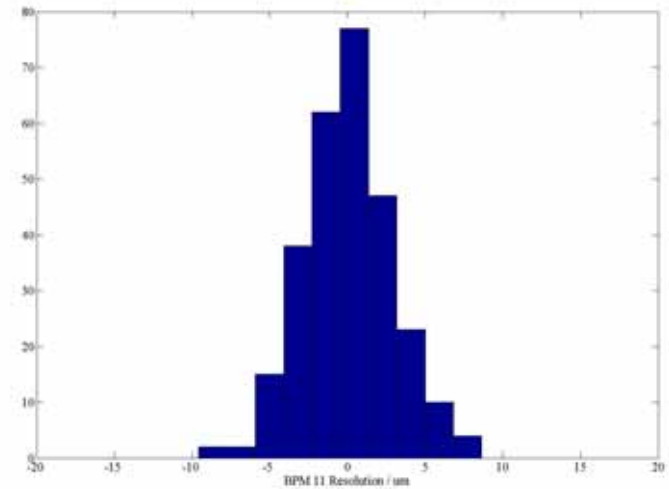
BPM13



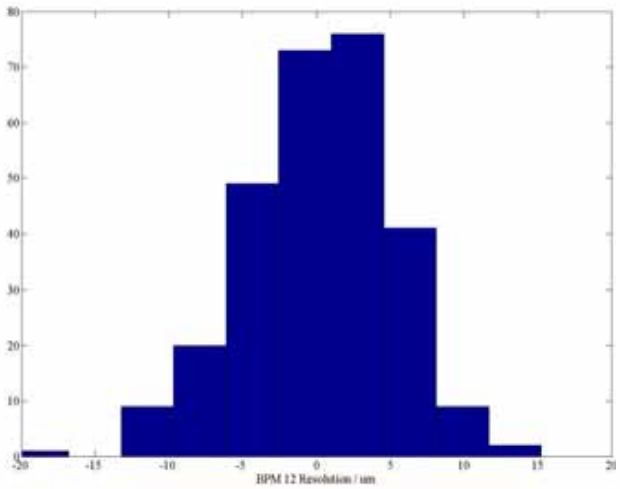
FONT3: BPM position resolution
(20-bunch data, March 17 2005 beam tests)

Distributions of residuals (240 beam pulses):

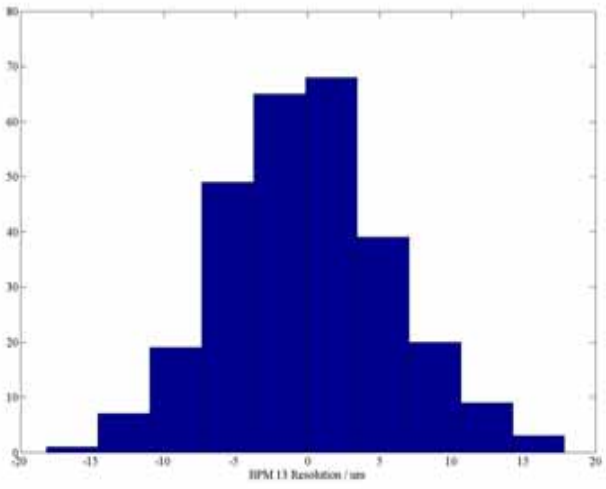
BPM11



BPM12



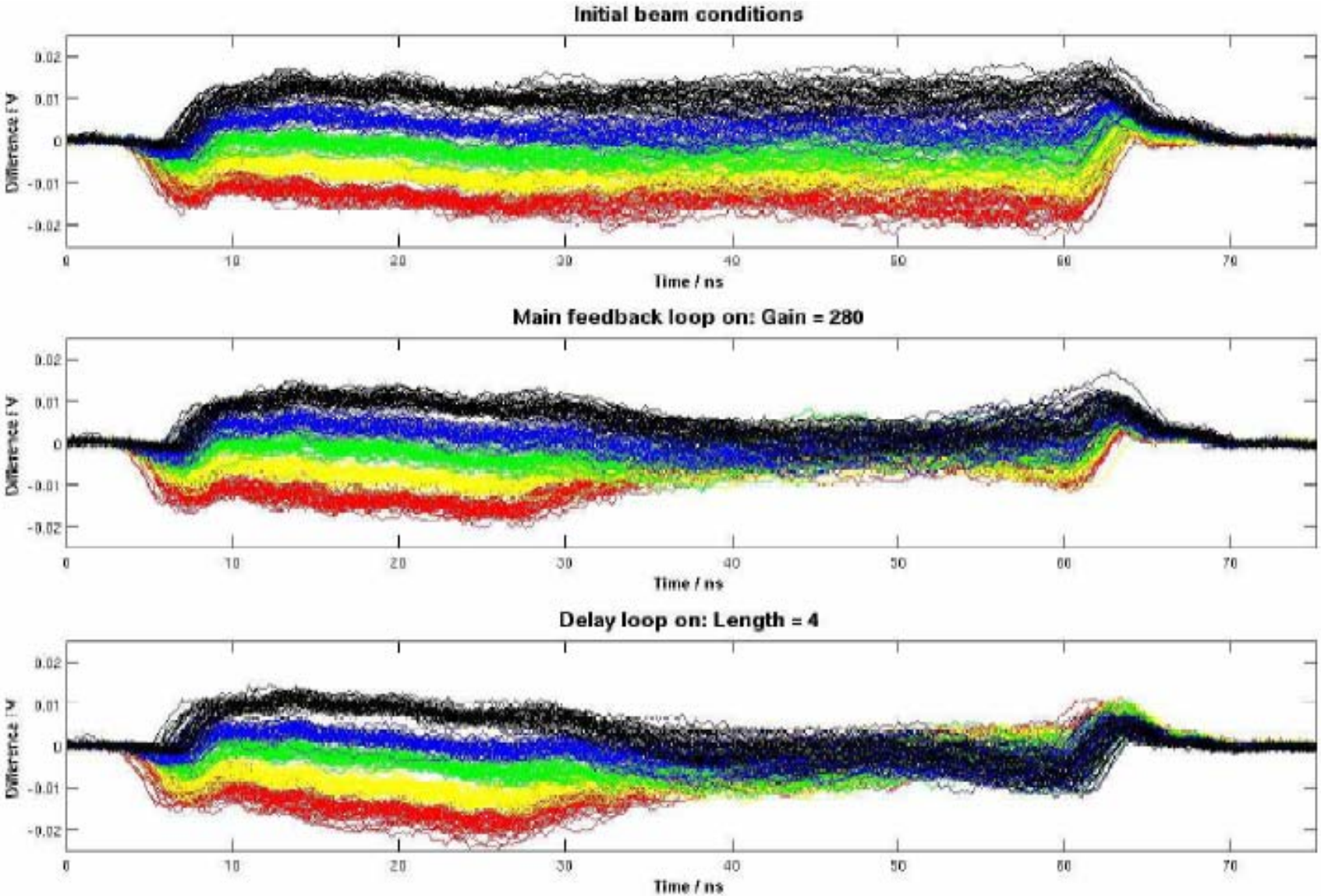
BPM13



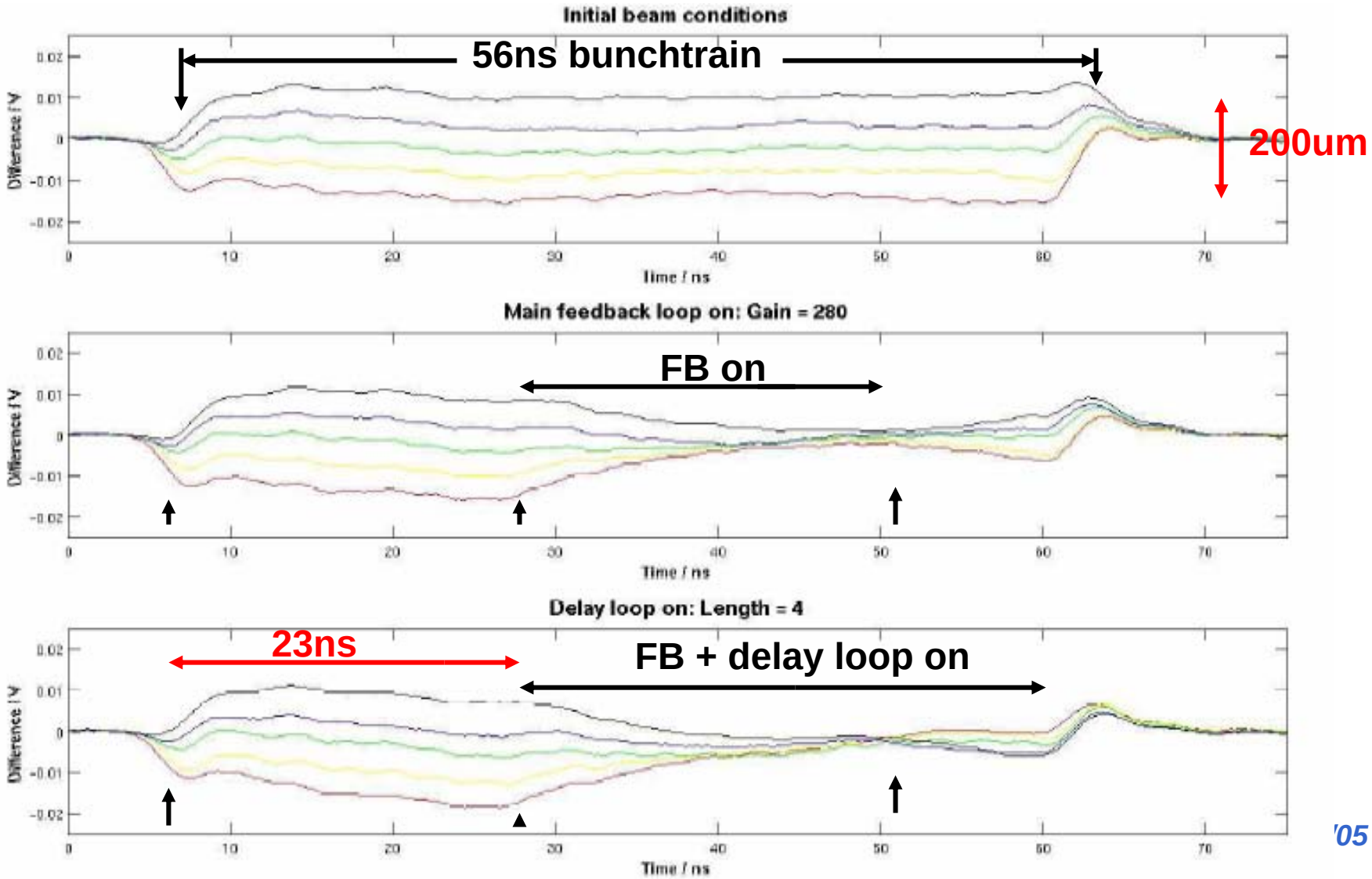
Resolution: 3 - 5 um

FONT3: Results (June 3 2005)

40 pulses per position setting



FONT3: Average over 40 Pulses



FONT3: Summary

Demonstrated feedback with delay loop

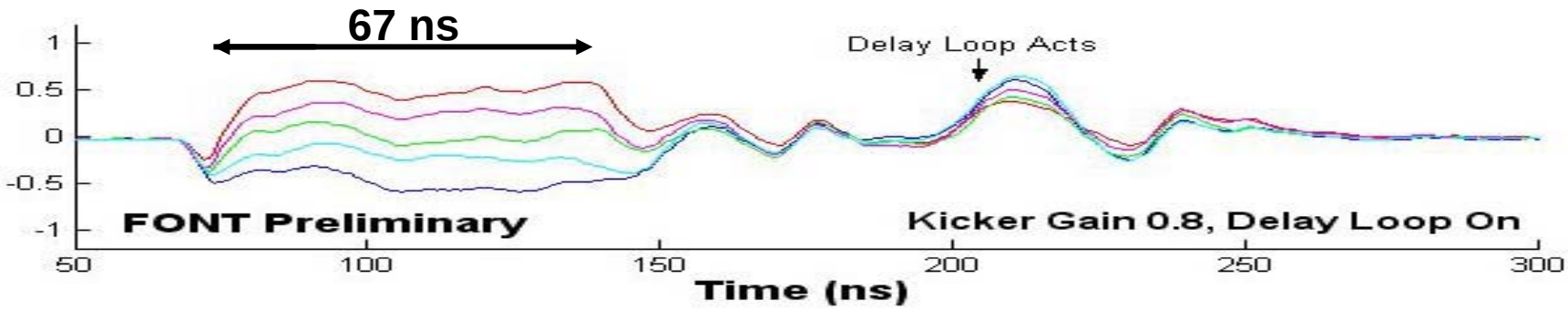
Ultra-fast system: total latency 23 ns

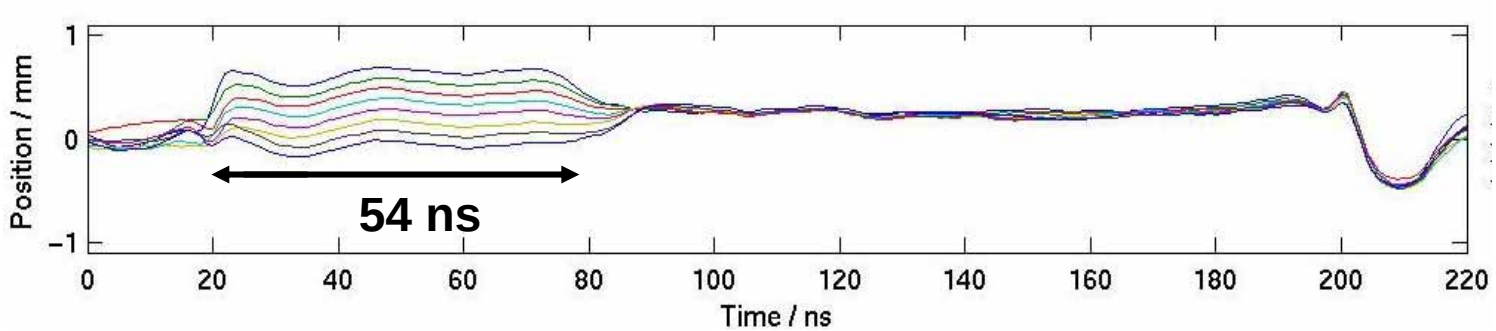
Varied main gain, delay loop length, delay loop gain

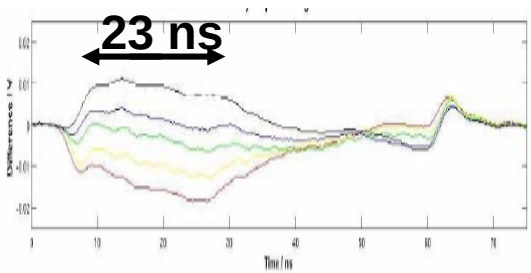
- **system behaves as expected**

Beam quality + limited time (6 shifts) did not allow detailed optimisation of system parameters

FONT1,2,3: Summary







Even fast enough for CLIC intra-train FB!

FONT4: Digital FB Processor Module (Dabiri Khah)

JTAG connector
JTAG circuit
RAM
Flash/ EEPROM
DAC
DAC
AOUT2
AOUT1
Serial connector
UART circuit
FPGA
ADC
ADC
ADC
ADC
Differential To single
Differential To single
Differential To single
Differential To single
AIN4
AIN3
AIN2
AIN1
USB connector
USB circuit
Clock circuit
5v
3.3v
2.5v
? v
Clk IN

Latency goal 100ns

FONT4: Prototype Digital Feedback System

ATF/(ATF2): 1.3 GeV beam, 3 bunches with spacing c. 150ns

FONT4 (2005-6):

- **modified FONT3 BPM front-end signal processor**
- **digital FB processor**
- **modified FONT2 solid-state amplifier: 300ns long o/p pulse**
- **FEATHER adjustable-gap kicker**

Aiming for first demonstration of FB w. ILC-like bunches:

- **latency 100ns (electronics)**
- **stabilisation of 3rd bunch at um level**

Possible first component tests at ATF December 2005/March 2006

5-Hz Integrated Feedback Simulations
(Linda Hendrickson)

Linac feedback distribution: 5 distributed loops per beam, each with 4 horizontal and 4 vertical dipole correctors, and 8 BPMs (X&Y). LJH simulations.

BDS feedback distribution: 1 BDS loop per beam, 9 BPMs and 9 dipole correctors, both horizontal and vertical. Based on NLC simulations by Seryi.

Linac and BDS feedbacks "Cascaded" system of 6 loops per beam: loops don't overcompensate beam perturbations, but can be independently disabled for operational convenience. SLC-style "single cascade" (each loop communicates beam information to single adjacent downstream loop).

Linac and BDS loops have exponential response of 36 5-Hz pulses.

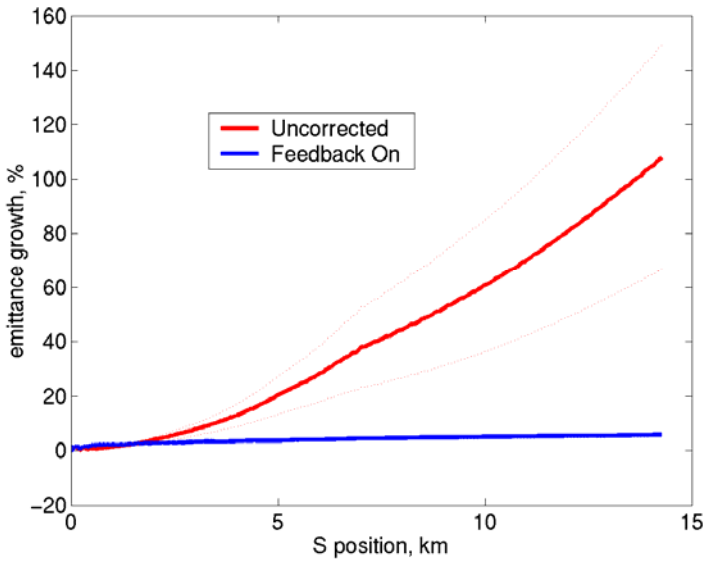
IP deflection (X&Y), not cascaded, exponential 6 pulses (like SLC).

Matlab/liar/dimad/guinea-pig platform. Upgraded liar/dimad for energy and current jitter, and dispersion measurements.

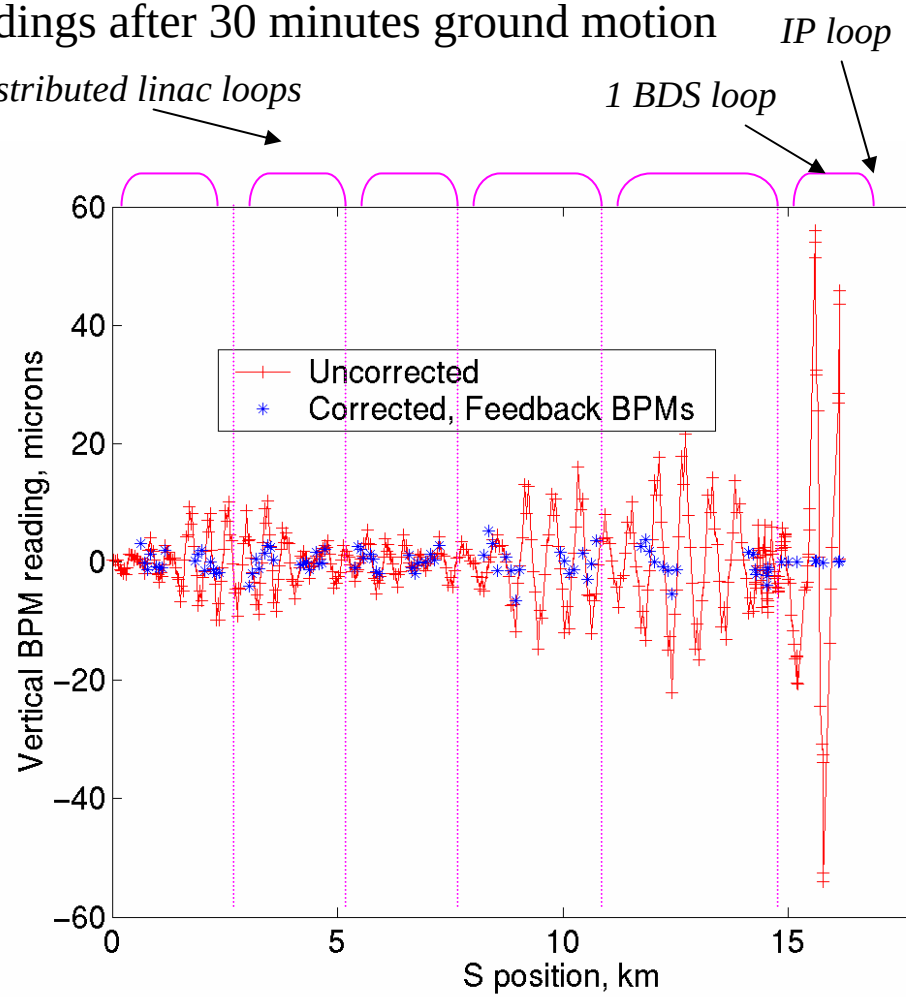
KEK-model ground motion (noisy site).

Feedback Simulations
(Linda Hendrickson)

Emittance growth in linac ~100% after 30 min "KEK" ground motion + jitter for 10 seeds, 6% with feedback (3% with feedback without jitter).

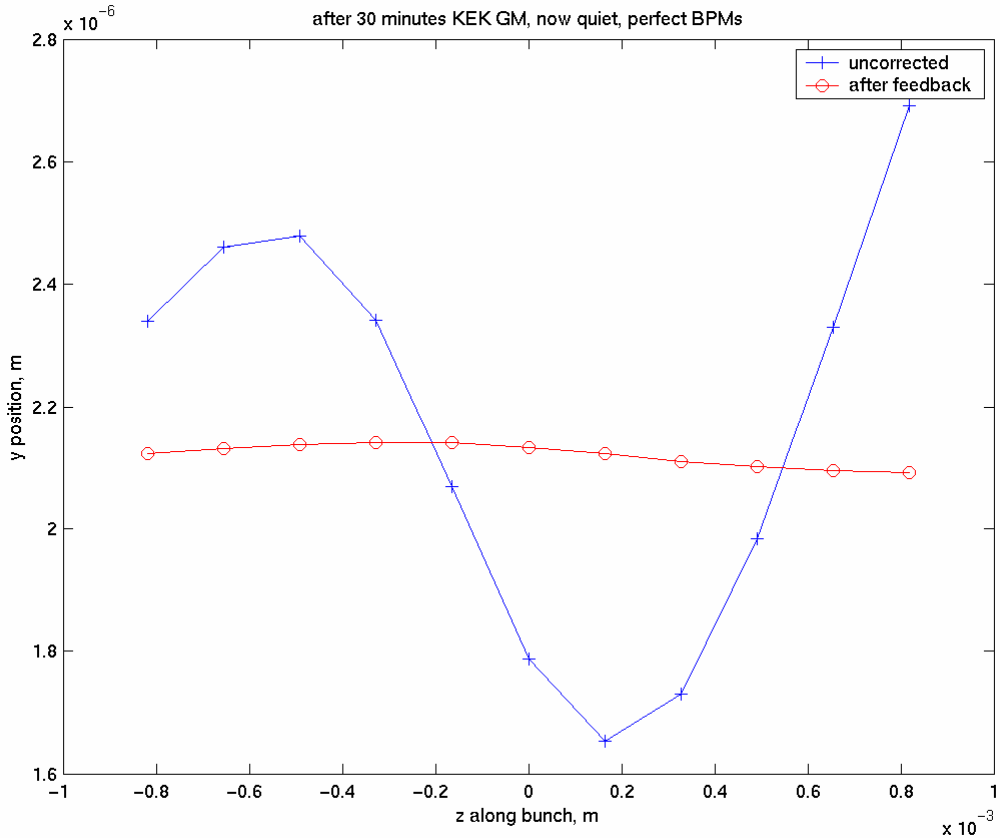


BPM readings after 30 minutes ground motion



Feedback Simulations
(Linda Hendrickson)

“Banana-bunch” shape is seen at end of LINAC after 30 minutes of “K” ground motion. Fixed with feedback.



Beamsize growth effects, with feedback (Hendrickson)

Single-beam studies of beamsize growth, with 5-hz feedback in LINAC and BDS.

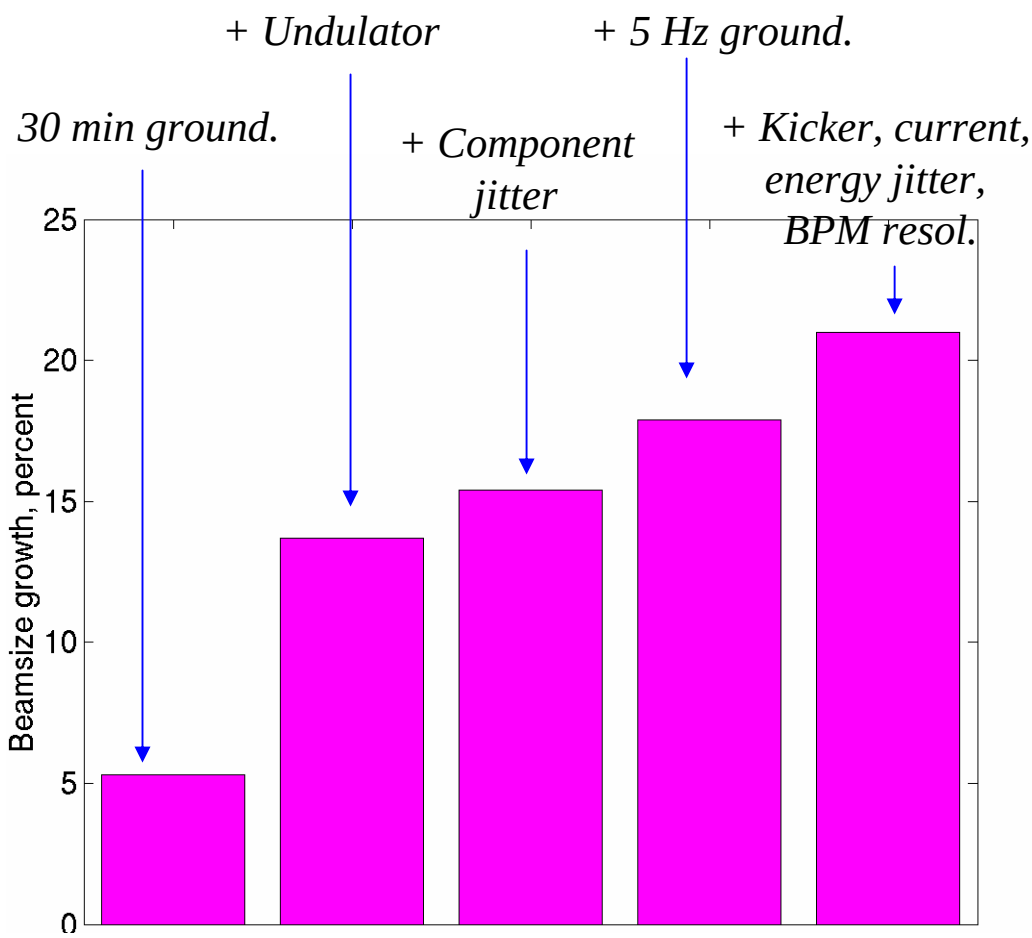
Perfect initially, add 30 minutes "KEK" ground motion", let feedback converge
-> 5% beamsize growth (380% without feedback).

Increase energy spread for undulator (.15% end of linac; this effect needs more study!)
-> 14%.

Add component jitter (25 nm BDS, 50 nm linac) -> 15%.

Add 5-Hz "KEK" ground motion -> 18%.

Add kicker jitter (.1 sigma), current jitter (5%), energy (.5% uncorrelated amplitude on each klys, 2 degrees uncorrelated phase on each klys, 0.5 degrees correlated phase on all klystrons, BPM resolution .1 um. -> 21%

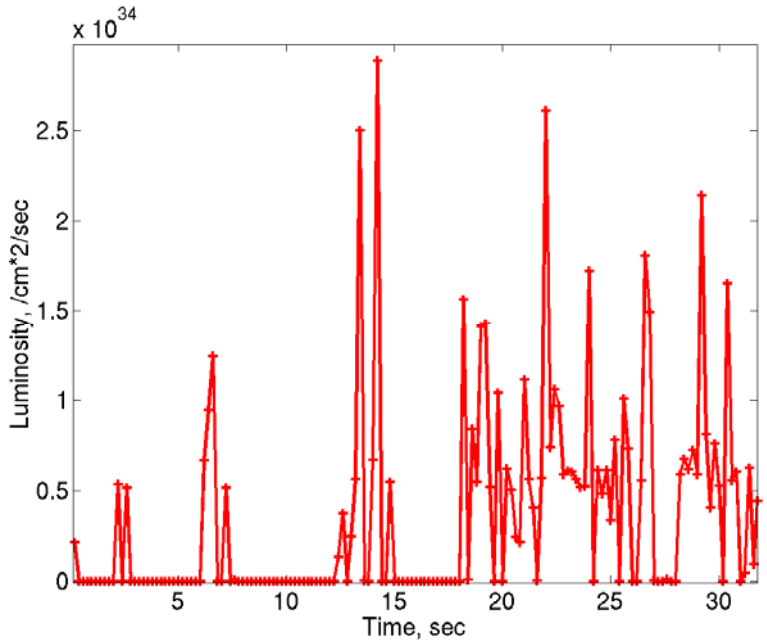


2-beam Integrated Feedback Simulations
(Linda Hendrickson)

2 beams, 5-Hz linac, BDS and IP deflection feedback. Perfect initially, feedback turned on after 30 minutes of "KEK" ground motion. 5 Hz ground motion, added component jitter, kicker, energy, current jitter.

No angle feedback, no intratrain feedback.

For the first ~20 seconds, IP feedback cannot keep up with large BDS steering changes. After 20 seconds, beams kept in collision but luminosity is poor (~20% in preliminary simulations, ~79% with perfect intratrain IP feedback).



International Fast FB Collaboration

- **FONT:**

  Queen Mary: Philip Burrows, Glen White, Glenn Christian,
  ***Hamid Dabiri Khah*, Tony Hartin, Stephen Molloy,**
  Christine Clarke, *Christina Swinson*

  Daresbury Lab: Alexander Kalinin, Roy Barlow, Mike Dufau

  Oxford: Colin Perry, Gerald Myatt

  SLAC: Joe Frisch, Tom Markiewicz, Marc Ross, Chris Adolphsen, Keith Jobe, Doug McCormick, Janice Nelson, Tonee Smith, Steve Smith, Andrei Seryi, Mark Woodley, Linda Hendrickson.

- **FEATHER:**

  KEK: Toshiaki Tauchi, Hitoshi Hayano

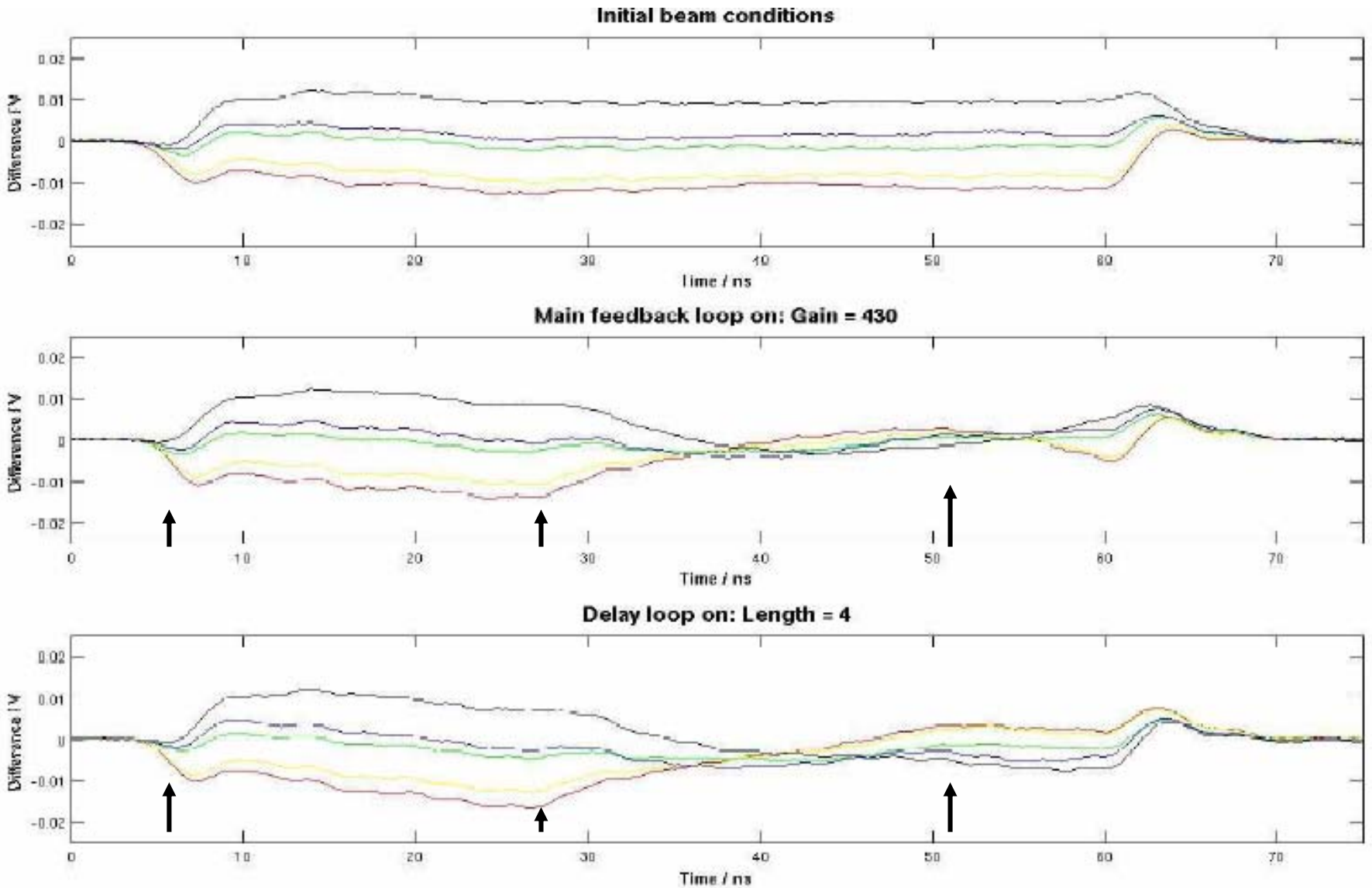
  Tokyo Met. University: Takayuki Sumiyoshi, Hiroaki Fujimoto

- **Simulations: Nick Walker (DESY), Daniel Schulte (CERN)**

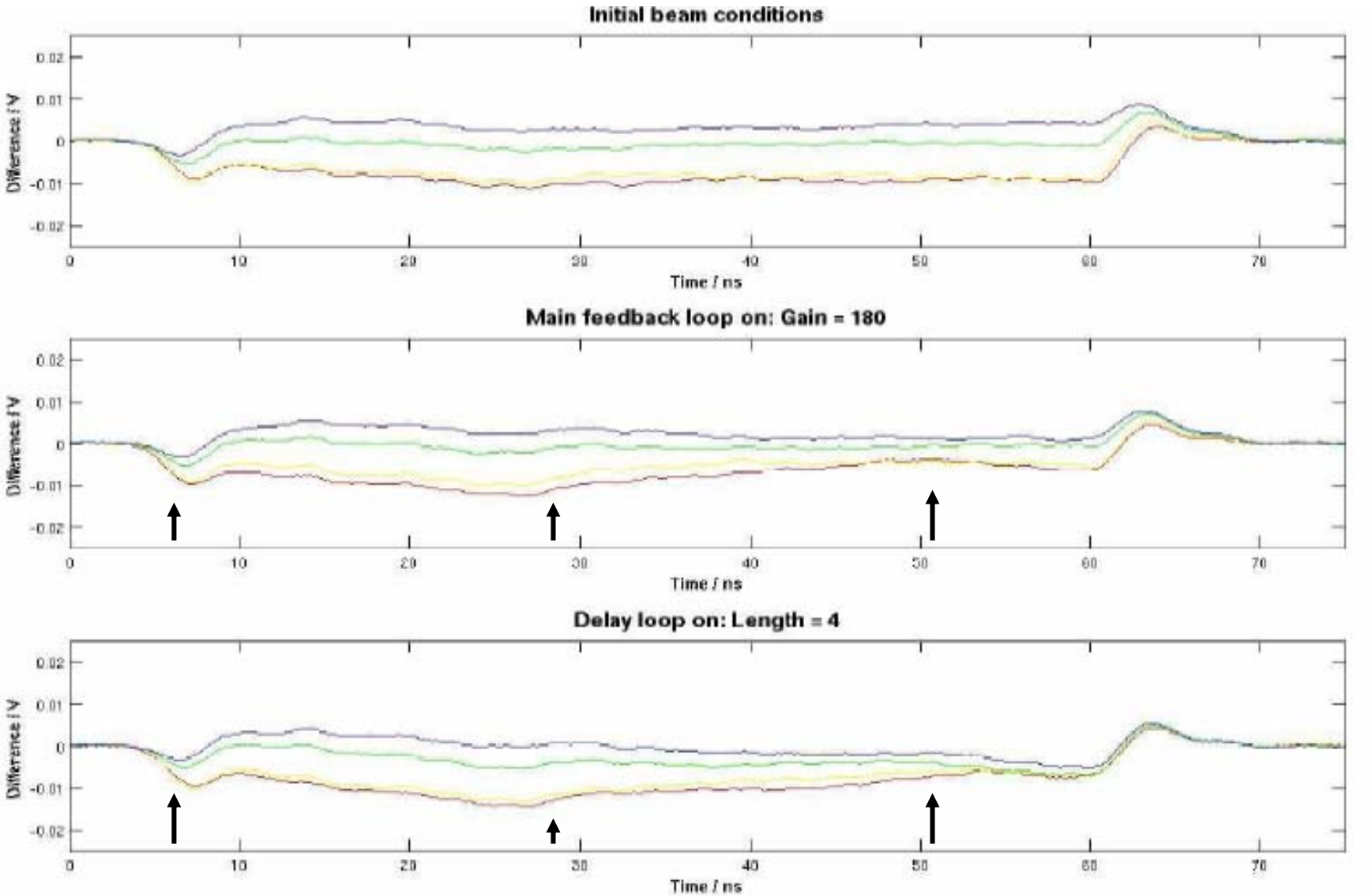
- **Eurotev (BDS, ILPS), ELAN (Instr, Bdyn), ILC WG4 (BDS)**

Spare slides follow

FONT3: Averaged results
(HIGH gain, nominal delay settings)

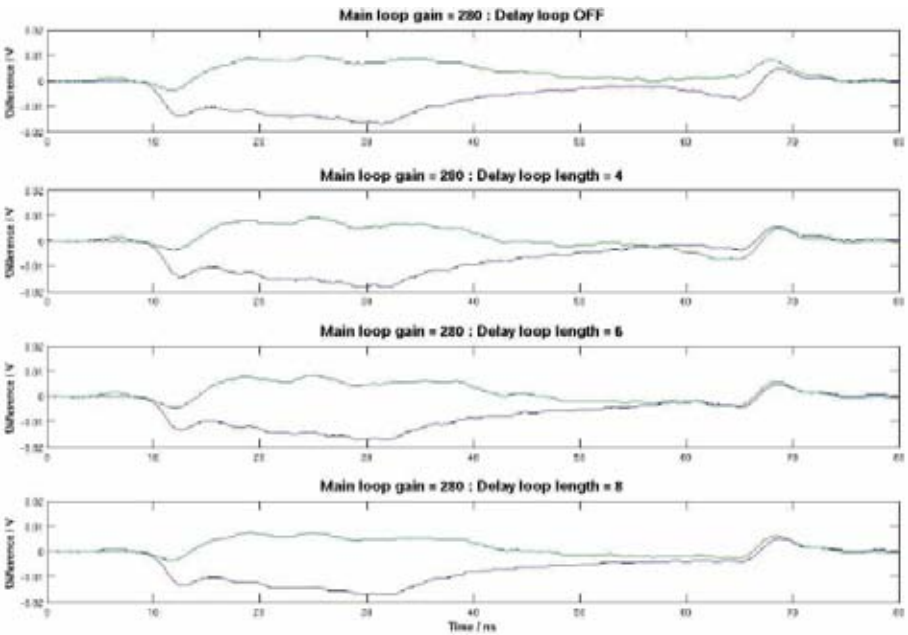


FONT3: Averaged results
(LOW gain, nominal delay settings)

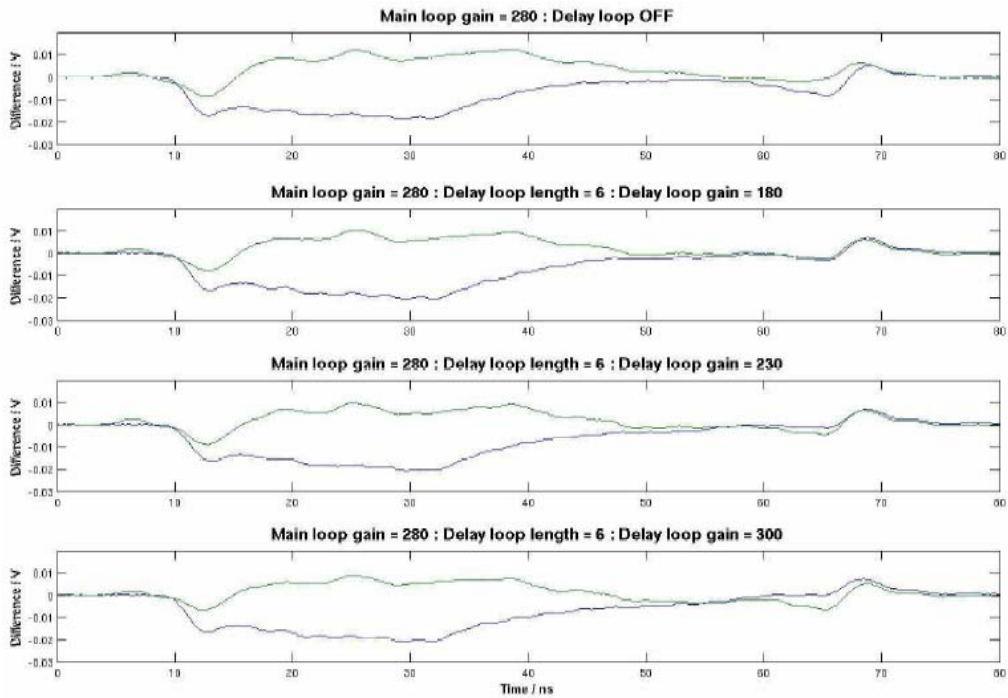


FONT3: Average results
(variation of delay-loop settings)

Delay loop length



Delay loop gain



Philip Burrows