The DEPFET for the ILC Vertex Detector

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Introduction

Reporting on work developed in collaboration between the MPI-Semiconductor laboratory and two German Universities

Detectors are designed produced and tested in own Semiconductor Laboratory with complete Silicon Technology processing line
capable of providing all DEPFET detectors for the ILC vertex detector

Small size prototype DEPFET pixel detectors have been produced and successfully tested

Prototype readout electronics with most features needed for ILC is existing

Overall arrangement of vertex detectors and module sizes follows the CCD proposal in the TESLA technical design report. A barrel + endcaps geometry will also be considered.

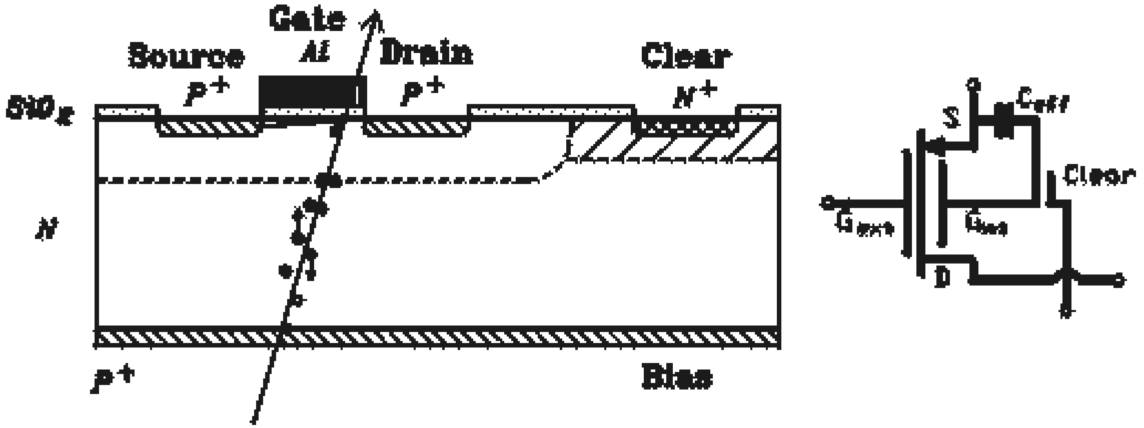
DEPFET concept dates back to 1985, verified soon after
leads to unique properties that make it ideal for pixel detectors

At present: parallel development of DEPFET pixel detectors for ILC and X-ray astronomy

Status of the ILC development will be presented

DEPFET concept

DEPFET structure and device symbol



Function principle

Field effect transistor on top of fully depleted bulk

All charge generated in fully depleted bulk

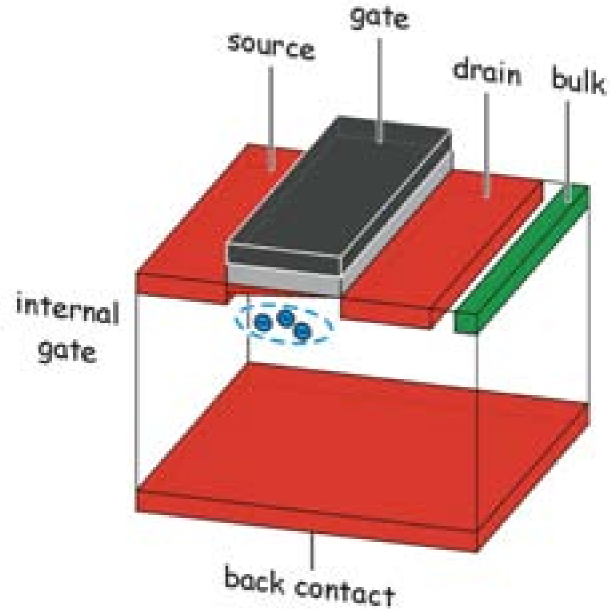
drifts into potential minimum underneath the transistor channel

steers the transistor current

Clearing by positive pulse on clear electrode

Combined function of sensor and amplifier

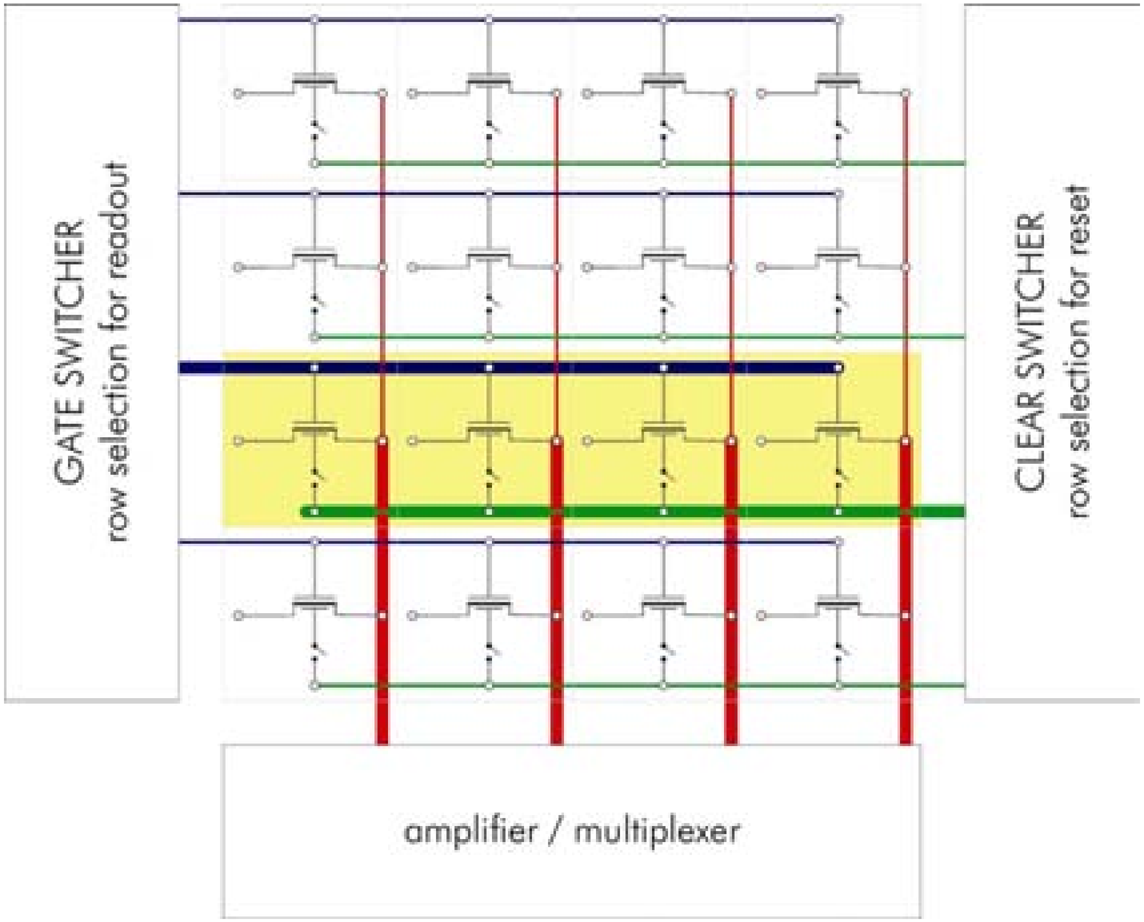
DEPFET concept



Properties

- Charge collection by drift mechanism
  over full wafer thickness
- low capacitance ► low noise
- Signal charge remains undisturbed by readout ► repeated readout
- Complete clearing of signal charge ► no reset noise
- Full sensitivity over whole bulk ► large signal for m.i.p.; X-ray sens.
- Thin radiation entrance window on backside ► X-ray sensitivity
- Charge collection also in turned off mode ► low power consumption
- Measurement at place of generation ► no charge transfer (loss) ►
  Operation over very large temperature range ► no cooling needed

DEPFET Pixel Detector Operation Mode

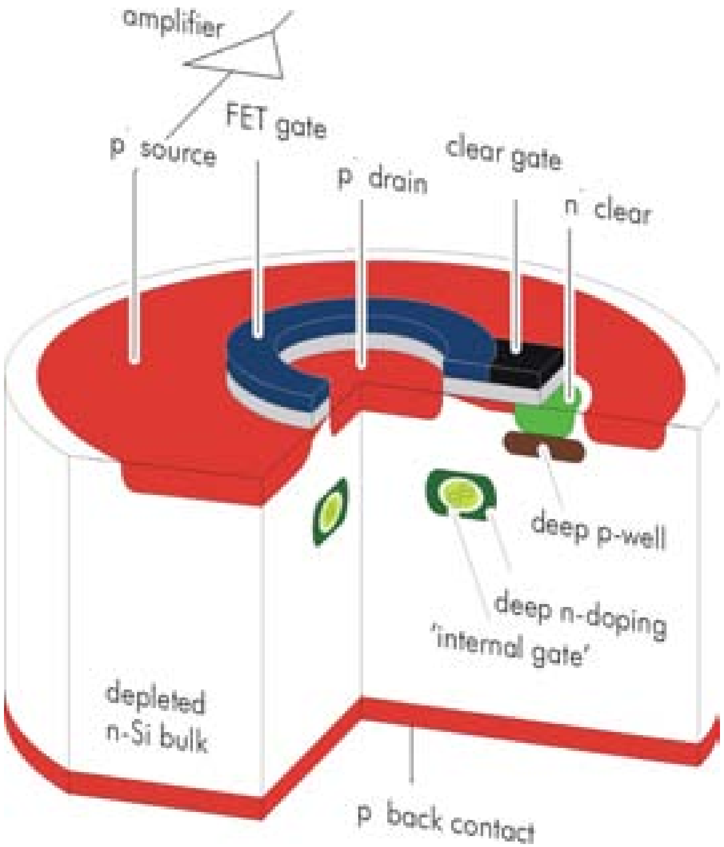


Large area covered with DEPFETS
Individual transistors or rows of transistors
Can be selected for readout
All other transistors are turned off
Those are still able to collect signal charge
Very low power consumption

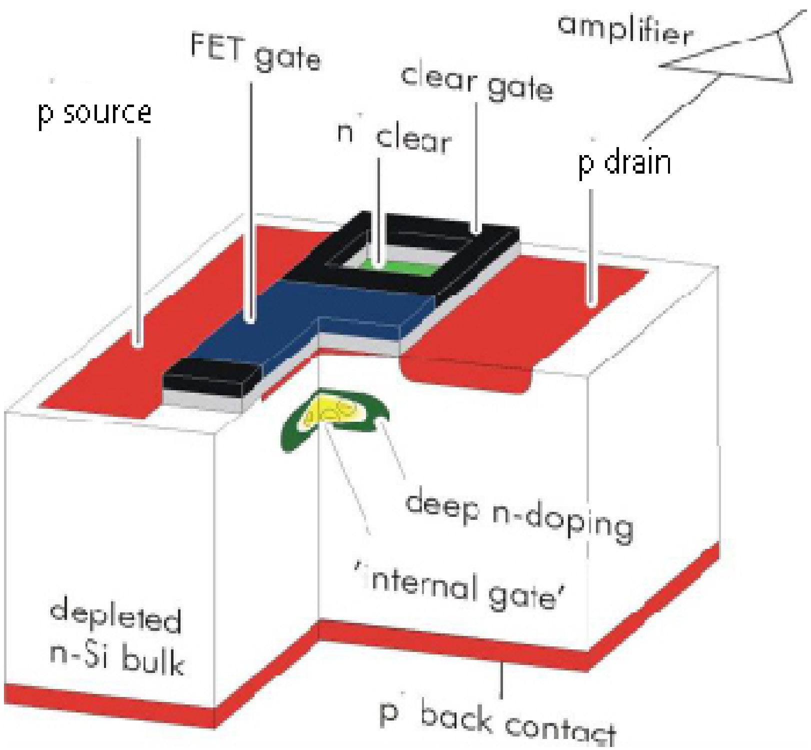
DEPFET pixel detector prototypes

Two projects on same wafer, two different geometries:

XEUS (future X-ray observatory):
Circular (enclosed) geometry
Source readout



Linear collider:
Rectangular geometry
Drain readout



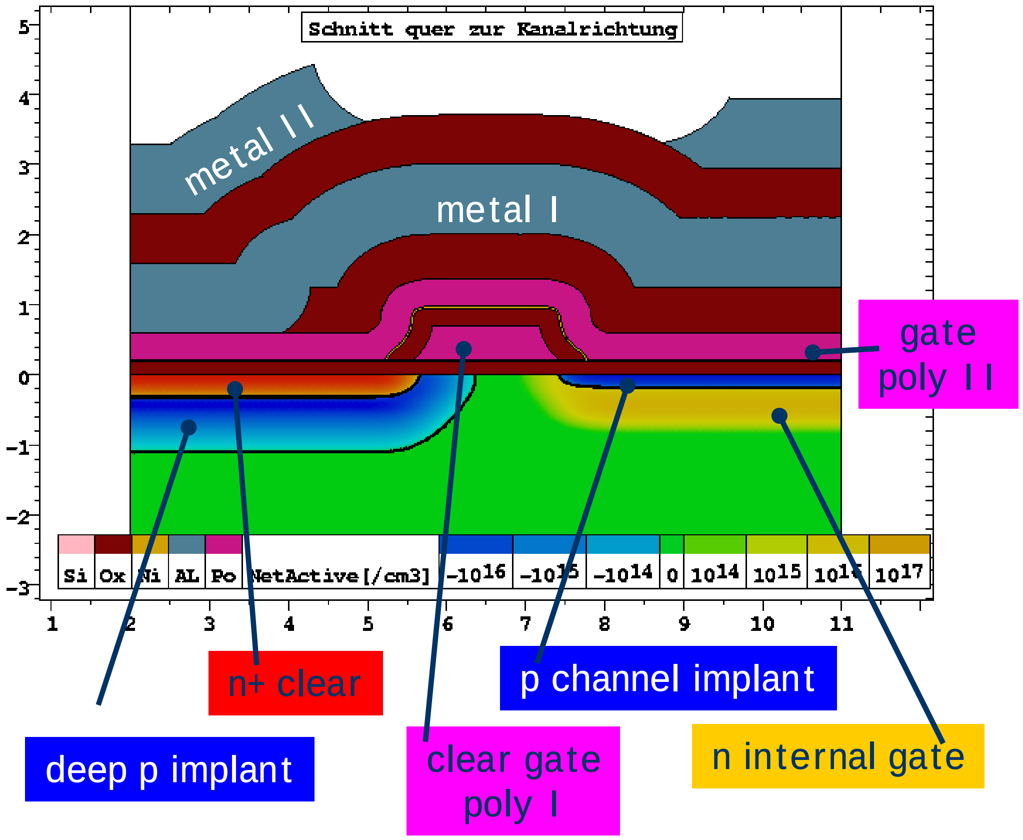
DEPFET Technology at MPI

Extendet technology:

Double metal

Double poly

cut perpendicular to channel (with clear)



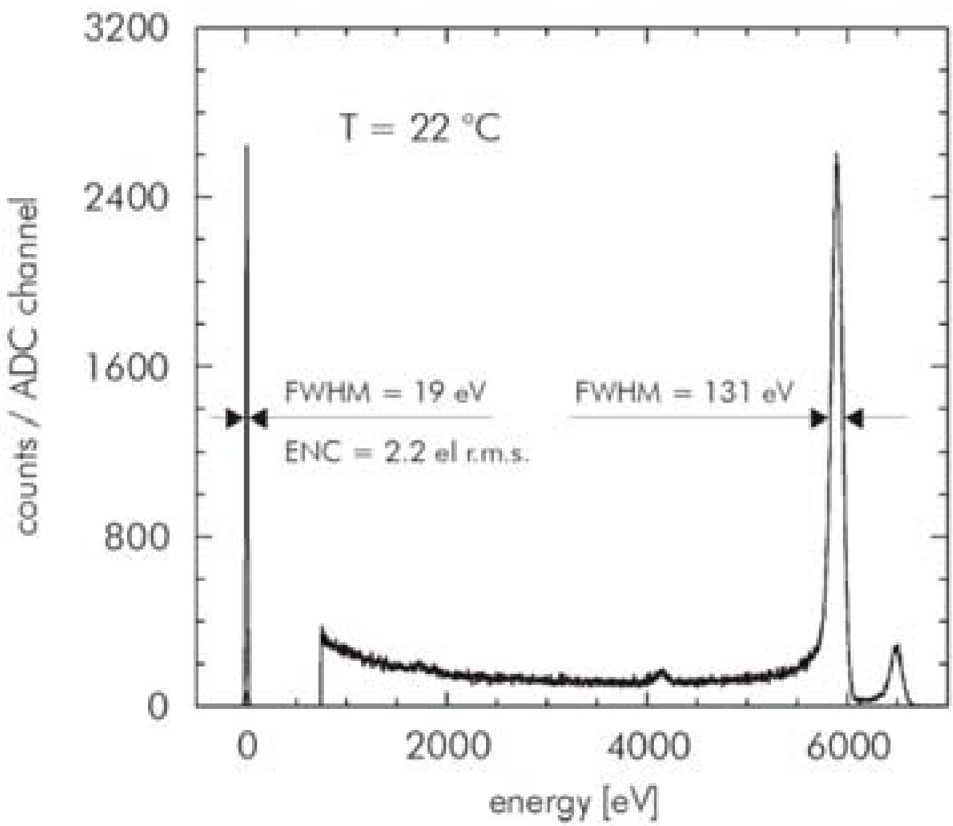
DEPFET noise

Fe55 spectrum measured with single circular (XEUS-type) DEPFET:

2.2 electrons rms

  at room temperature

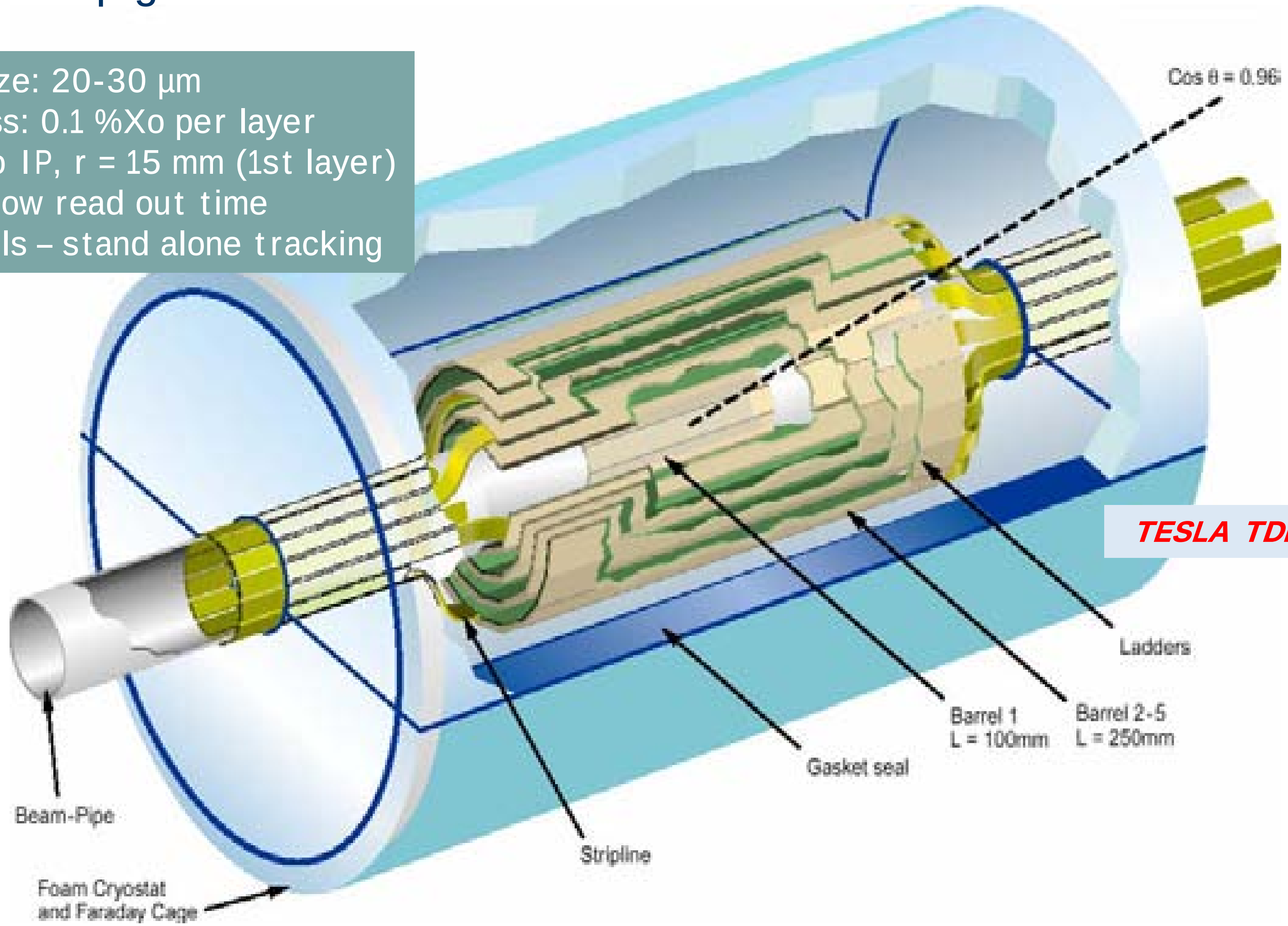
  with slow shaping



Vertex Detector

Layout so far follows the TESLA TDR concept
Barrel-endcap geometries will be considered

- pixel size: 20-30 µm
- low mass: 0.1 %Xo per layer
- close to IP, r = 15 mm (1st layer)
- 20 ns/row read out time
- 5 barrels – stand alone tracking

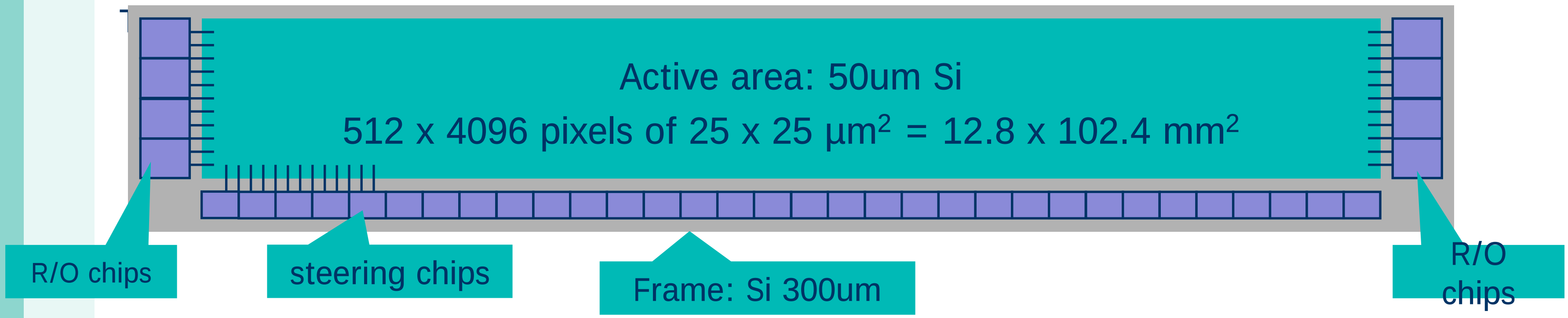


TESLA TDR Design

1st layer module: 100x13 mm², 2nd-5th layer : 125x22 mm² ➔ ∑120 modules

ILC DEPFET Module (Layer 1)

Modules have active area ~**13 x 100 mm²**



Rigid self supporting structure of single material
Avoids thermal stress and distortions

Electronic chips thinned and bump bonded to frame

Possible Geometry of Layer 1

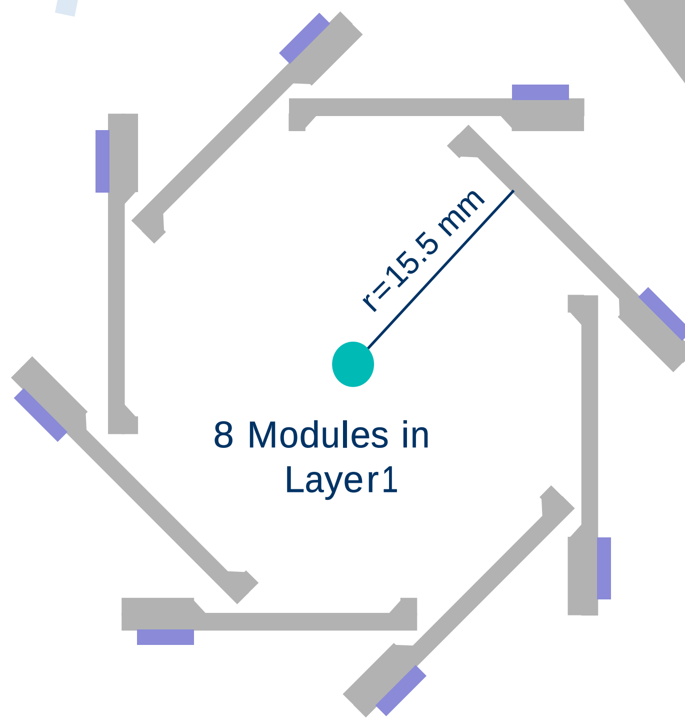
‘Holes’ in frame can save material

Chips are thinned to 50 µm, connection via bump bonding

Thinned sensor (50 µm) in active area

Thick support frame (~300 µm)

Cross section of a module



Estimation of material budget:

pixel area:	13x100 mm^2, 50µm:	0.05% X_0
steering chips:	2x100 mm^2, 50µm:	0.01% X_0
frame w. holes:	4x100 mm^2, 50% of 300µm:	0.05% X_0
total:		**0.11% X_0**

Thinning technology

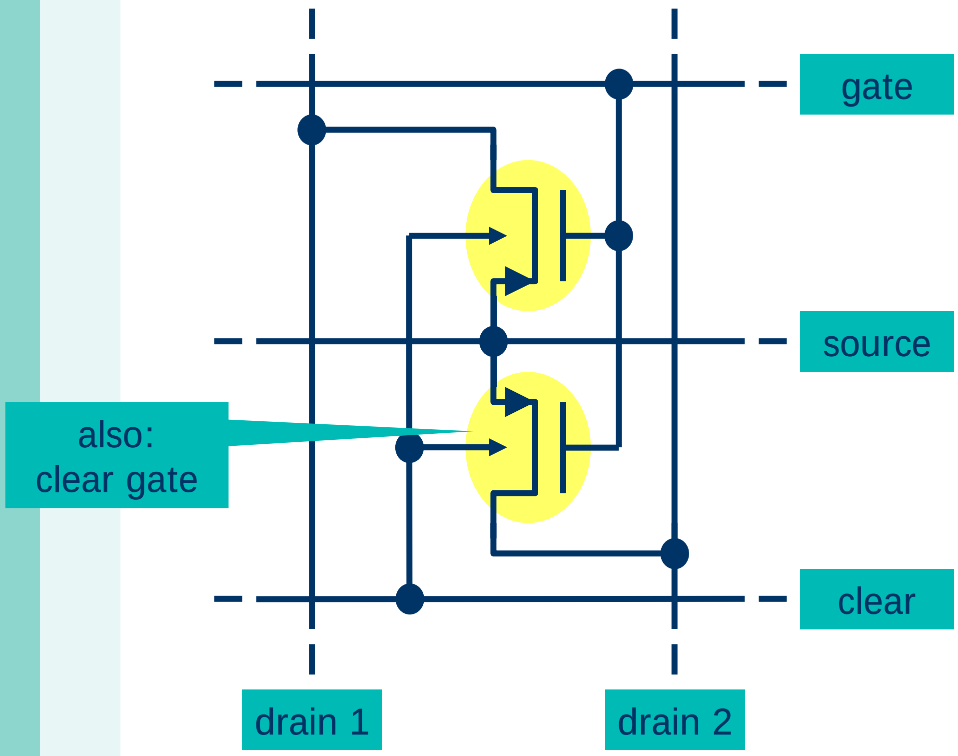
Already presented

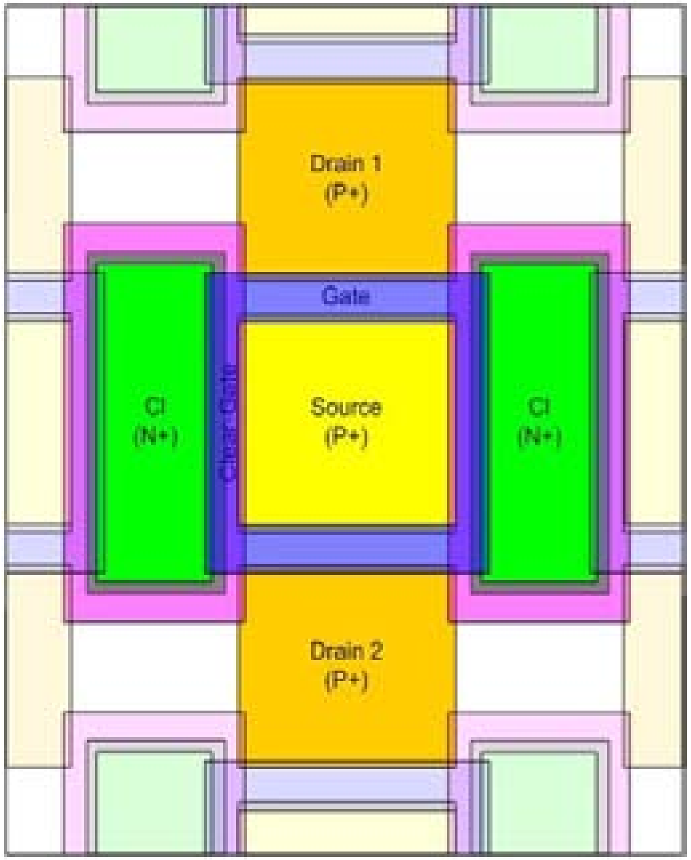
in VTX subgroup 2 on thursday

Sensor Design: MOS Devices

PMOS type DEPFETs

Double pixel cells with
with common source and clear
for readout of two rows at a time





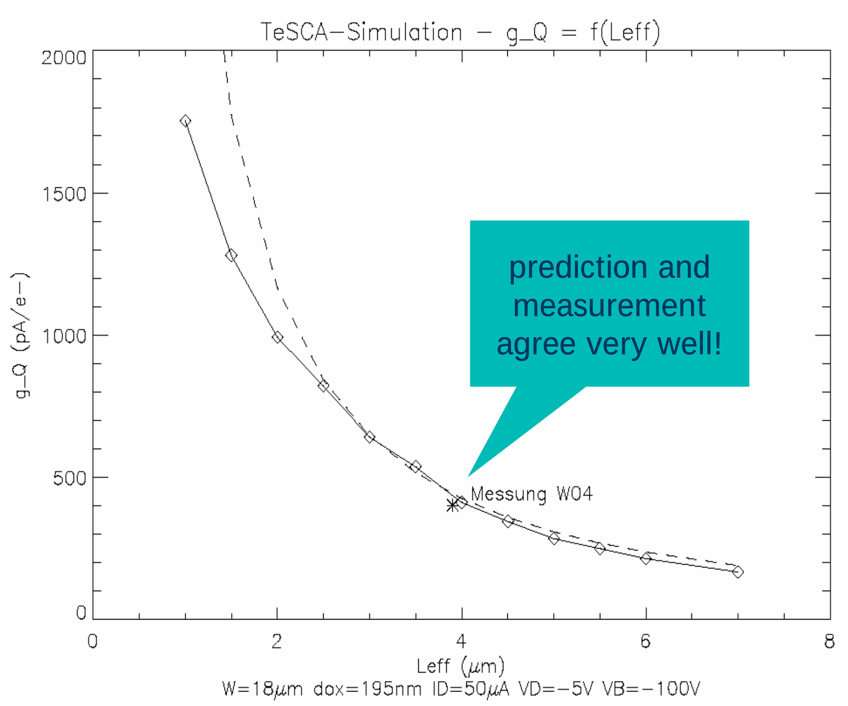
Sensor Simulations

Design relies heavily on device simulations: 2D TeSCA and 3D Poseidon

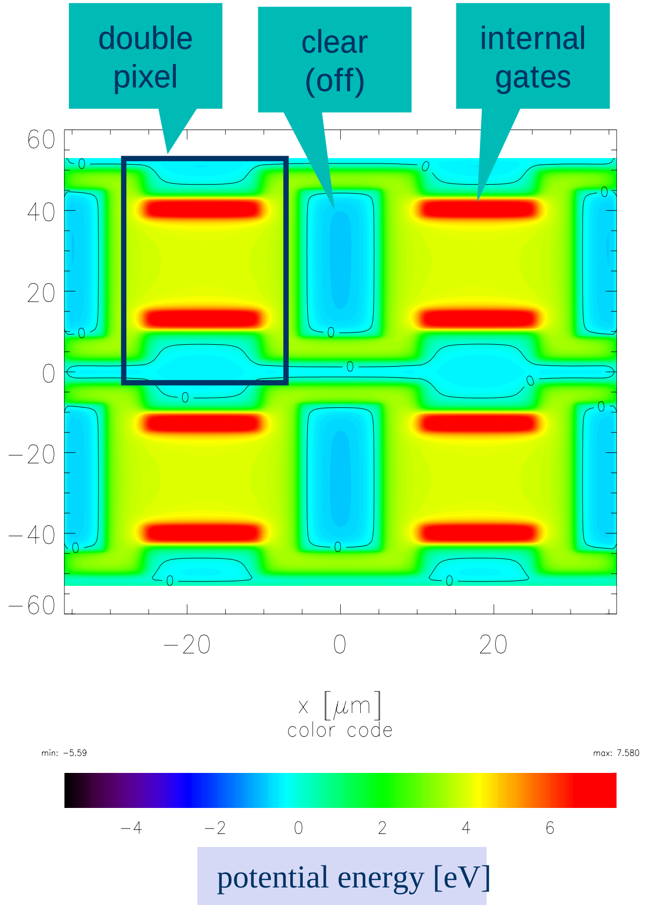
2D simulation of current response to signal charge as function of channel length

Device behavior can be predicted accurately.

Important for successful new designs!



charge gain g_q for varying gate length

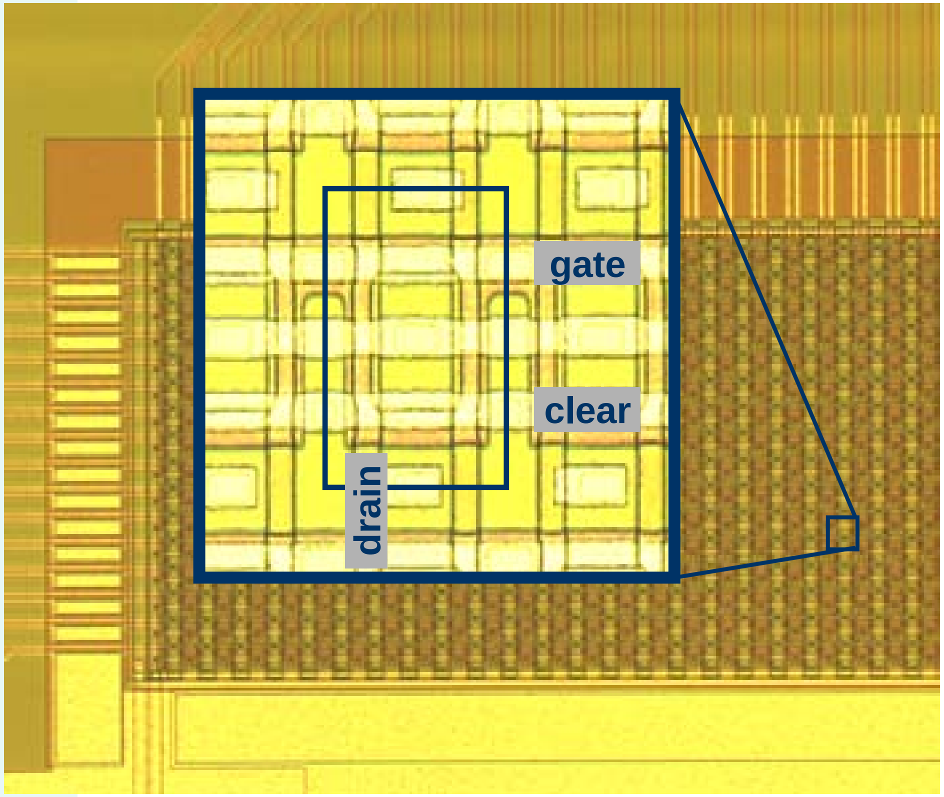


Potential distribution in 1μm depth in charge collection mode

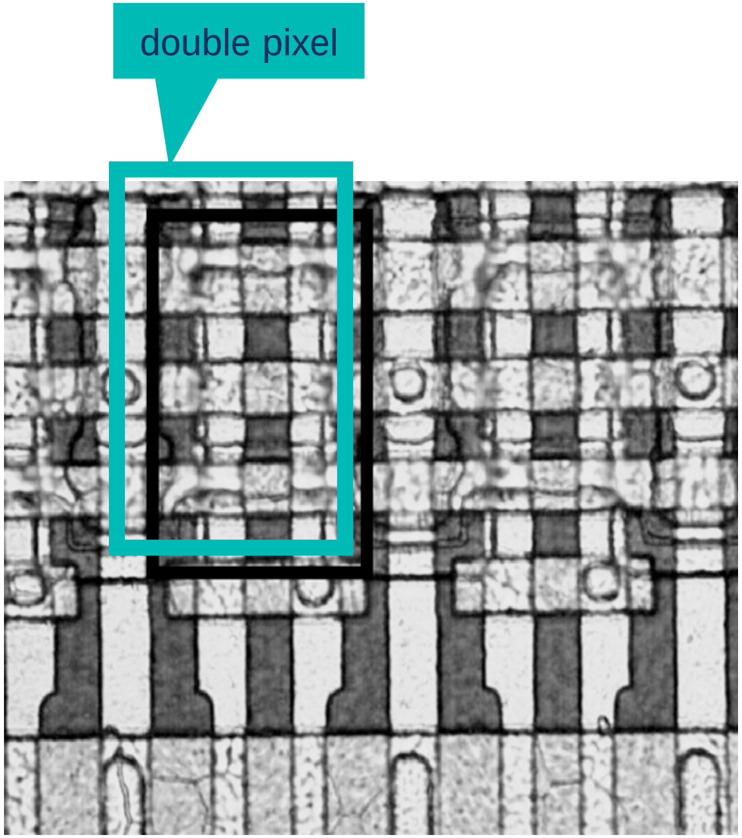
Prototype matrix production

A sensor-compatible technology with **2 poly and 2 metal layers** has been developed at HLL

These are required for large matrix designs

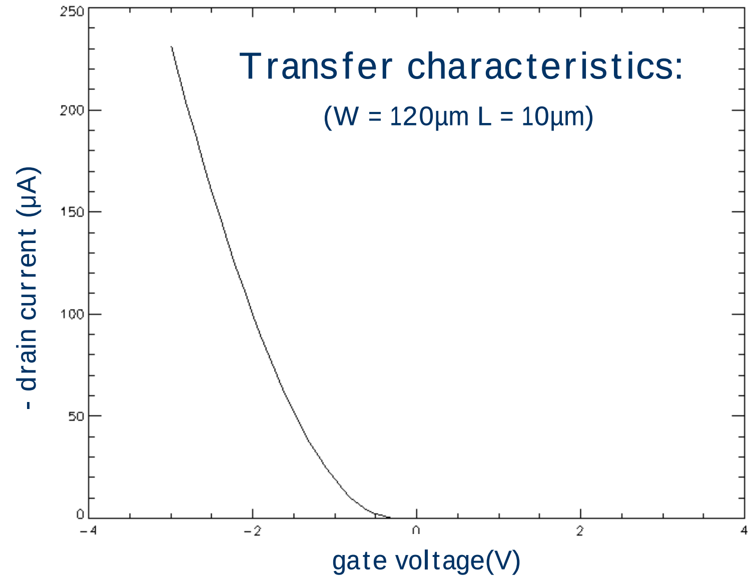


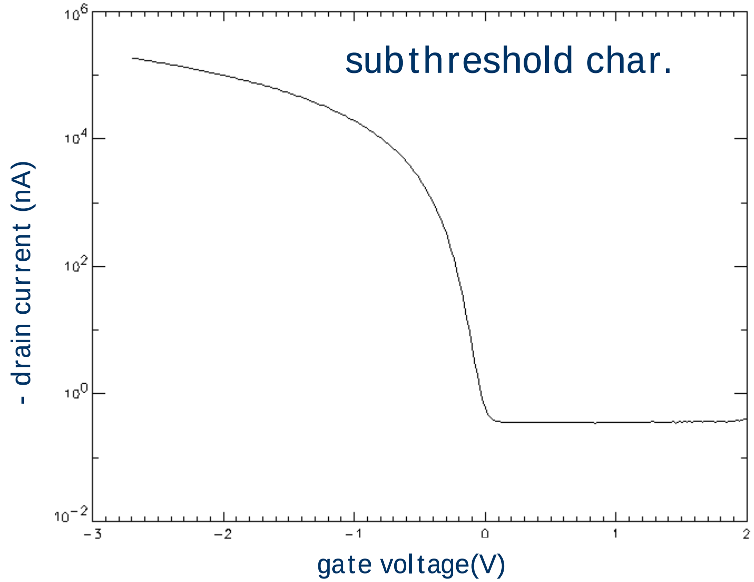
16x128 test matrix, double pixel cell 33 x 47 μm^2

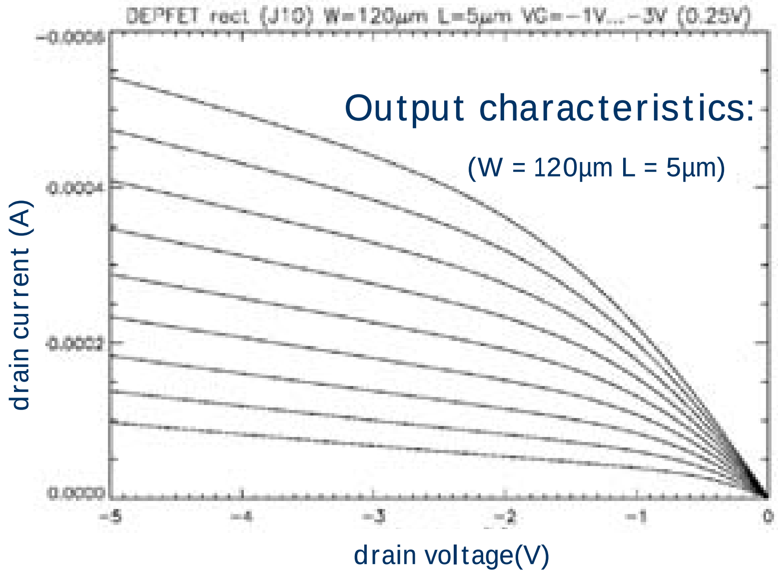


double metal matrix

DEPFET Basic Parameters







- ✓$V_{th} \approx 0V$
- ✓subthreshold slope ≈ 80mV/dec
- ✓Transistors can completely be turned off
- ✓all basic parameters agree with simulations

Radiation hardness

Threshold shifts due to oxide damage could have been a serious problem

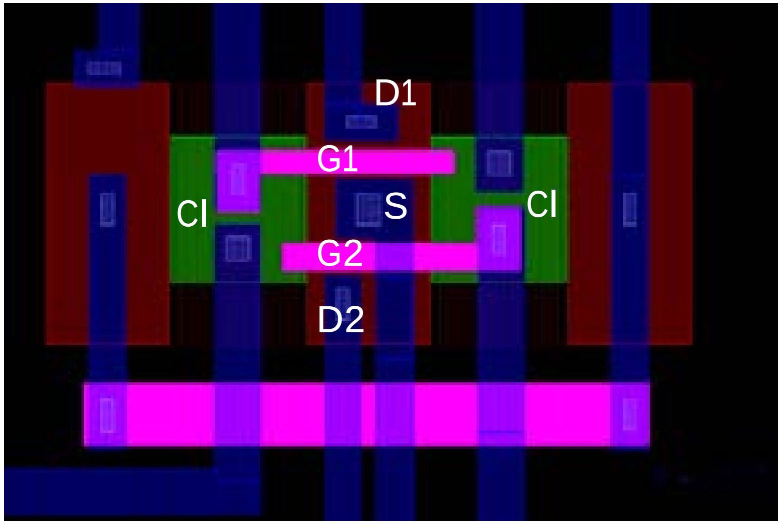
Irradiation tests with Co60 up to 1 Mrad and with X-rays demonstated that this is not the case

The moderate threshold shift observed can be compensated by a change in external gate voltage

Excellent spectroscopic properties after irradiation

Irradiated Devices - Overview

PXD4-2:	L= 6 µm	A2-1[1], B2-1[1], D2-1[2]
	L= 7 µm	A2-2[1], B2-2[1], D2-2[2]
PXD4-2:	L=10 µm	T10-1[1]
	L=20 µm	T20-1[1]
PXD4-1:	L=60 µm	T60-1[3], T60-2[3], T60-3[3]
PXD4-3:	L=5 µm	T5-1*



Bias during irradiaton:

1: empty int. gate, in „off“ state, V_{GS}= 5V, V_{Drain}=-5V → $E_{ox} \approx 0$
2: empty int. gate, in „on“ state, V_{GS}=-5V, V_{Drain}=-5V → $E_{ox} \approx$ -250kV/cm
3: all terminals at 0V

NB: only one row active at a time in normal matrix operation!
for a 512x1024 matrix → $T_{off}/T_{on} \approx 1000$!

→ measure threshold voltage (quadratic extrapolation if $I_D(V_G)$ to I_D=0) as a function of TID

all measurements with V_{bulk}=10V..12V, $V_{cleargate}$=5V .. 12V → “empty” internal Gate

Irradiation Facilities

GSF – National Research Center for Environment and Health, Munich

^{60}Co (1.17 MeV and 1.33 MeV)

CaliFa Teststand at MPI HLL

X-Ray tube with Mo target at 30kV

bremsstrahlung with peak at 17.44 keV

Dosimetry

Ionization Chamber, provided and calibrated by GSF staff

(M. Panzer, GSF)

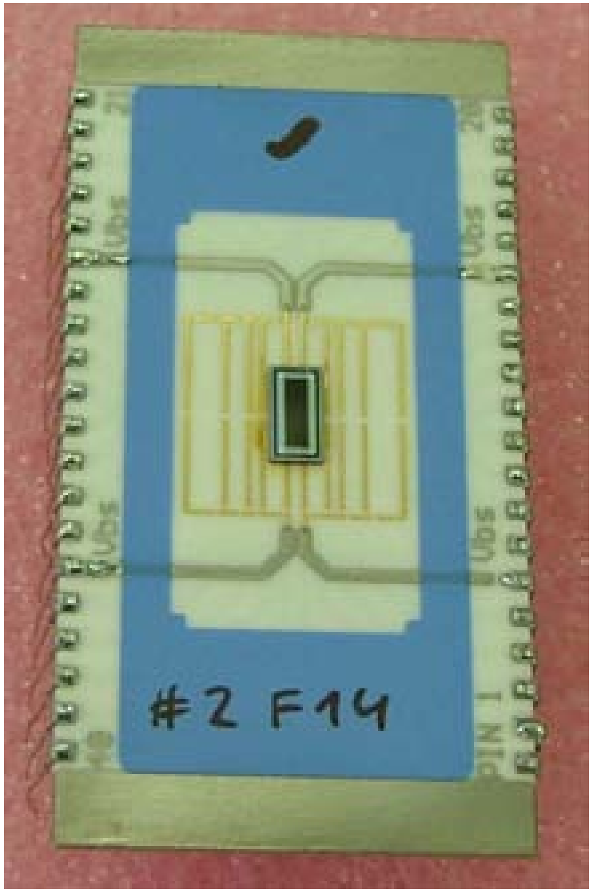
Dose rate: ≈ 20 krad(SiO_2)/h

Intergrated Spectrum with known absorption coeff. of SiO_2

(A. Pahlke, HLL)

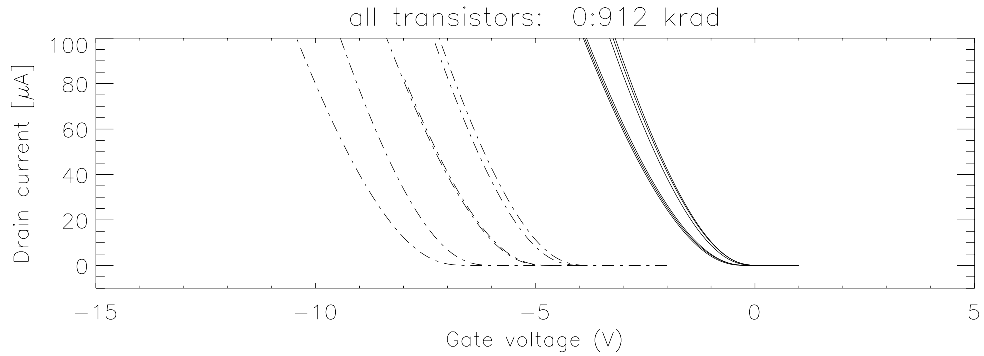
Dose rate: ≈9 krad(SiO_2)/h

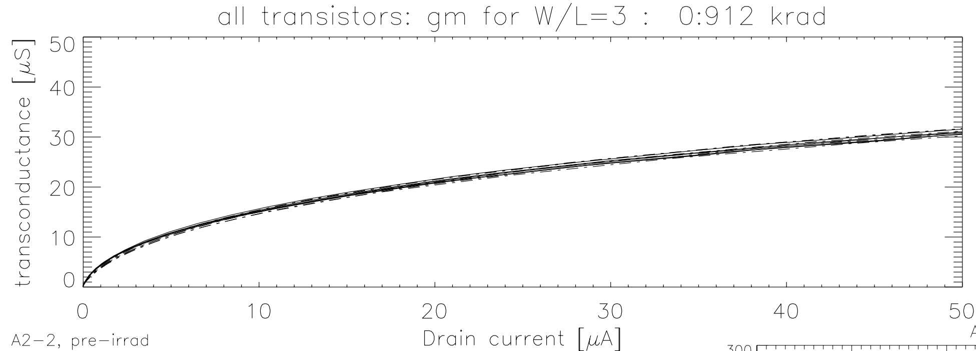
Before... and ... After



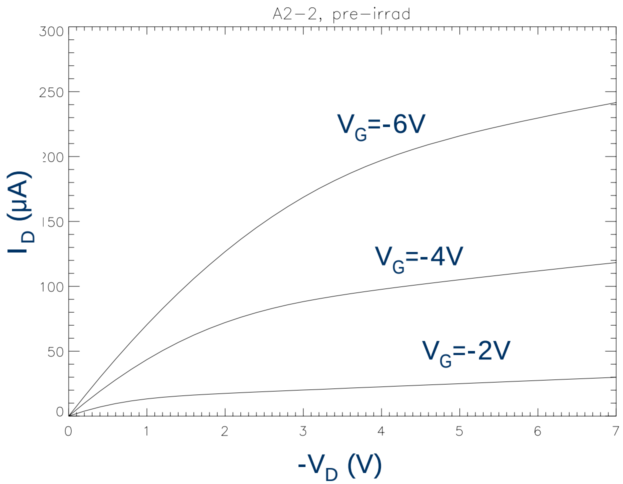
Ceramic base board after 912 krad(Si)
of 60Co Gammas

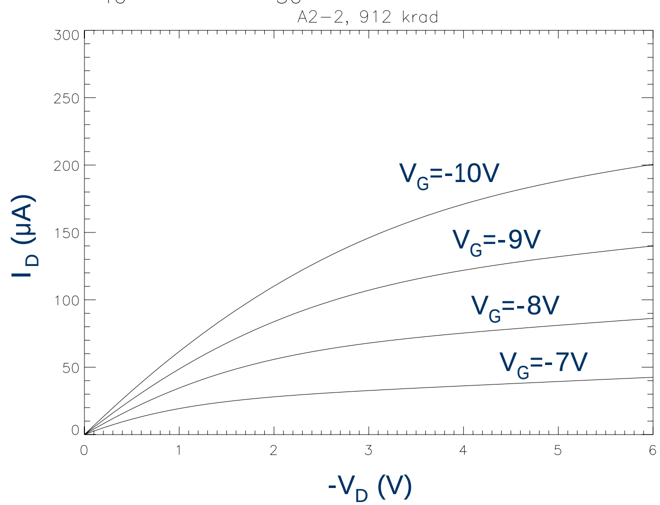
Basic Characteristics - pre and post-irradiation



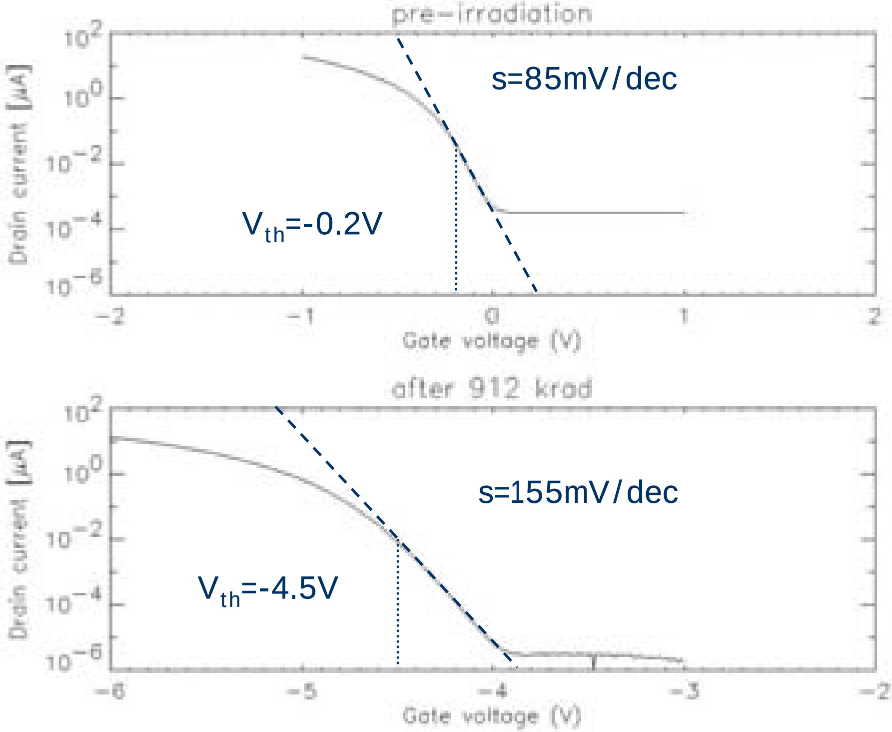


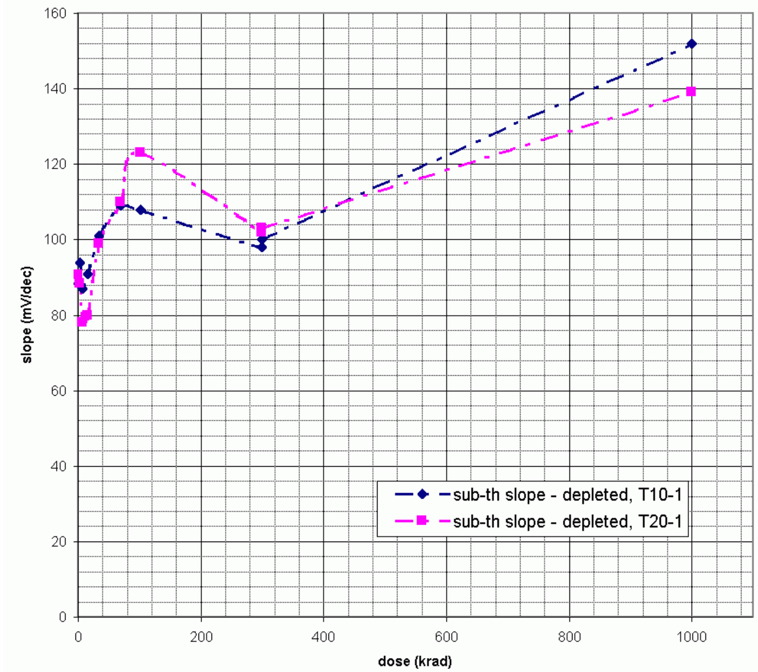
$$g_q = \frac{dI}{dQ} = \frac{g_m}{C_{ox}}$$





Subtreshold slope → interface traps





$$N_{it} = \frac{C_{ox}}{kT} \cdot \ln(10) \cdot (s_{D2} - s_{D1})$$

300 krad	:	$N_{it} \approx 2 \cdot 10^{11}$ cm^{-2}
1 Mrad	:	$N_{it} \approx 7 \cdot 10^{11}$ cm^{-2}

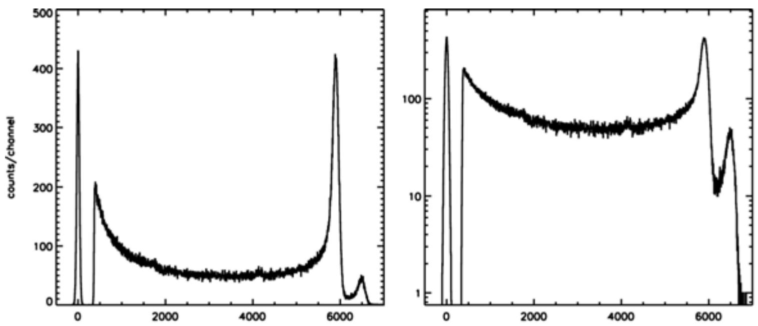
Literature:
after irradiation (1Mrad) of 200 nm oxide:
$N_{it} \approx 10^{13}$ cm^{-2}

Noise after 1 Mrad Co60 irradiation

Single pixel test structure
irradiated with 913krad Co60

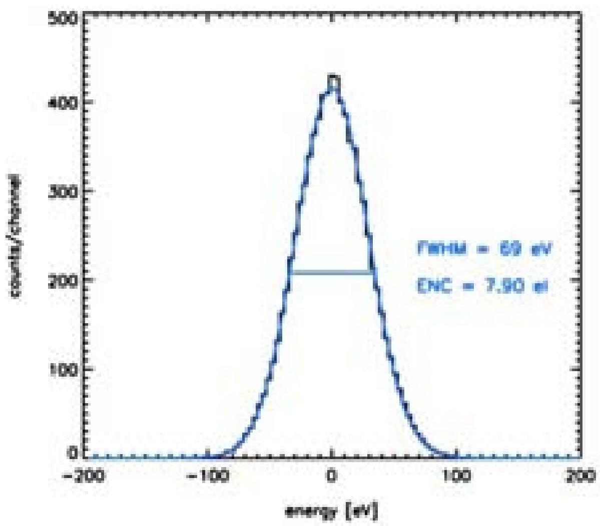
30 uA drain current
-5 V drain voltage
-5 V gate voltage
6 us gaussian shaping

ENC=7.9 electrons after irrad.

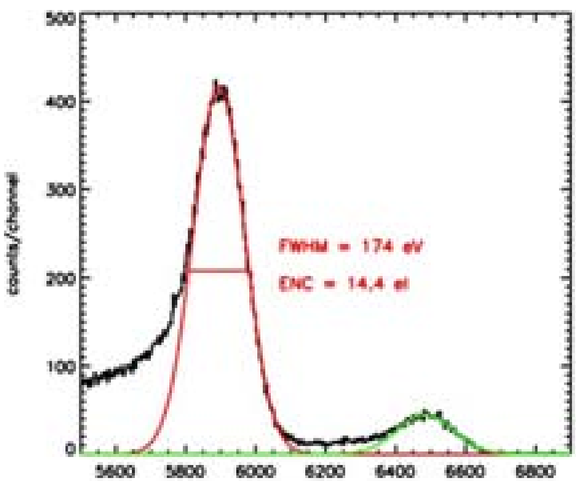


Fe55 spectrum after 1Mrad irradiation

Noise peak



Mn Kalfa Kbeta peaks



On module electronics

Switcher ASIC:

provides steering signals (double) row by (double) row:

external gate voltage pulse

clear voltage pulse

CURO:

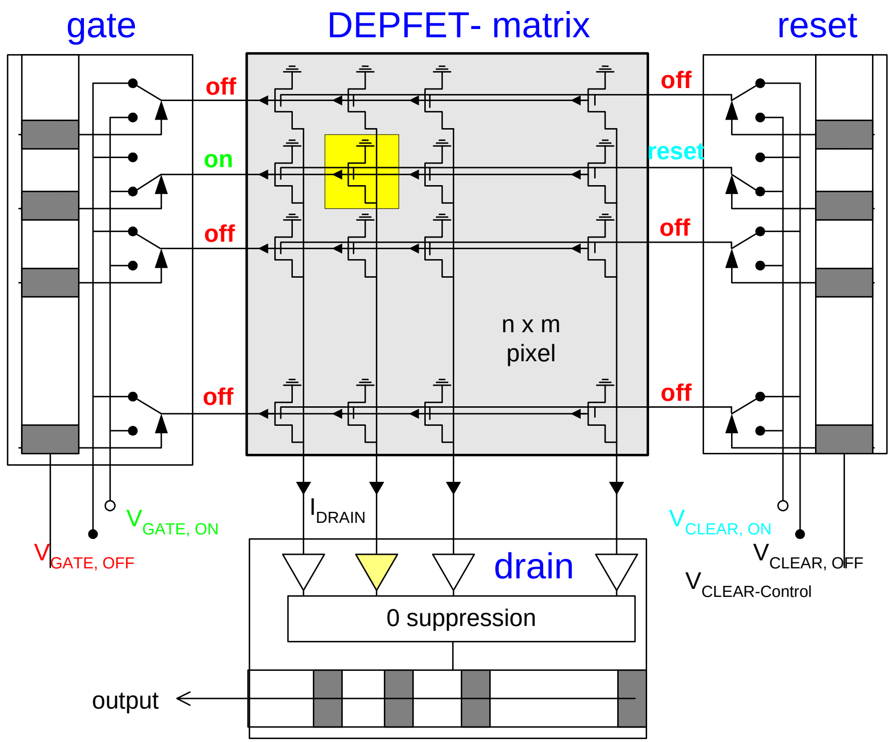
subtracts drain currents before/after clear for all columns in parallel

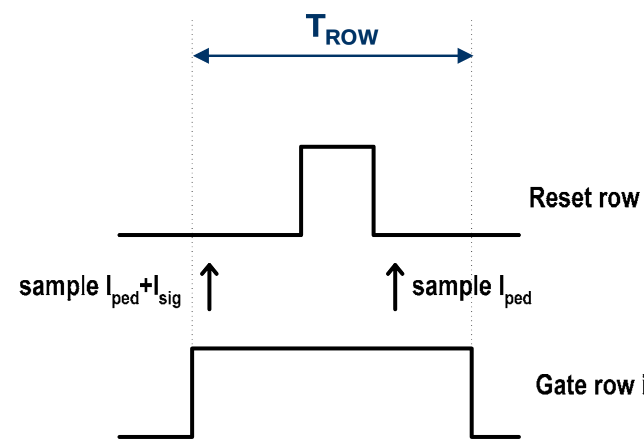
shifts differences into analog FIFO

identifies pixels with signals

sends analog signals of hit pixels to outside ADC

Matrix operation





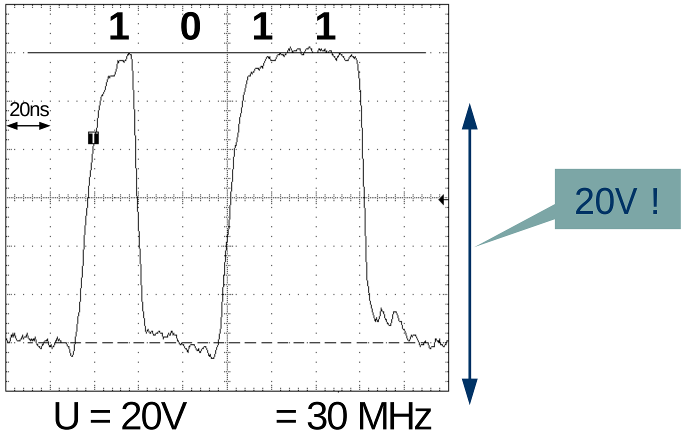
Readout sequence

- o Select one row via external Gates and measure Pedestal + Signal current
- o Reset that row and measure pedestal currents
- o Collected charge in internal gate ~ (Difference of both currents)
- o continue with next row ...

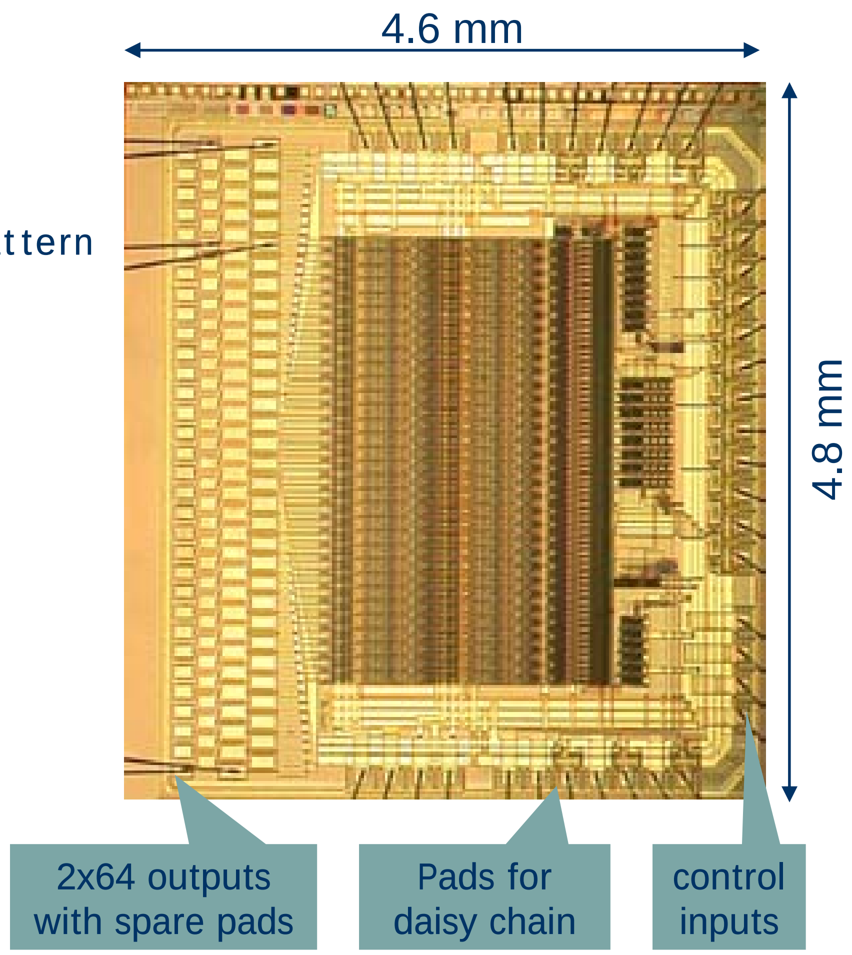
Only selected rows dissipate power
but
Sensor still sensitive even with the DEPFET in OFF state

Switcher ASIC (Multiplexer)

- **64 channels** with **2 analog MUX** outputs
- Can switch up to **25 V**
- **digital control ground + supply floating**
- **fast internal sequencer** for programmable pattern (operates up to 80MHz)
- **Daisy chaining** of several chips on a module possible
- 0.8µm AMS HV technology
- Radiation tolerance may be problematic!



Switching 20V @ 30MHz

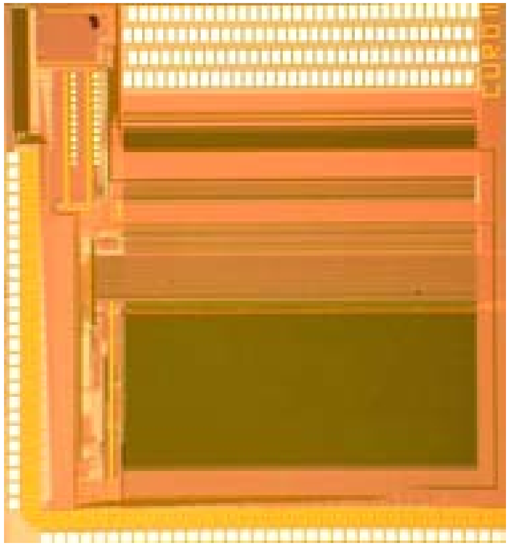


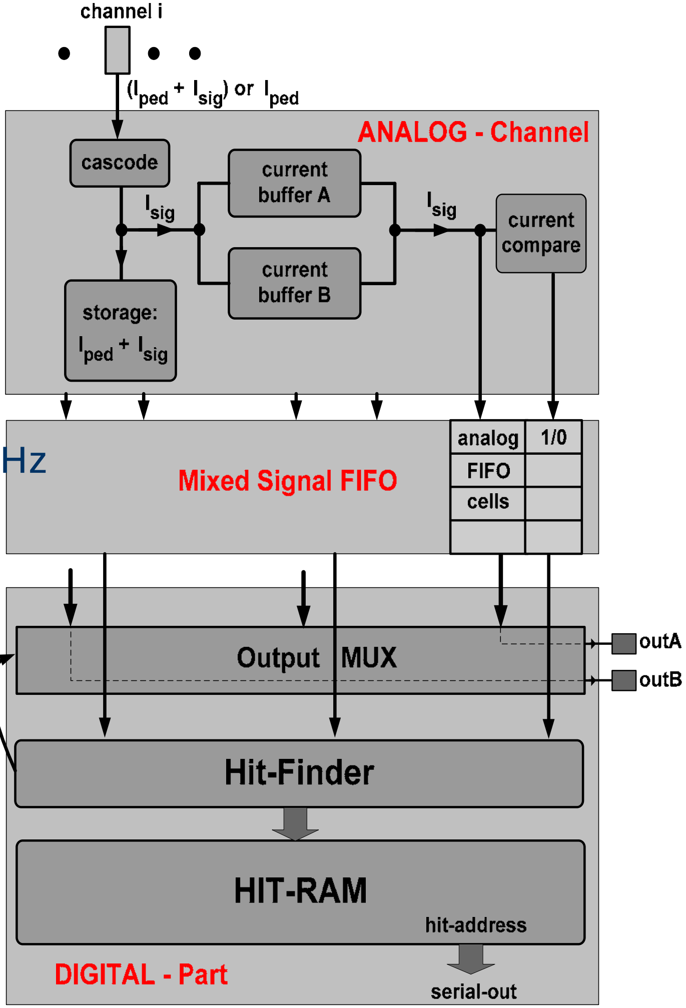
CURO ASIC (Drain Readout)

- ✓ **Digital part**: works up to **110 MHz**
- ✓ **Noise** (CURO) as calculated: about **40nA**
  expected signal (MIP) in thin DEPFET

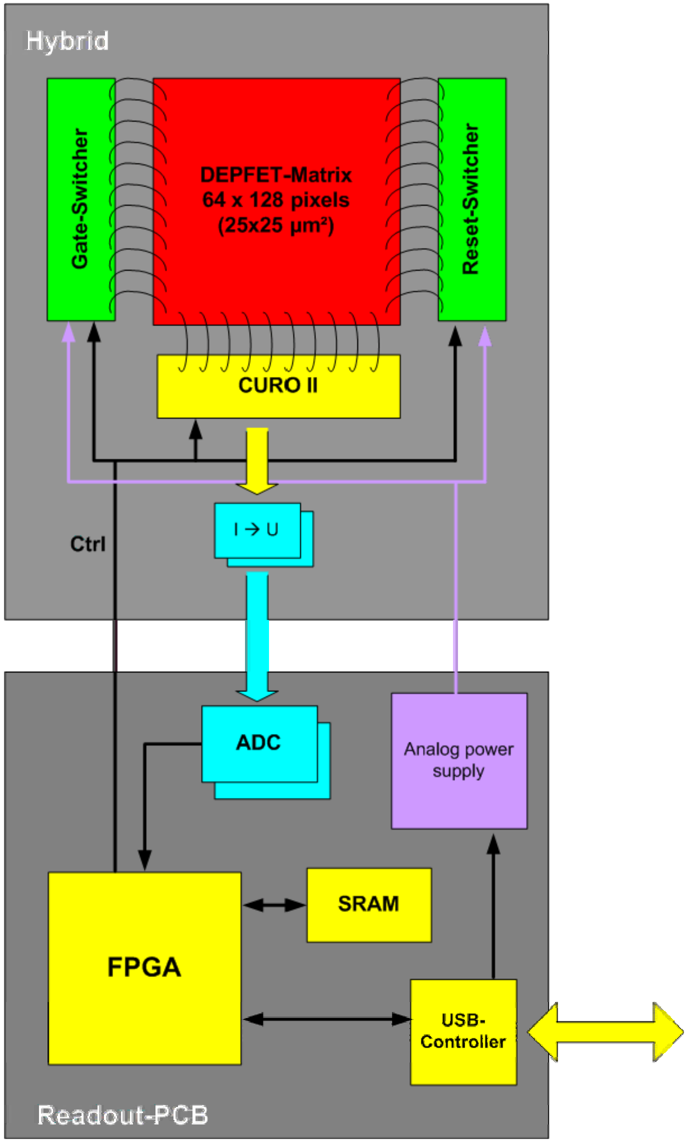
  50 µm * 80 e-/µm * g_q (0.4nA/e-) = 1.6 µA
  → **S/N ≈ 40**

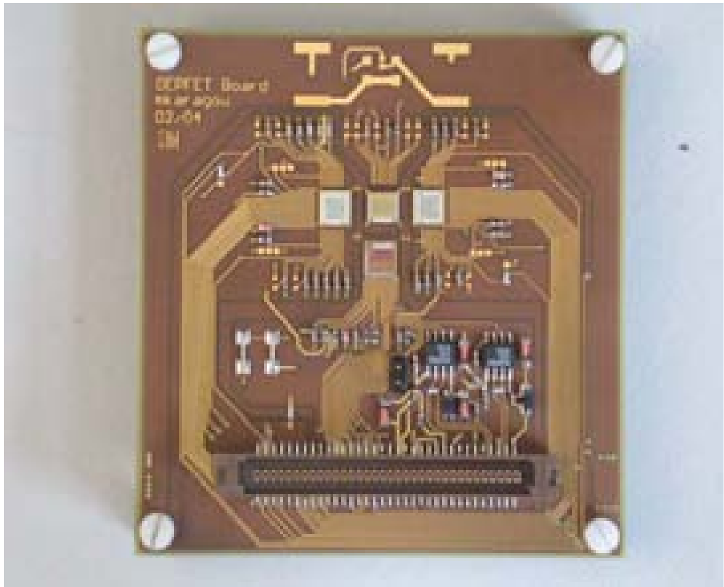
- ✓ **Analog Part** works with 50MHz
  (means **100MHz sampling** !)
- ✓ **Digital Part** (Hit Finder): works up to 110MHz
- ✓ **Power consumption**: 2.8 mW / channel @ 50MHz

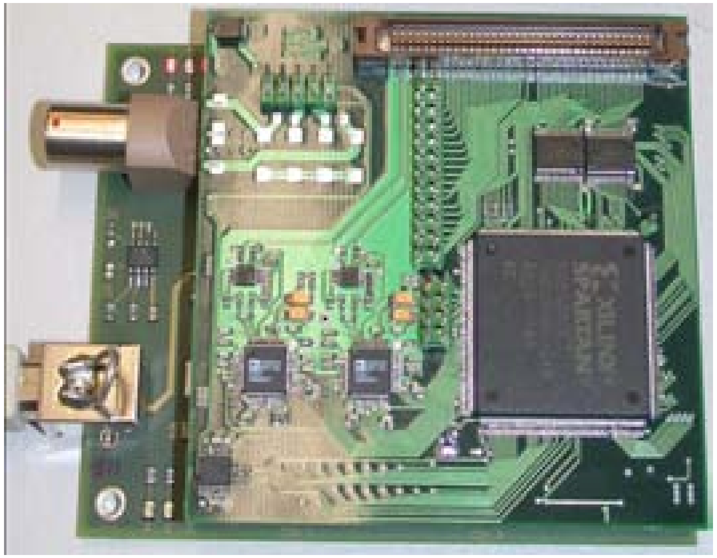




DEPFET prototype system







ILC DEPFET-System in the Lab

ILC system performance in the lab:

High speed: row rate 0.6 MHz

Noise: 230 e$^-$

Noise contributions:

~ 100e- from CURO etc.

~ 60e- from I2U converter (CURO → ADC)

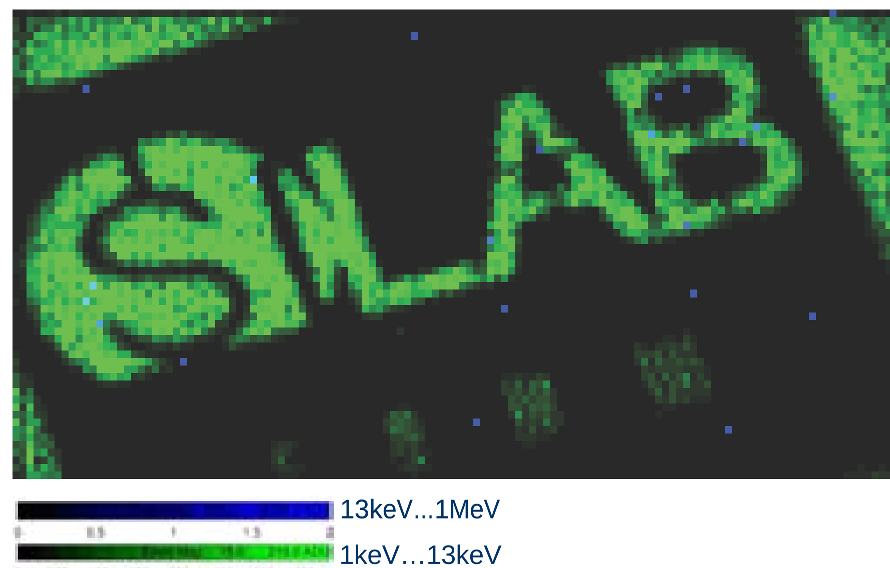
~ noise pickup of I2U converter

10µm thick Tungsten-Mask

irradiation with ^{55}Fe (6keV γ, 1700 e-)

2.7 mm

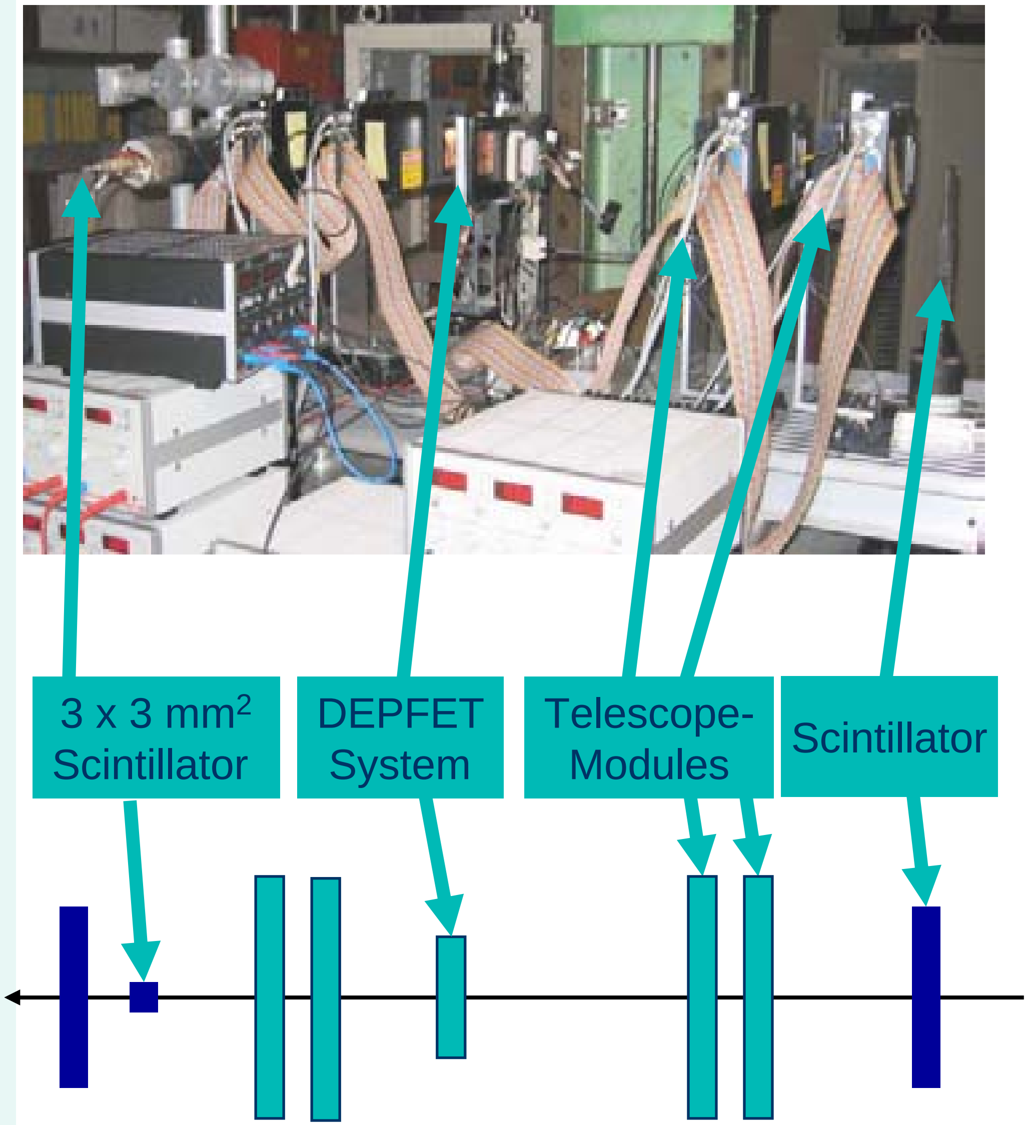
3.4 mm



13keV...1MeV

1keV…13keV

Test Beam Setup (Jan / Feb 2005 @ T24, DESY)



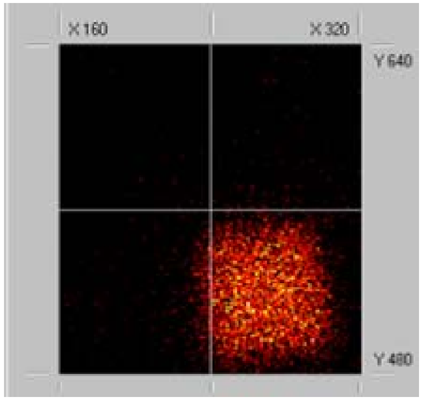
- Beam T24 @ DESY, Jan/Feb. 2005
- Electrons @ 4GeV
- Reference telescope:

  4 Si-strip planes (pitch in x- and y: 50µm)

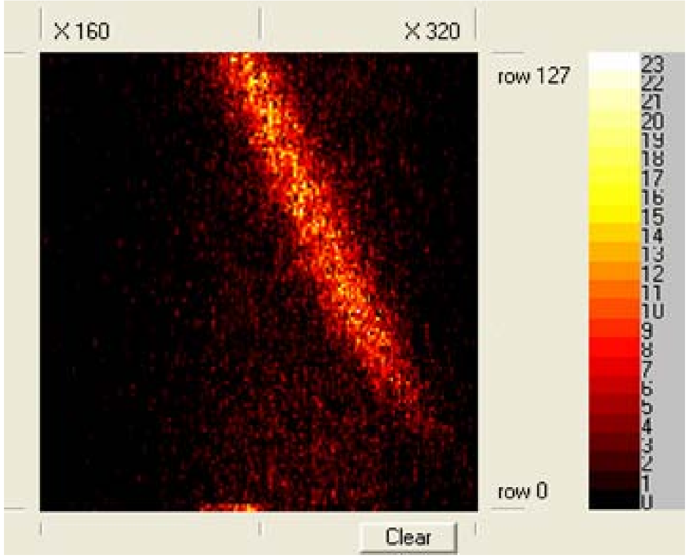
- Two matrices have been tested with

  4 x 128 pixels of 36µm x 28.5µm

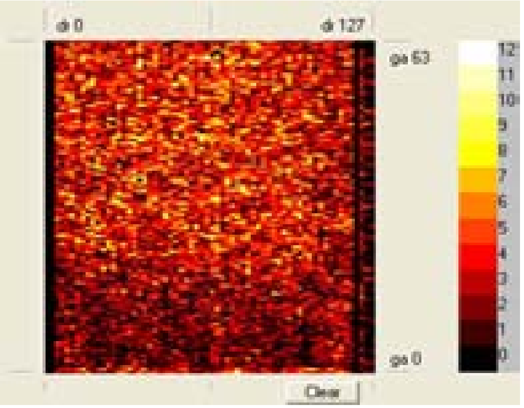
Test Beam Results: Online Correlations



Beam spot on telescope



correlation telescope x ⇔ DEPFET x



Beam spot on (small) DEPFET

- Event rate: 10Hz
- collected 10 million events
- highE / non-highE in beam
- data analysis ongoing

Module Concept/Power Consumption

Total power consumption of the vtx-d in the active region (TDR design, 25 μm pixel)

DEPFET matrix only:

1st layer : 2 rows active, $30\ \mu A \cdot 5V \cdot 650 \cdot 2 \cdot 8 =$ 1.6 W

2nd .. 5th layer: 1 row active, $30\ \mu A \cdot 5V \cdot 1100 \cdot 1 \cdot 112 =$ 18.5 W

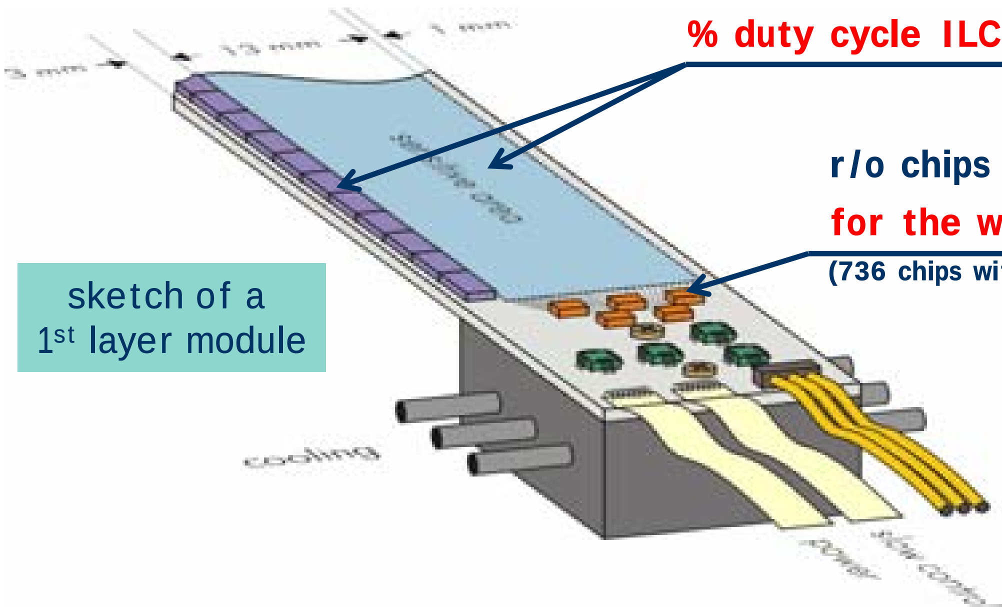
Steering chips: assuming 0.15 mW for an inactive, 300 mW for an active channel

1st layer : $[(4998 \cdot 0.15\ mW)+(2 \cdot 300mW)] \cdot 8 =$ 10.8 W

2nd ..5th layer: $[(6249 \cdot 0.15\ mW)+(1 \cdot 300mW)] \cdot 112 =$ 138.6 W

Σ active region ≈ 170 W

% duty cycle ILC 1/200 → ≈ 0.9 W



sketch of a 1st layer module

r/o chips (current version):2.8 mW/chn.

for the whole vtx-d: ≈ 2W

(736 chips with 128 channels 1/200 -> 1.3W)

Conclusion

Achievements:

- Present Pixel size: 24x33 μm^2 – can go to ~ 20x20 μm^2, limited only by manufacturing equipment
- Complete clearing works with short (10ns) clear pulses at moderate voltages. No need to clock clear gate
- Radiation tolerance (threshold voltage shift) demonstrated up to 1Mrad
- Technology for thin ($\leq$ 50µm) detectors established (total budget of sensor 0.11% X_0)

Advantages DEPFET

- Charge collection by drift in fully depleted bulk
- High S/N (~40 at 100e noise), high spatial resolution (expect ~2µm)
- Low average power dissipation for full ILC system (4W)
- Fast readout possible (some 10 MHz)
- Low radiation length
- Operation at room temperature

Present collaboration: MPI Munich, Bonn, Mannheim; Charles Univ. joining
Further actively working participants are welcome

The long (and incomplete) list of open items

1:- DEPFET specific conceptual design of the vertex detector
#layers?, pixel size?, impact of the inhomogenously distributed material on the physics results.....

2:- Analyse quantitatively the mechanical and thermal properties of the ladders
FEA and measurements

3:- Development of the interconnect and assembly technology for the modules
bump bonding, wedge bonding with the thin modules?

4:- Irradiation and characterization of matrices, chips and the entire system with
gammas, hadrons, electrons...

5:- EMI: Is it really a problem??

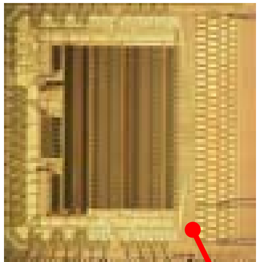
6: - ......

Next steps within the presentcollaboration:

Operate complete system at full ILC speed	→ Bonn, MPI
Beam Tests at CERN (pos. resolution??)	→ all
Produce thin sensors with larger matrices	→ MPI
Design new SWITCHER	→ Mannheim
Design new CURO (deeper FIFO, standby mode, ADC?,)	→ Bonn

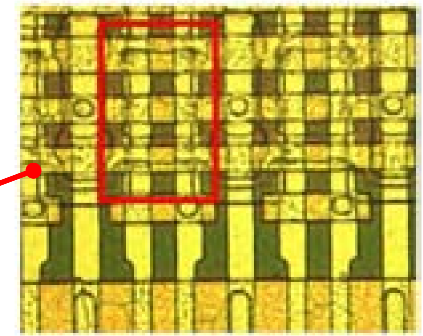
Project Status - in Summary

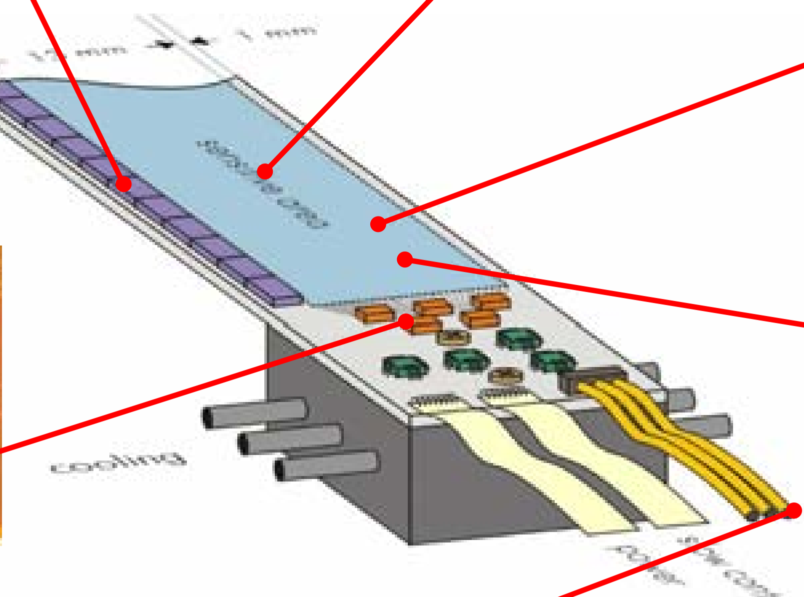
✓ steering chips Switcher II



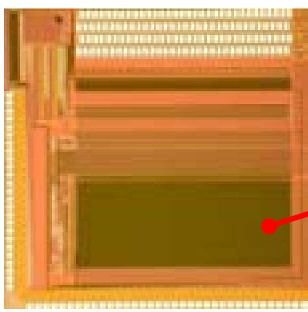
✓ thinning technology

✓ Technology development

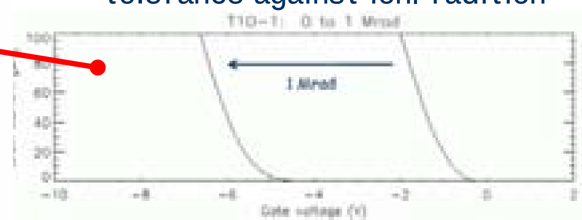


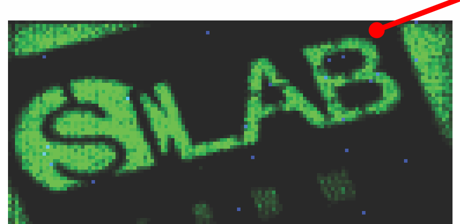


✓ r/o chips Curo II

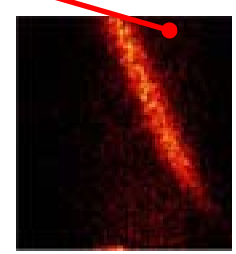


✓ tolerance against ion. radition



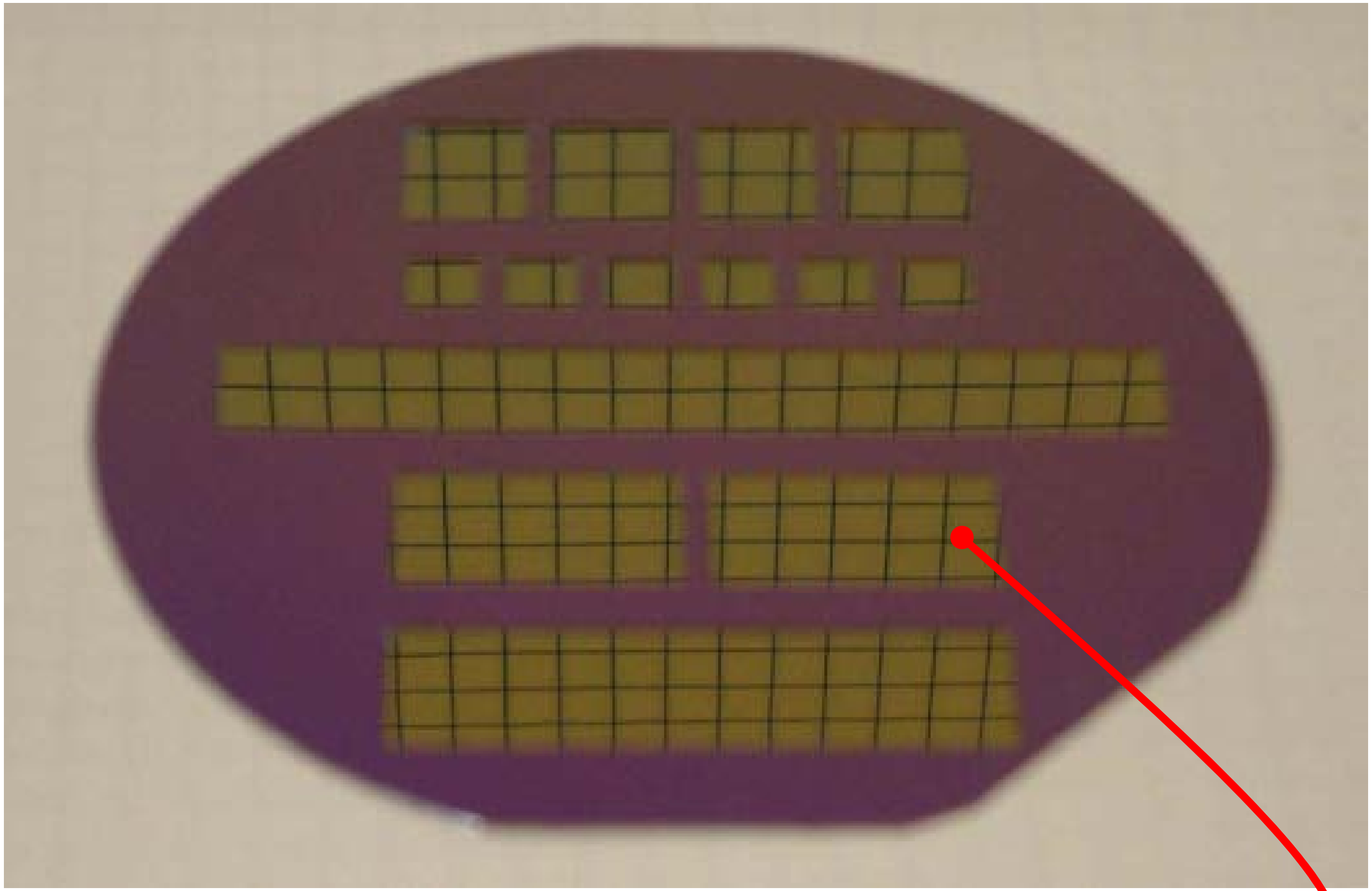


✓ system in the lab and in the beam



Mechanical Dummies

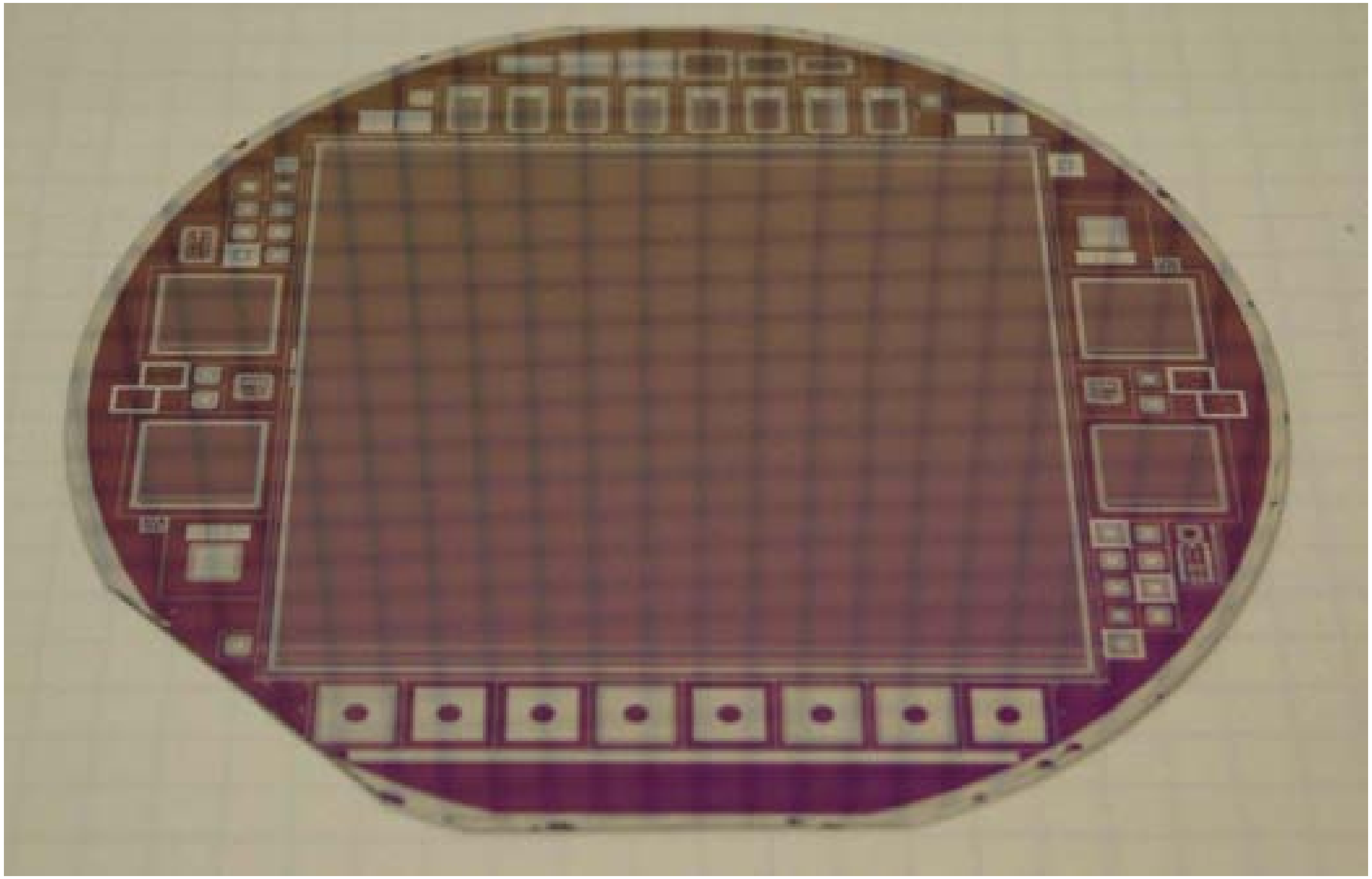
the mirror image of a 5mm grid...



polished back side of a **40 µm** thin top wafer after deep etching with TMAH

Mechanical Dummies

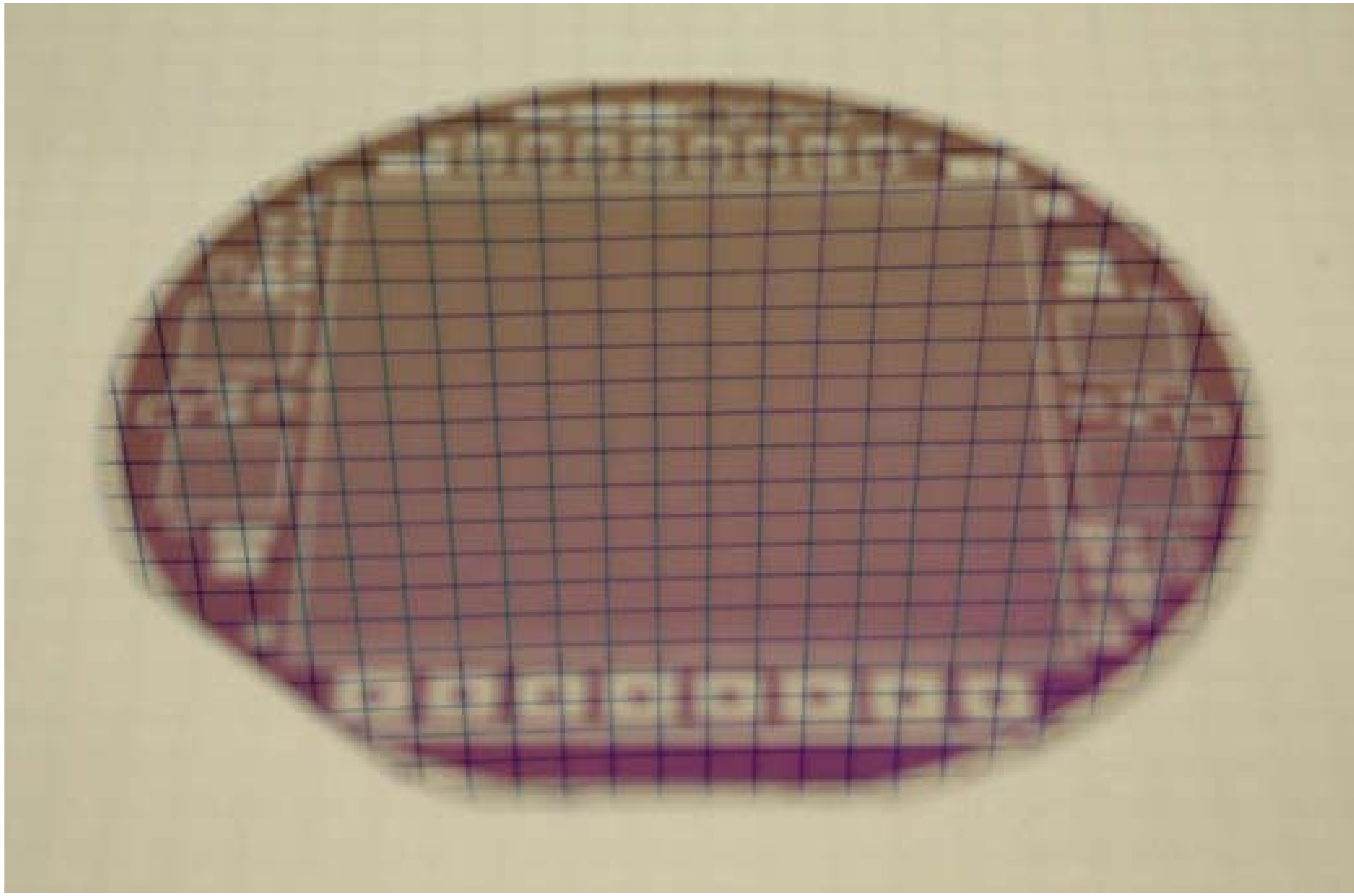
the mirror
image of a
5mm grid...



40 µm top wafer side: patterned aluminum layer (ATLAS strip detector prototype mask)

Mechanical Dummies

the mirror
image of a
5mm grid...



focus on the mirror image: **no distortions visible, even after single sided metallization!!**