

SOI detector R&D

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on behalf of the SOI workgroup

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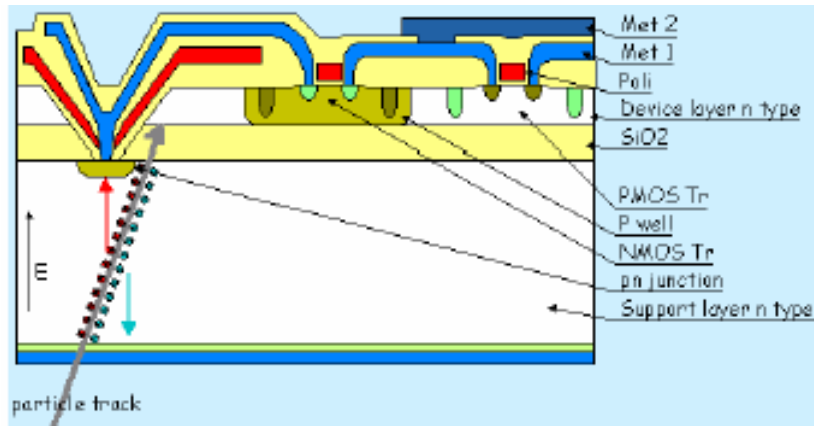
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Principle of SOI Monolithic detector



Integration of a fully depleted p⁺-n junction matrix and the readout electronics in a wafer bonded SOI substrate

Detector → Handle wafer

High resistive (> 4 kΩcm, FZ)

400 μm thick

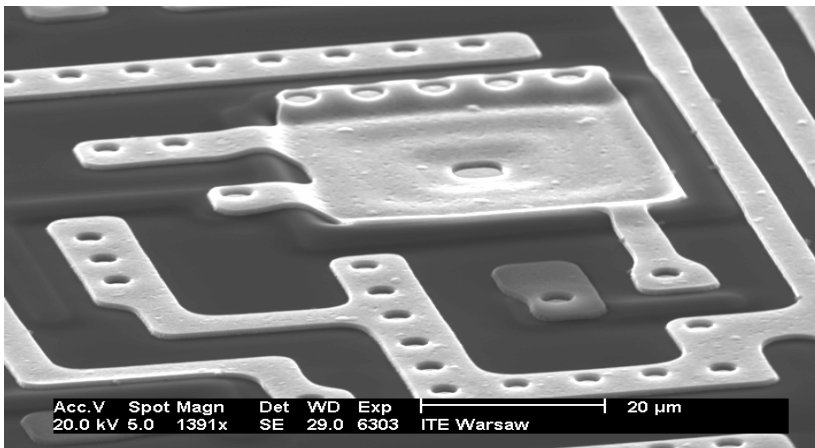
conventional p⁺-n matrix

Electronics → Device layer

Low resistive (9-13 Ωcm, CZ)

1.5 μm thick

Standard CMOS technology



SOI pros and contra

PROS

- **Monolithic:** no need of any hybridization and consequent thickness reduction
- **Fully depleted:** high SNR, high sensitivity
- **Standard CMOS electronics:** both type of transistors
- **Custom technology:** will never become obsolete

CONTRA

- **Non standard technology:** requires dedicated process in non standard foundries
- **Thermal budget:** high temperature processes for the electronics parts clash against the low thermal budget required for high quality p⁺-n junctions.
- **Low availability of SOI substrate:** with detector grade handle wafer

SOI development

2002

2003

2004

2005



Phase 1: Technology definition

Phase 2: Small area prototype

Phase 3: Full area fully functional sensor

Developed by the SUCIMA collaboration within a EC project for medical applications.

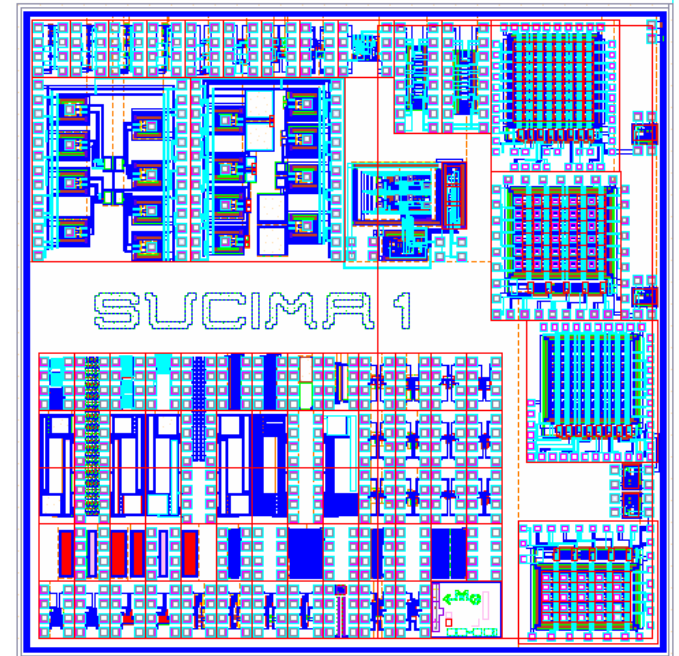
US Patent Application no. PCT/IT2002/000700

- Electronics design by the AGH team
- Technological implementation at IET on a 3 μ m production line

Phase 1: technology definition

Two steps procedure:

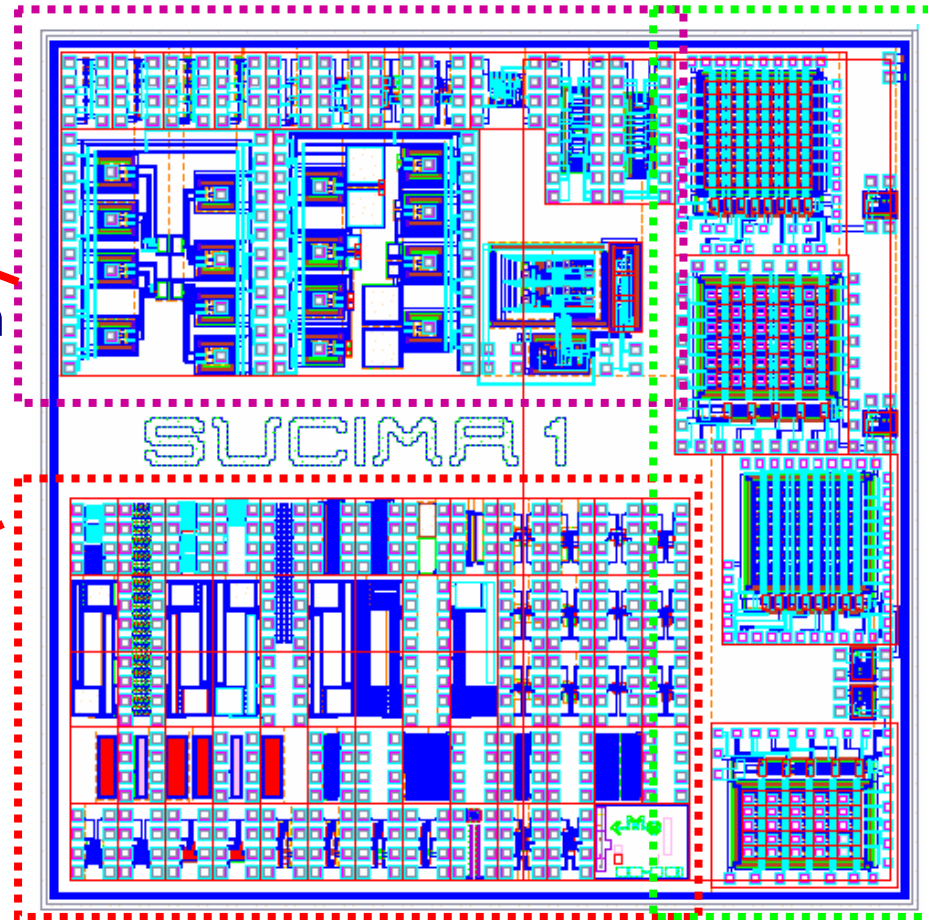
1. Definition of the technology file → test structure
2. Readout electronics functionality → AMS 0.6 multi-project run



SOI test structures / 1

Structure for
electronics
circuit
characterization

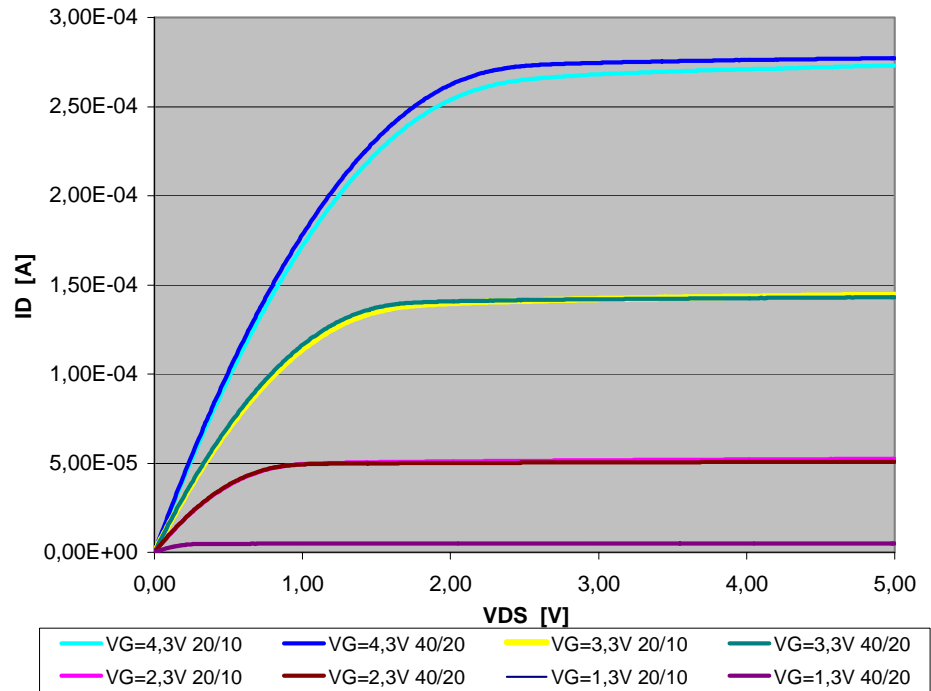
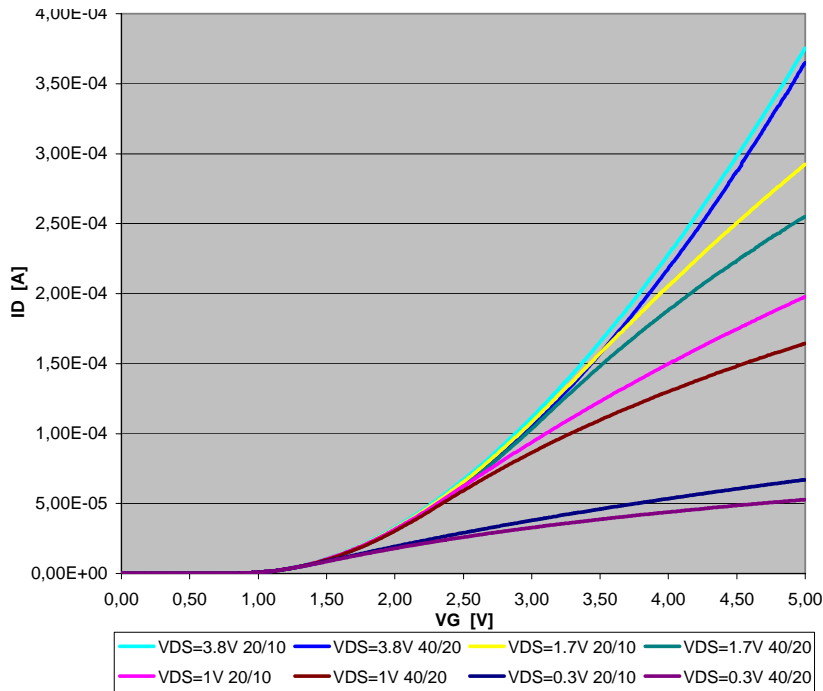
Structure for
technological
parameter
extraction



Detector
prototypes
(8x8 pixels) w/
and w/o
charge
injection pad.

SOI test structures / 2

Transfer and output characteristics of NMOS with W/L=20/10 and 40/20



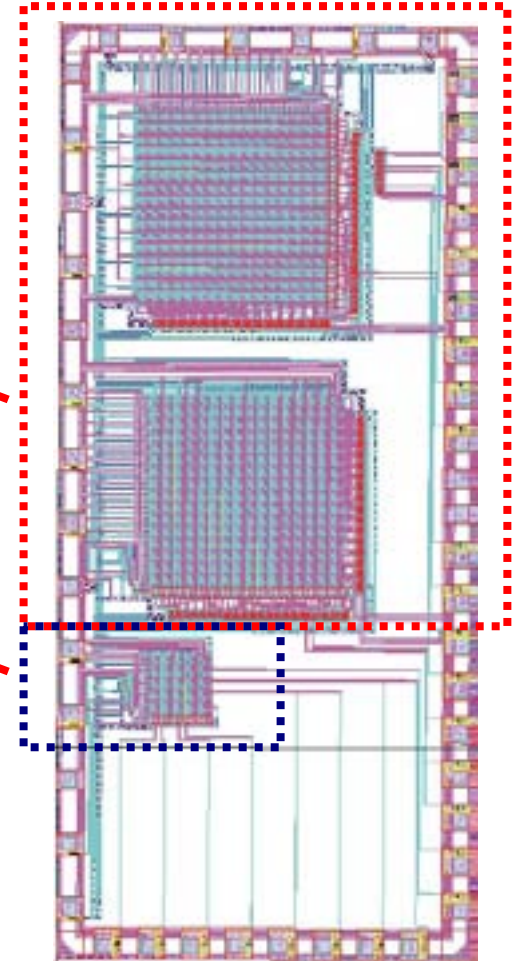
$g_{ds} \approx 428 \text{ nS}$ @ $V_{GS}=2.3 \text{ V}$ for $W/L = 20/10$

$g_{ds} \approx 196 \text{ nS}$ @ $V_{GS}=2.3 \text{ V}$ for $W/L = 40/20$

Electronics functionality assessment / 1

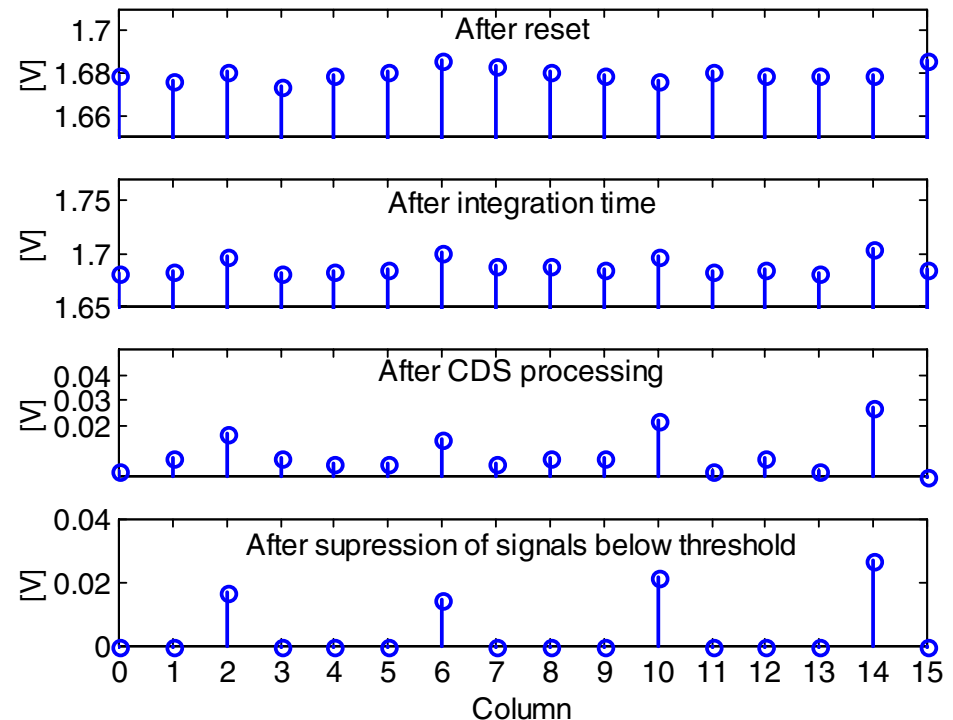
Readout electronics part in AMS 0.6

- 2 fully functional matrices 16x16 pixels with different pixel addressing circuitries
- 1 smaller 5x5 matrix with only the analog part



Electronics functionality assessment / 2

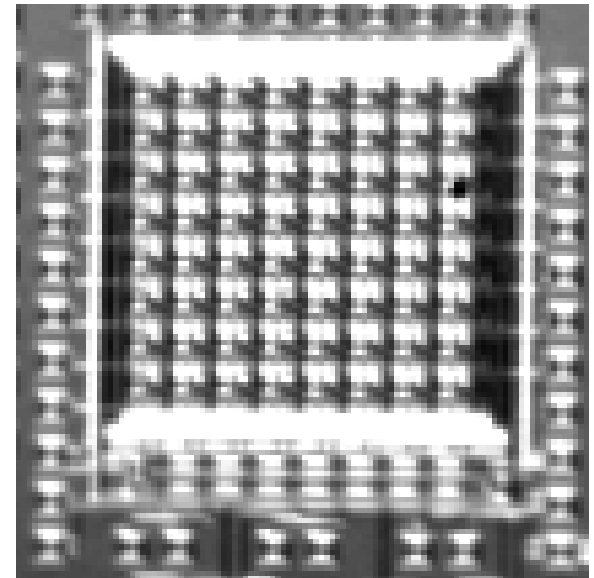
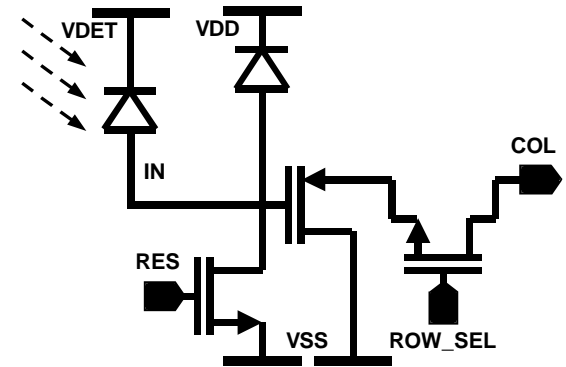
- Measured noise ~ 1.78 mV
- 20 mV signal injected every fourth pixel
- Test of the CDS processing with 5σ threshold.



Phase 2: small area prototype / 1

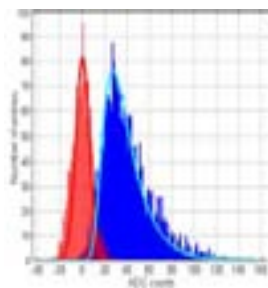
- Basic 3 trans. architecture only slightly modified with PMOS

- Single cell dimensions are $140 \times 122 \mu\text{m}^2$.
- Matrix dimensions: $1120 \mu\text{m} \times 976 \mu\text{m}$
- Not surrounded by guardring

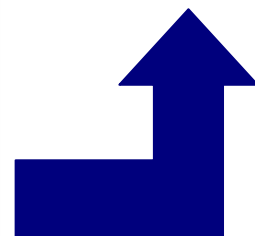
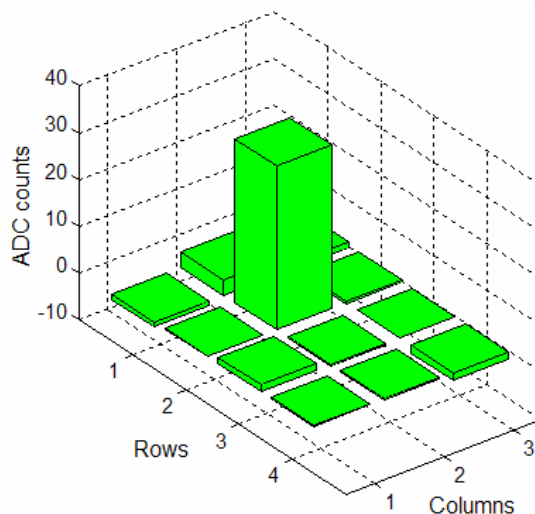
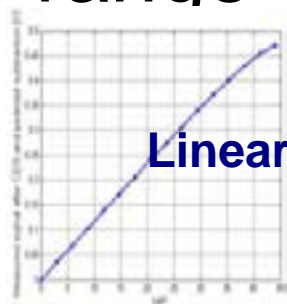


Phase 2: small area prototype / 2

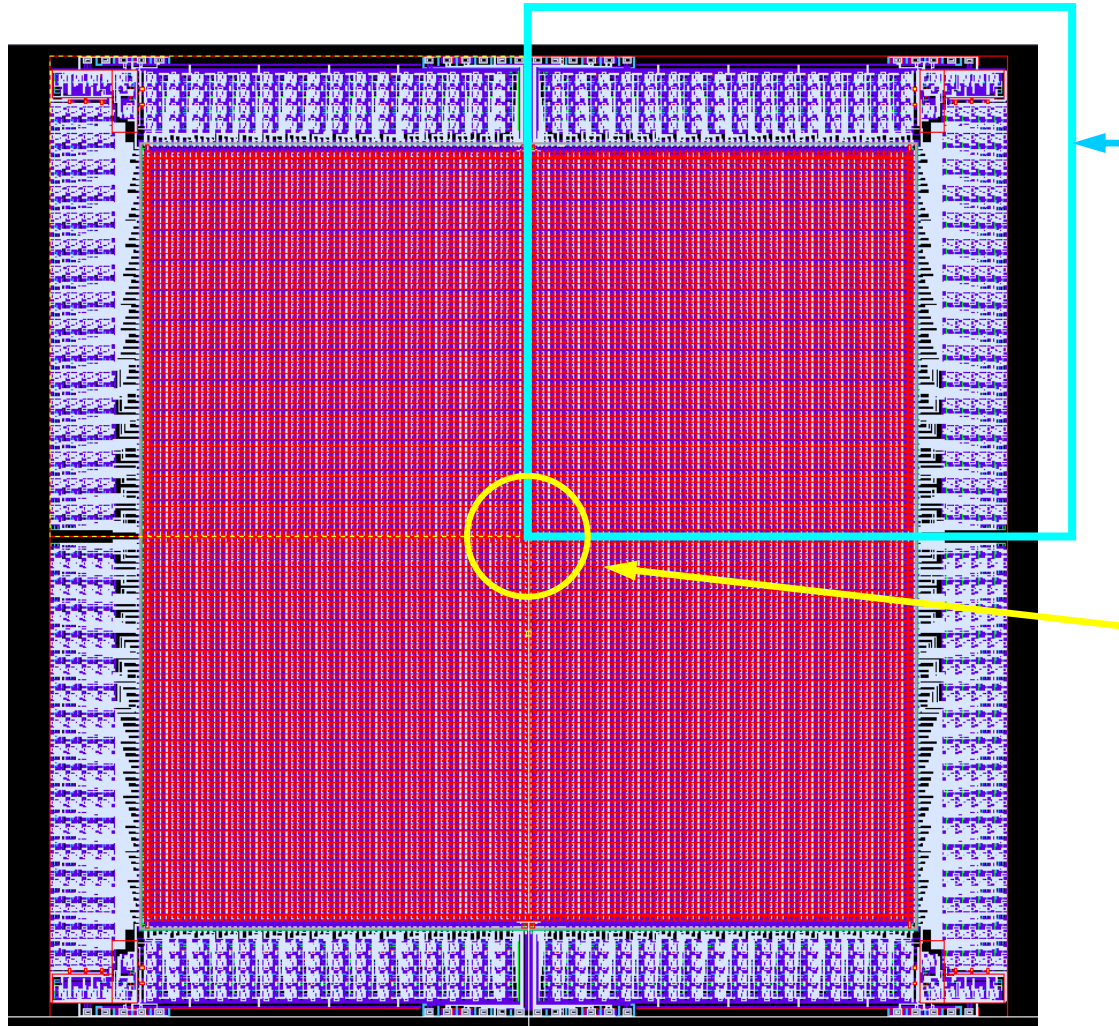
- Charged particle sensitivity with radioactive sources
- Linearity and dynamic range with infrared laser



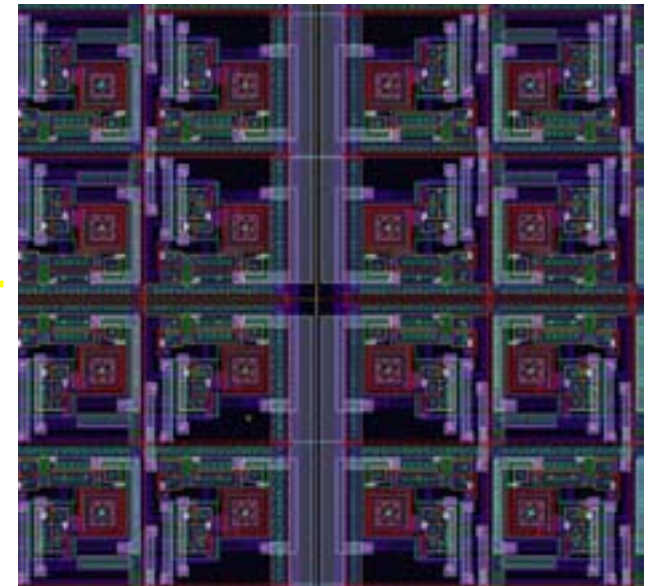
^{90}Sr



Phase 3: full area sensor design

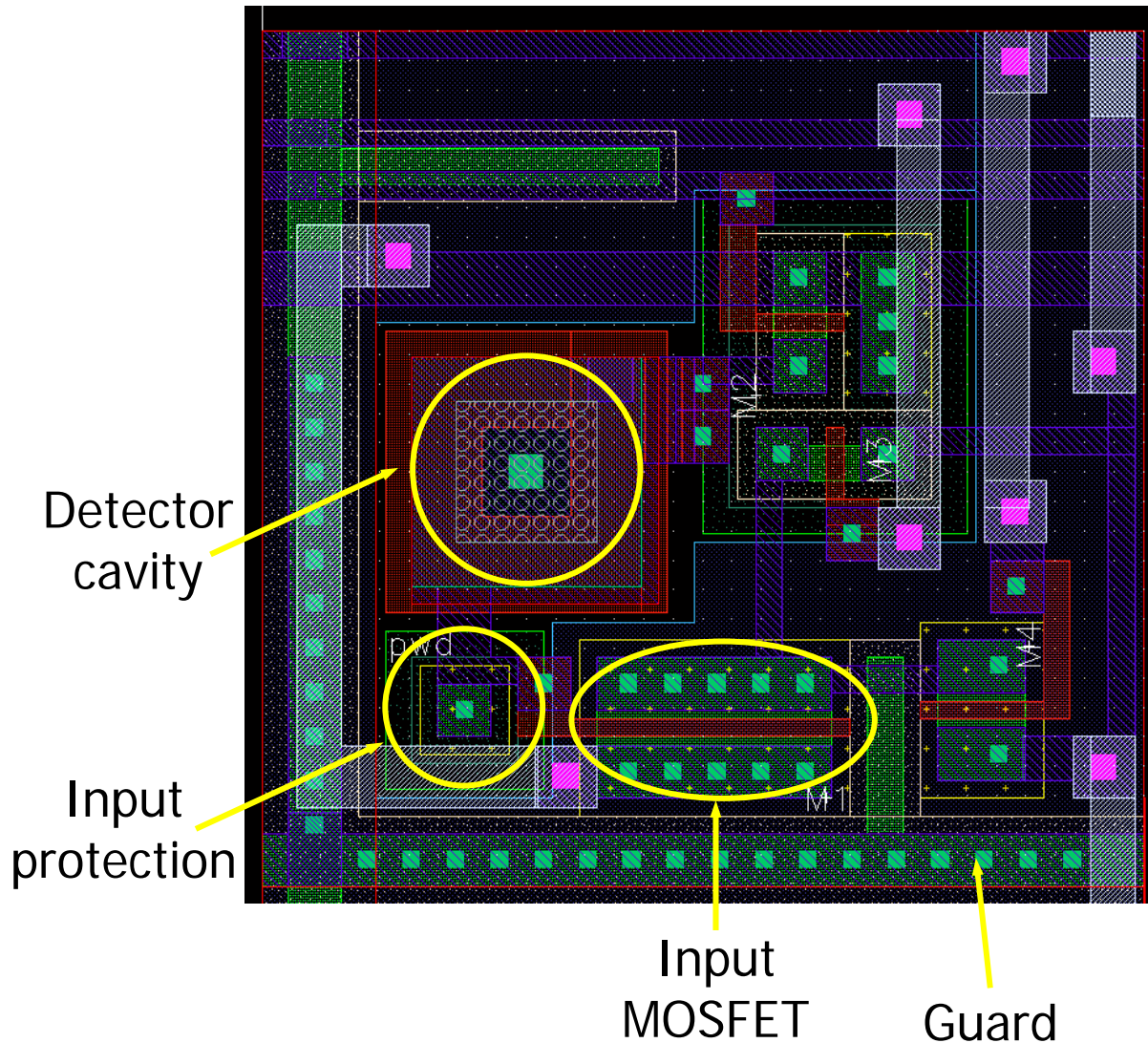


Functionally
independent quarter
of the detector



No dead area,
preserved pitch

Sensor characteristics



- 128 x 128 pixels on 2.4 x 2.4 cm² sensitive area
- Dimensions: 150x150 μm²
- Input capacitance similar to test structures → similar signals levels
- Larger PMOS in transmission gate → improved linearity

Preliminary results

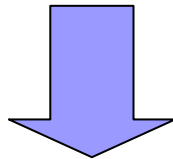
- Sensor sensitivity observed with laser pointer and α particles.
- Dynamic range up to 100 MIP
- Charge to voltage gain 3.6 mV/fC
- Problems with production yield: only $\frac{3}{4}$ of the best chip fully functional
- Readout frequency up to 4 MHz



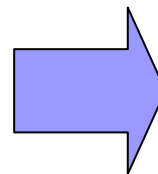
Future plans / 1

- Proof of principle accomplished taking advantage of IET.

Partner foundry with a primitive 3 μ m production line



Looking for another partner (device company) with a more advanced technology



Contacts positively established with Hamamatsu 1 year ago

Full cost 650 k€
(of which for personnel 200 k€)

Future plans / 2

- Next formal meeting with Hamamatsu during Pixel 2005 conference in September with the definition of a development plan
- Interests from many groups: INFN, AGH, KEK, BONN