D. Strom
With apologies to C. Baltay
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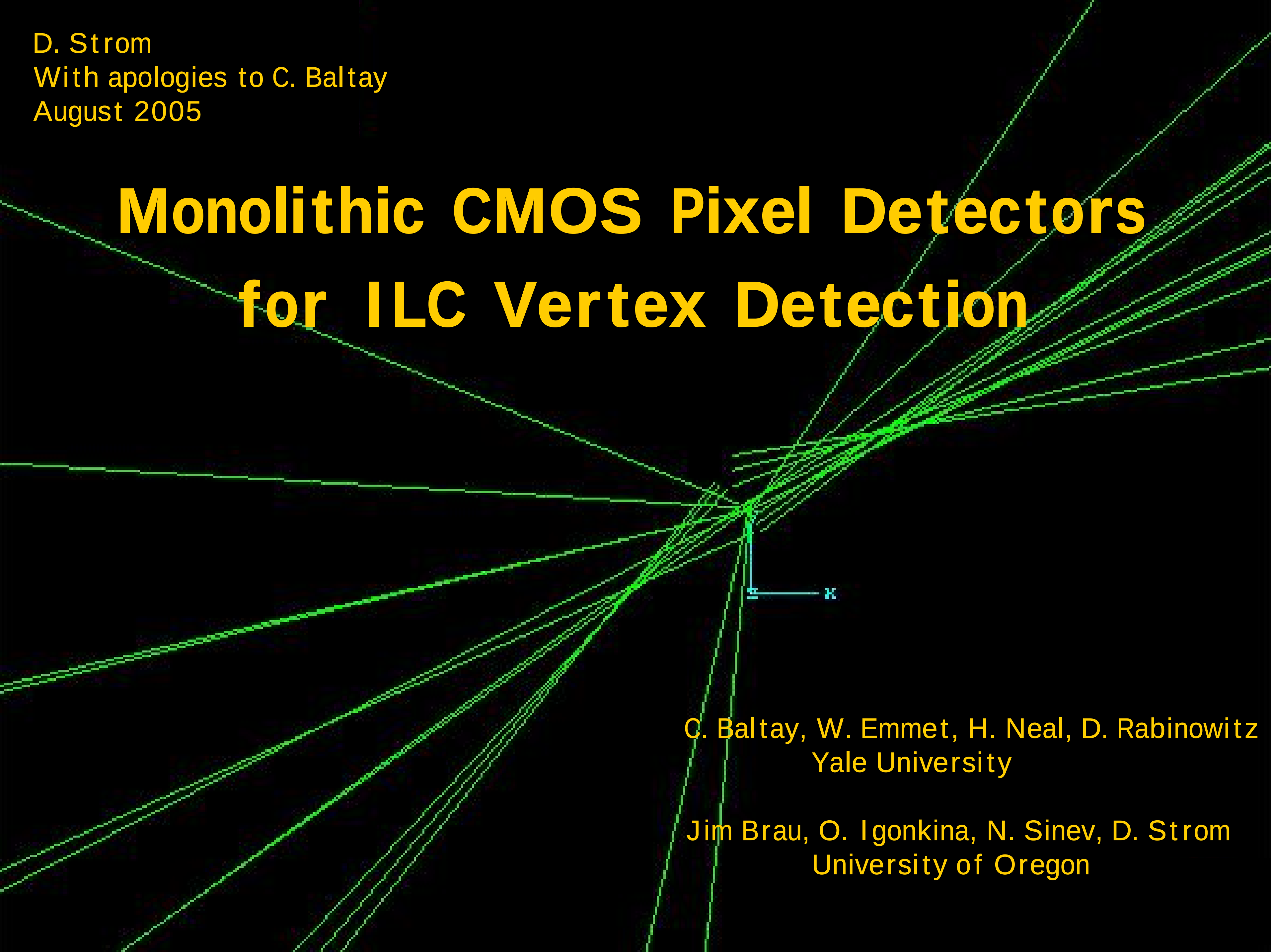
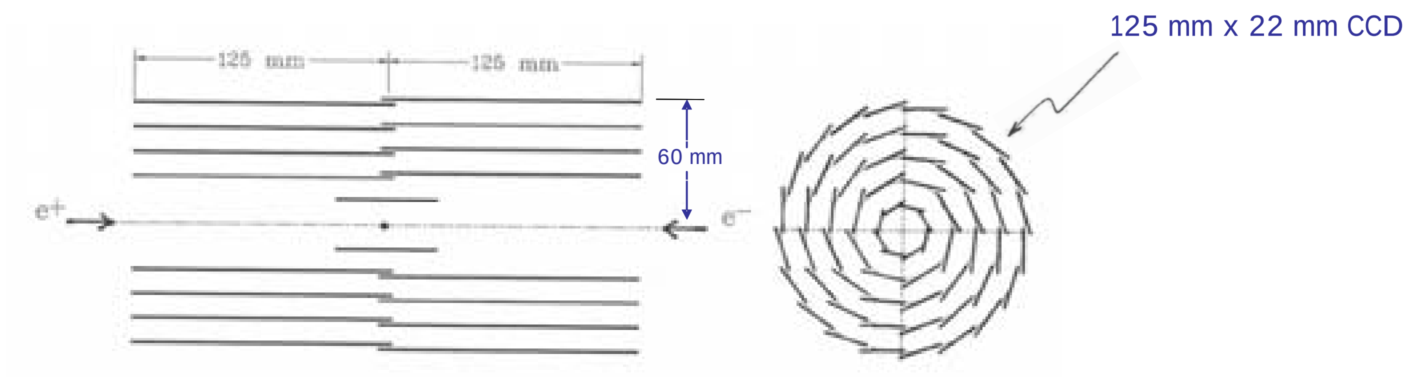
Monolithic CMOS Pixel Detectors for ILC Vertex Detection



C. Baltay, W. Emmet, H. Neal, D. Rabinowitz
Yale University

Jim Brau, O. Igonkina, N. Sinev, D. Strom
University of Oregon

ILC Vertex Detector Design



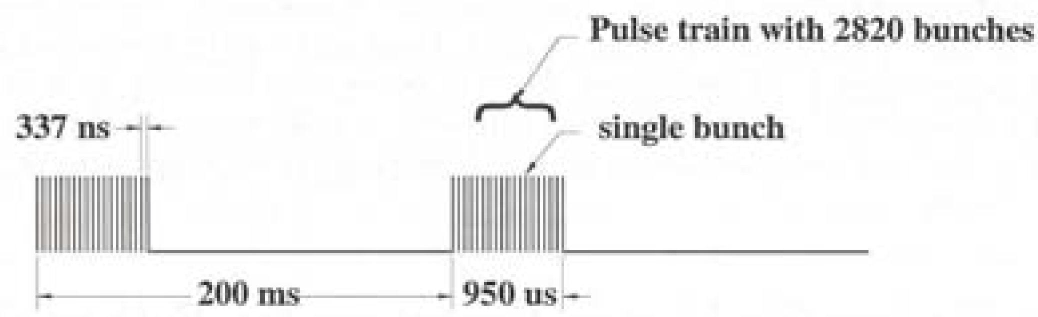
Monolithic CMOS Pixel Detectors

Total number of chips 120

Layer	Radius	Total Length	No of Chips	Chip Size
	Cm	Cm		Cm
1	1.2	5.0	8x1	5.0x1.2
2	2.4	25.0	8x2	12.5x2.2
3	3.6	25.0	12x2	12.5x2.2
4	4.8	25.0	16x2	12.5x2.2
5	6.0	25.0	20x2	12.5x2.2

Total Number of Pixels 1.25 x 10^{10}

Time Structure for the Cold Design



Background Calculation:

At 1.5 cm from Interaction Point with 3 Tesla field expect
0.03 hits /mm^2/bunch crossing

Will use this number for the entire detector

Conventional CCD's Not Well Suited for This Application

- Consider SLD type CCD's with 20μ x 20μ pixels

    22 mm x 125 mm = 2750 mm^2

    with 6.9 x 10^6 pixels/CCD

- Readout time at 25 MHz is 275 msec

    May be can push to 50 MHz readout or divide CCD into several readout sections

➔ Can readout in 200 msec between pulse trains

- Occupancy, integrating over 2820 bunches in a pulse train

    0.03 hits/mm^2/bunch x 2820 bunches x 3 pixels/hit

    = 250 pixels hit/mm^2

    or 10% of the pixels have a hit (occupancy)

- SLD Experience – occupancy of 10^{-3} or 2.5 hits/mm^2 are maximum we could handle!

➔ Occupancy too high by factor of ~ 100!!

Monolithic CMOS Pixel Detectors

➔ What are they?

- New CMOS technology makes pixels as small as 5 μ x 5 μ possible
- Each pixel has its own intelligence (electronics) under the pixel
- Unlike CCD's, all pixels are NOT read out in a raster scan
- Reads out x,y coordinates only of pixels with hit (i.e., exceeding an adjustable threshold) at 25 MHz
- Monolithic design – photosensitive detector pixel array and read out electronics for each pixel on the same piece of silicon – can be quite thin (few x 100 μ?)

➔ Advantages over CCD's

- Significantly faster read out. Typical occupancy of vertex detector at e^+e^- collider ~ 10^{-3}

  1000 times faster read out! (Read only hit pixels!)
- Potentially more radiation hard
- Small 5 µ x 5 µ pixels allow good resolution

➔ Advantages over hybrid pixel devices used at the LHC

- Do not need bump bonding of pixel detector to electronics layer
- Allows much smaller pixels

Present Conceptual Design

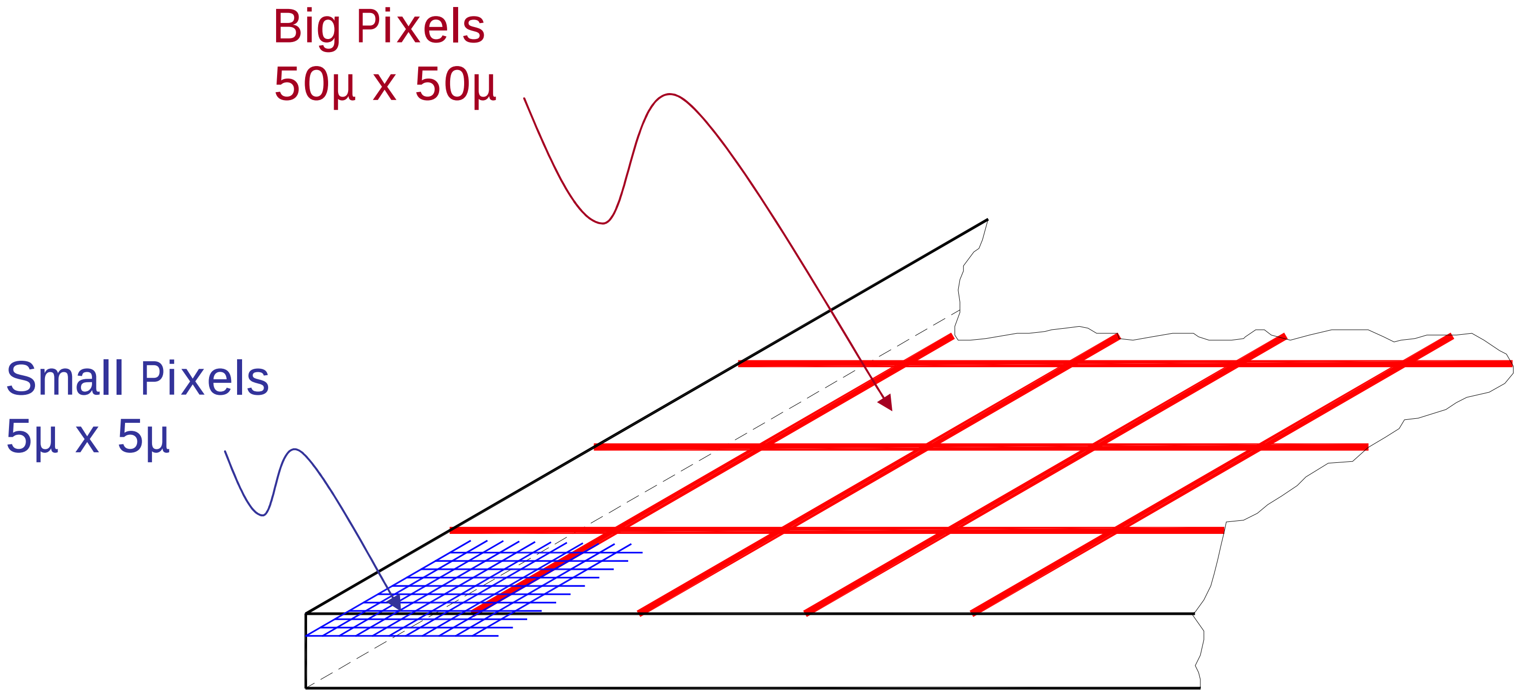
- During the past year, working with SARNOFF we developed a conceptual design that:
  - we believe will work for an ILC Vertex Detector
  - that SARNOFF believes they can build.
- Plan to integrate over pulse train and readout during 200 msec between trains to avoid EMI (Electromagnetic Interference) during train.
  - Occupancy would be too high
  - BUT – for each hit, readout x,y, intensity, AND time of hit (time to better than 300 nsec precision effectively tagging each hit with its bunch crossing number)
  - In analyzing Vertex detector data look only at hits which occurred in the same single bunch crossing

➔ Occupancy ~ 10^{-6} or 0.03 hits/mm^2!!

Present Conceptual Design (Continued)

- Accomplish this with a Hierarchical Design Approach. Each device will have two separate sensitive pixel arrays with its own electronic logic under each pixel
  - Big Pixel (Macro Pixel or High Speed) Array
    - 50µ x 50µ pixels
    - Triggers on hits above threshold
    - Records time of hit
  - Small Pixels (Micro Pixel or High Resolution) Array
    - 5µ x 5 µ Pixels
    - Addressable, random access array
    - Records intensity of hit (3 digit resolution)

Monolithic CMOS Pixel Detectors



Two active particle sensitive layers:

Big Pixels – High Speed Array – Hit trigger, time of hit
Small Pixels – High Resolution Array – Precise x,y position, intensity

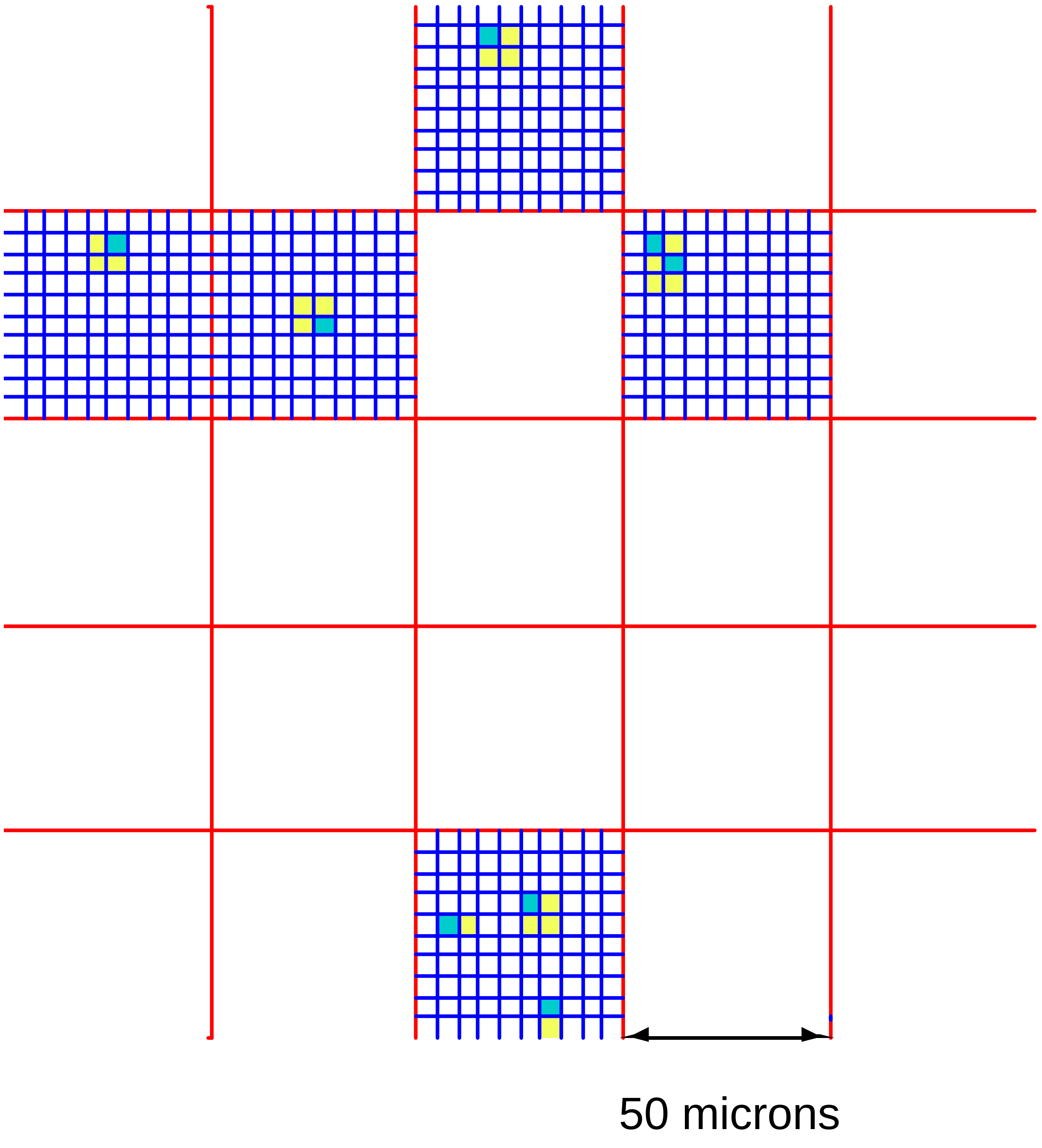
The blue grid shows the hit big pixels

The green and yellow show the hit small pixels

If all the hit pixels come from different events the big pixel with two small pixels hit will have a two-fold bucket ambiguity

The big pixel with three hits will have a three fold ambiguity

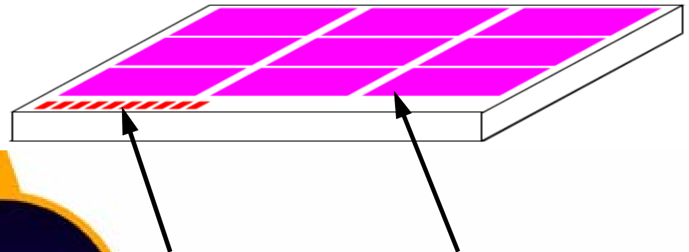
"Event Display" showing hit pixels



Array Designs

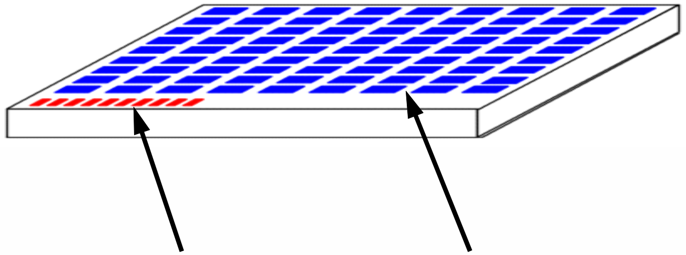
High-speed arrays

- Designed for quick response.
  - Threshold detection only.
  - Large pixels (~50 x 50 µm).
- Transmits X,Y location and time stamp of impact.



High-resolution arrays

- Designed for resolution and querying.
  - Smaller pixel size (~5 x 5 µm).
  - Random access addressability.
  - Records intensity.
- Provides intensity information only for pixel region queried.



Hierarchical Array Operation

- Particles from any particular bunch crossing traverse both the Big and the Small pixel arrays
- The Big Pixels which are hit store the time information (i.e. bunch number) in a 13 bit digital memory located under the area of the Big Pixel. The hit number counter is advanced after each hit. Up to 4 hit times can be stored under each pixel

  (The probability of a Big Pixel being hit more than 4 times in a pulse train is $\lesssim 10^{-3}$)

- The Small Pixels which are hit store the analog signal charge locally in the area under each pixel for the duration of a pulse train

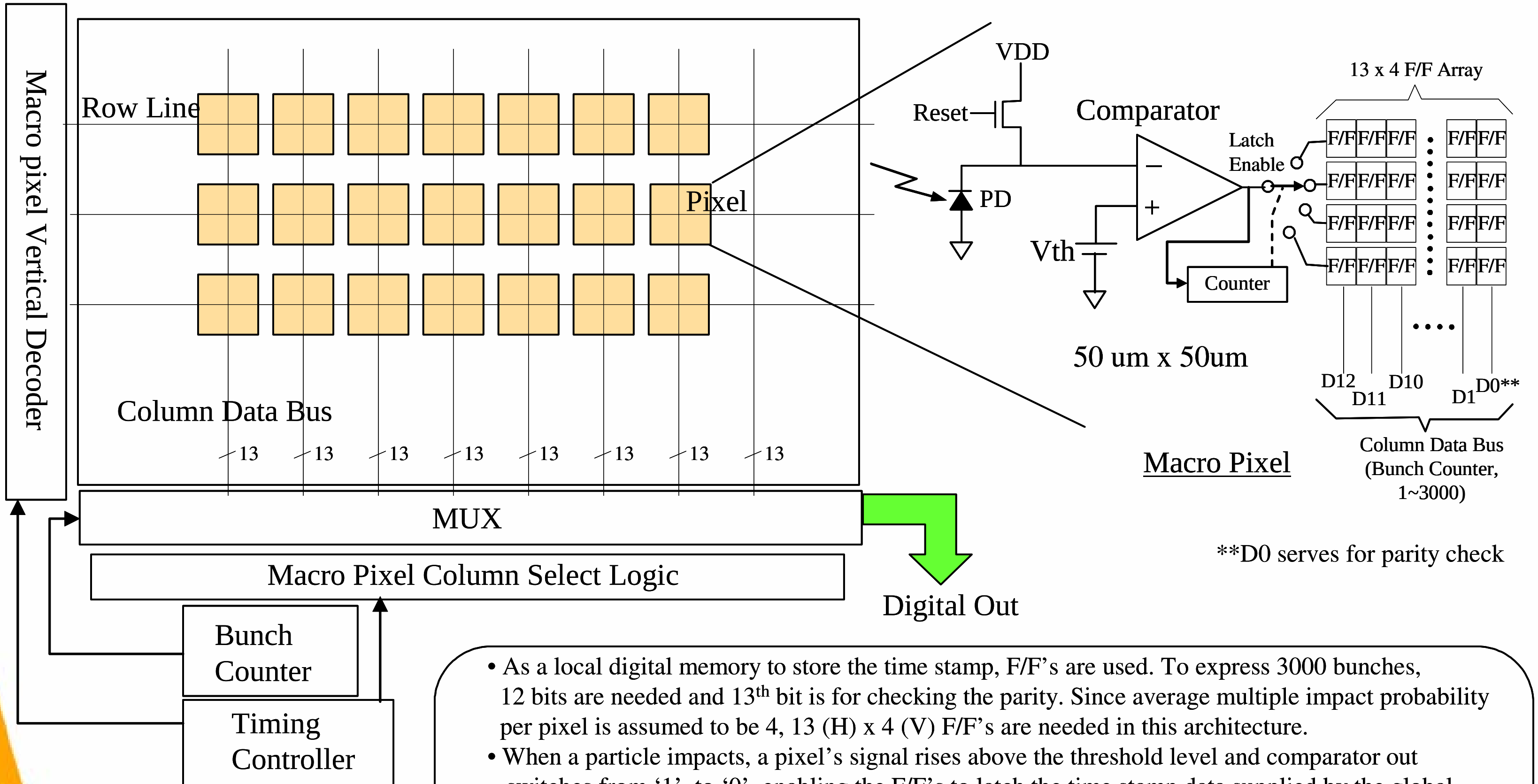
  (Probability of two hits in the same Small Pixel in a pulse train is $\lesssim$ 1%)

Hierarchical Array Operation (continued)

- Readout starts in the 200 msec gap after each train
  - x,y coordinates and intensity from Small Pixels that are hit, with time stamp from the corresponding Big Pixel
  - A small fraction of the hits will have ambiguity in time, i.e., more than one time stamp

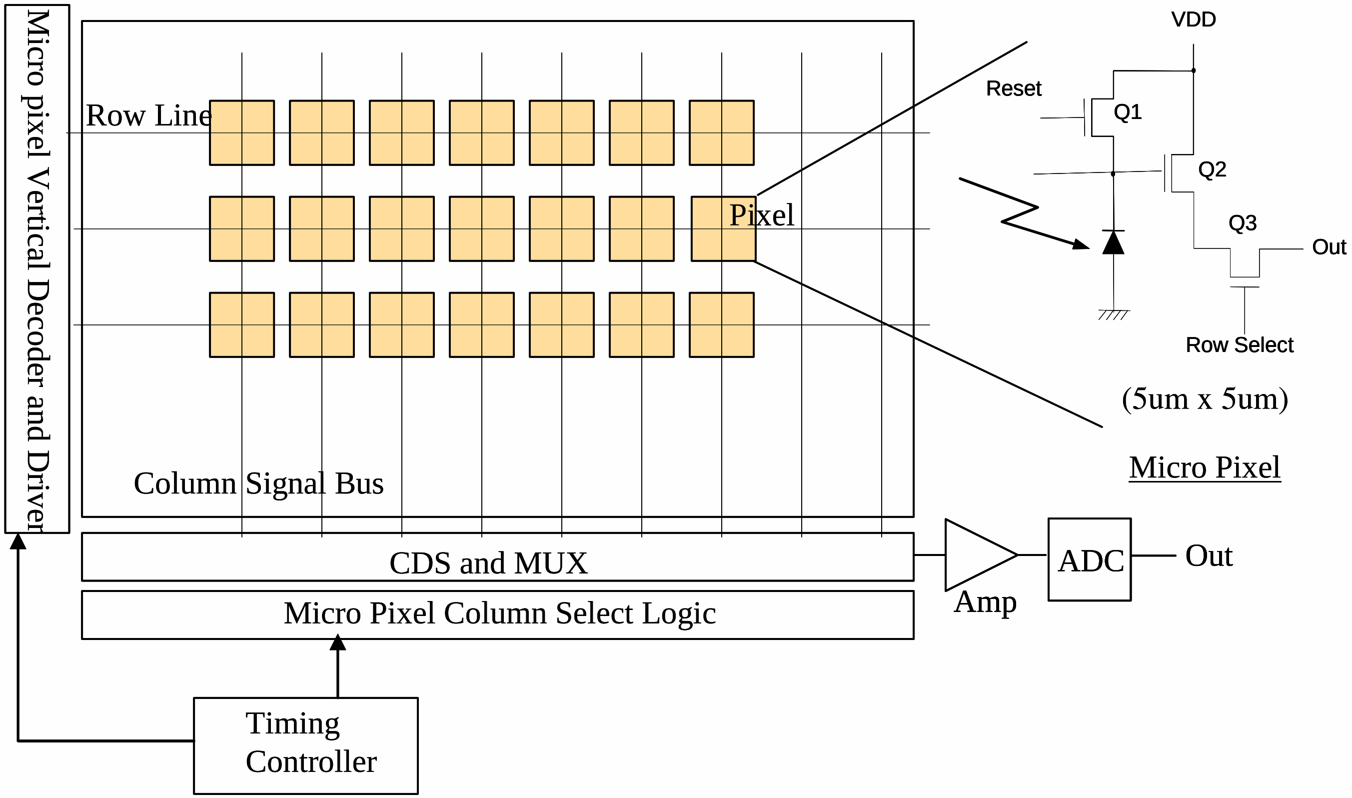
    (This will increase the occupancy by 30% above 10^{-6})
  - Both the Big Pixel and the Small Pixel arrays will be reset before the next pulse train

Macro Pixel Array Architecture



- As a local digital memory to store the time stamp, F/F's are used. To express 3000 bunches, 12 bits are needed and 13th bit is for checking the parity. Since average multiple impact probability per pixel is assumed to be 4, 13 (H) x 4 (V) F/F's are needed in this architecture.
- When a particle impacts, a pixel's signal rises above the threshold level and comparator out switches from '1' to '0', enabling the F/F's to latch the time stamp data supplied by the global bunch counter. When the data is latched, the pixel is reset.
- If next particle impacts the same location, comparator out enables next set of F/F's to preserve the previous time stamp data. This is implemented using a counter which increments the row address of the F/F array.
- Time stamp information is read out in the random access mode from the pixels of interest which stored nonzero time stamp data.

Micro Pixel Array Architecture



Expected Occupancy and Hit Rates

- Estimate for a typical 22 mm x 125 mm chip using 0.03 hits/mm^2/bunch crossing (this is conservative for the outer layers). Assume that each hit will put charge above threshold into, on the average, 3 Small Pixels.
- Each chip will have

  22 mm x 125 mm = 2750 mm^2

  1.1 x 10^6 Big Pixels

  1.1 x 10^8 Small Pixels
- Integrating over 2820 bunches in a pulse train we expect
  - 0.03 hits/mm^2/bunch x 2820 bunches ≈ 85 hits/mm^2
  - ~ 20% probability of a hit in a Big Pixel

    (~ 4% probability of 2 hits, 0.8% 3 hits, 0.16% 4 hits)
  - 6 x 10^{-3} occupancy in Small Pixels per pulse train

    2 x 10^{-6} occupancy in Small Pixels per bunch crossing
    - Effective Occupancy ~ 2 x 10^{-6}!!
  - Total number of hits per 22 mm x 125 mm chip

    7 x 10^5 Small Pixel hits/pulse train
  - Readout time 7 x 10^5 hits/25 MHz ~ 28 msec + some overhead

Other Comments & Issues

1. Thickness

   Present state of the art is 100 to 200 μ total thickness for the sum of the Macro and Micro Arrays. Could improve with some R&D to maybe 50 μ.

2. Power Consumption

   Present estimate 1.8 watts/chip could improve with R&D.

3. Fabrication Issues – two possible approaches
   a) Both Macro and Micro Pixel Arrays fabbed in a single process on the same piece of silicon.
   b) Macro and Micro Pixel Arrays fabbed in separate processes, then bonded together. No electrical connections needed between Macro and Micro Pixels in active area of detector – all connections are at one end of the chip.

4. Stitching

   Present layout tooling allow 21 mm x 21 mm devices – will have to learn how to "stitch" these areas together to make our size devices. They don't think this is a problem but they have not actually done it yet in CMOS process.

5. First Prototype
   a) The first prototypes will probably be 5 mm x 5 mm devices with the readout logic on a separate chip.
   b) In the final 22 mm x 125 mm active area device the readout logic can be on the same chip, at one end, making the actual device 22 mm x 130 mm long. Output connections will be at one end (away from interaction point).

Statement of work

Task-1 : Design and layout the micropixel (Sarnoff)

Task-2 : Design and layout the macropixel (Sarnoff)

Task-3 : Fabricate the test chips using MOSIS shuttle (Sarnoff)

Task-4 : Particle bombardment on test chip (Yale/Oregon)

Task-5 : Perform testing on test chip (Yale/Oregon w/ consulting from Sarnoff)

Task-6 : Summarize data (Yale/Oregon/Sarnoff)

Task-7 : Write report (Yale/Oregon/Sarnoff)

Program Plan

ID		Task Name
1		Micropixel design and layout
2		Macropixel design and layout
3		MOSIS test run
4		Particle bombardment on test chips
5		Testing of chips
6		Summarize test date
7		Write report