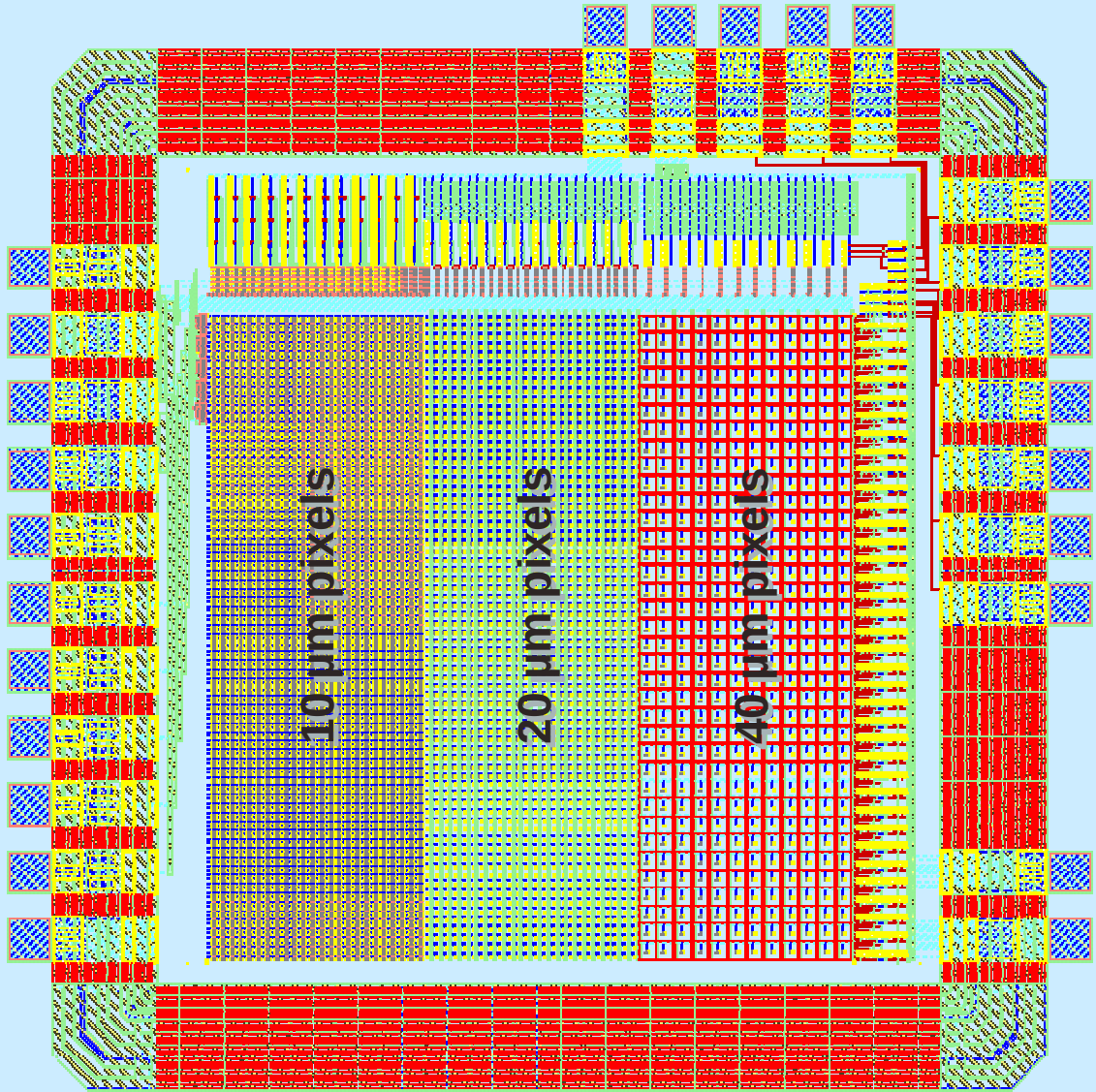
Activities supporting ILC at LBNL

- Leverage R&D in other areas to support LC
  - *CMOS Active Pixels*
  - *Column Parallel CCDs*
- APS
  - *Plans*
- CCDs

Simple Test Chip

- AMS 0.35 µm OPTO process
  - *Thicker epi*
  - *lower leakage:*
    - *CMOS 10,000 pA/cm²*
    - *OPTO 45 pA/cm²*

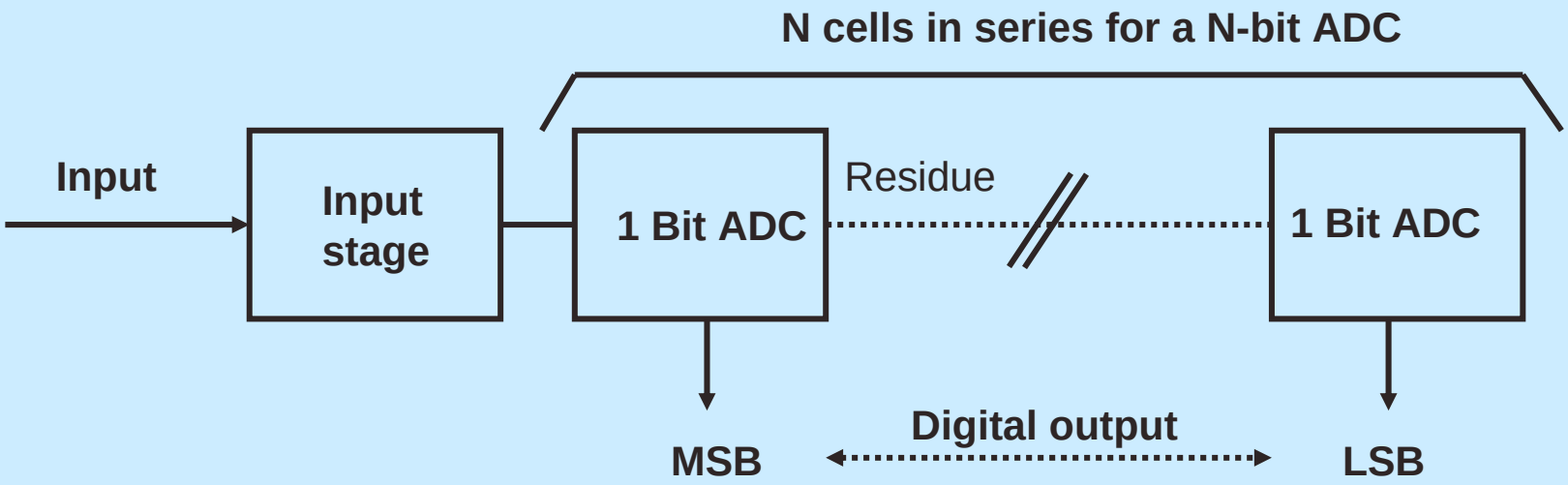
- 1st MOSIS run (some "issues")
- Analog outputs only
- Just arrived...



Next steps

- Have APS with on-chip ADC and in-pixel CDS for electron microscopy (described tomorrow)
  - *10-bit Wilkinson on 19 µm pitch in 0.25 µm TSMC*
  - *4-5 bit Wilkinson marginal (speed) for LC*
- Develop 4-5 bit pipelined ADC
  - *Based on SNAP design*
  - *Prototype in 0.35 µm AMS OPTO or 0.18 µm AMS OPTO (if available)*

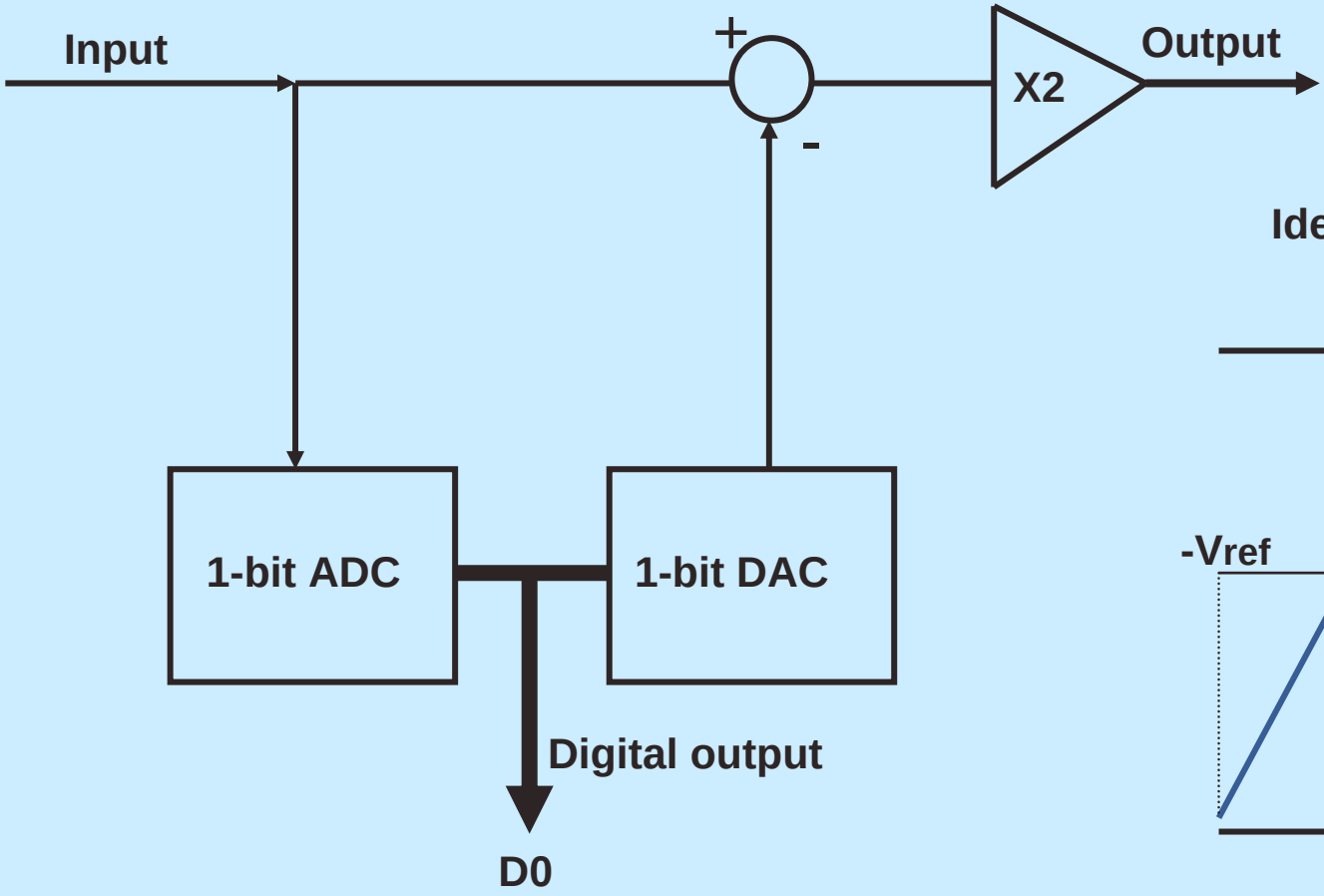
Pipelined ADC

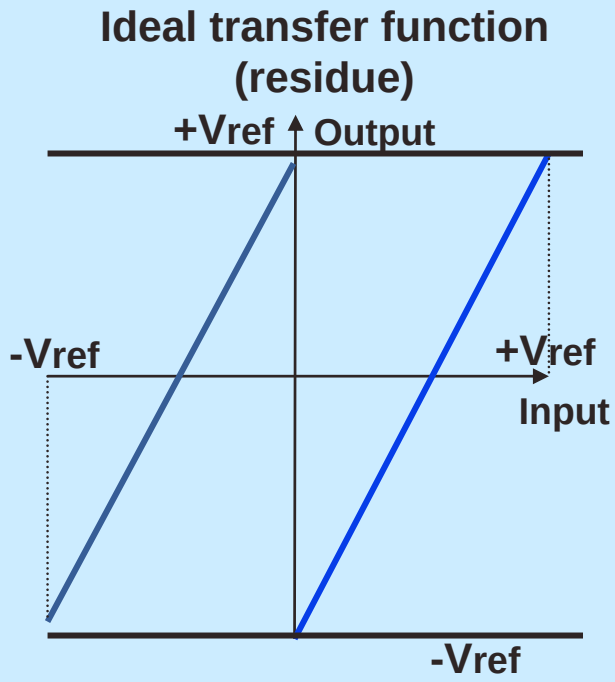


- Sub ranging architecture: Each stage determines one bit.
- The first stage residue is digitized by a (N-1) bit ADC and so on…
- Digitization rate = ADC clock frequency
- Latency = Digitization rate x number of bits / 2

From J-P Walder

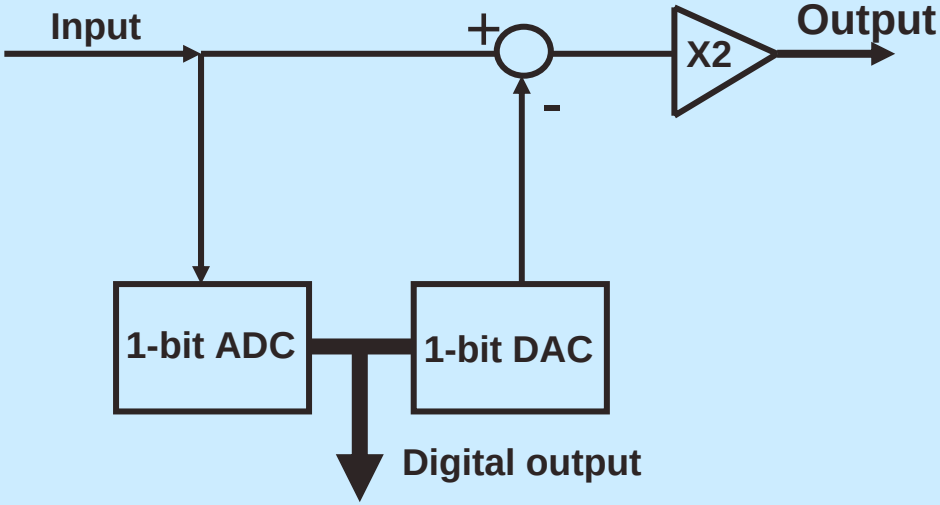
1-Bit Cell



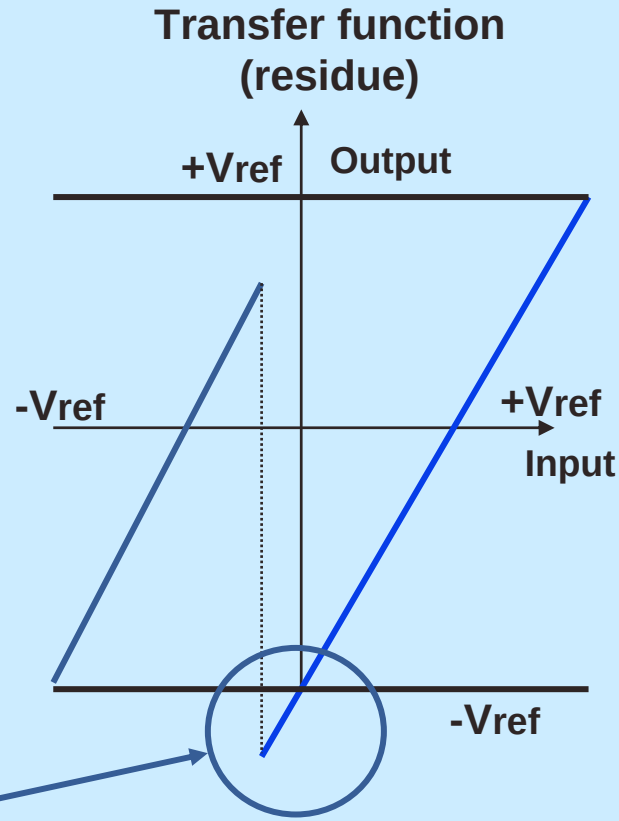


From J-P Walder

Limitation of the 1-Bit Cell



D0
0 → Vout = 2xVin + Vref
1 → Vout = 2xVin - Vref

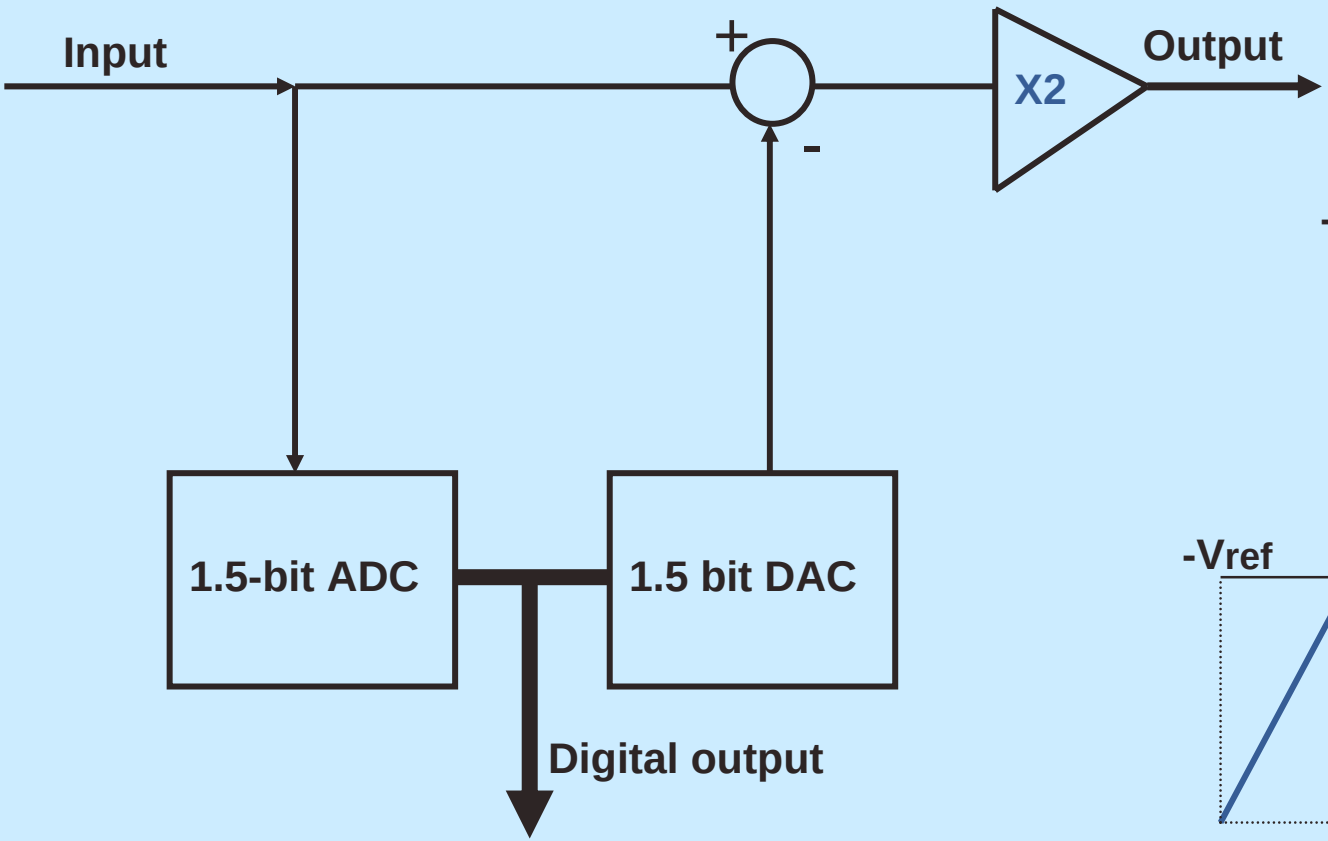


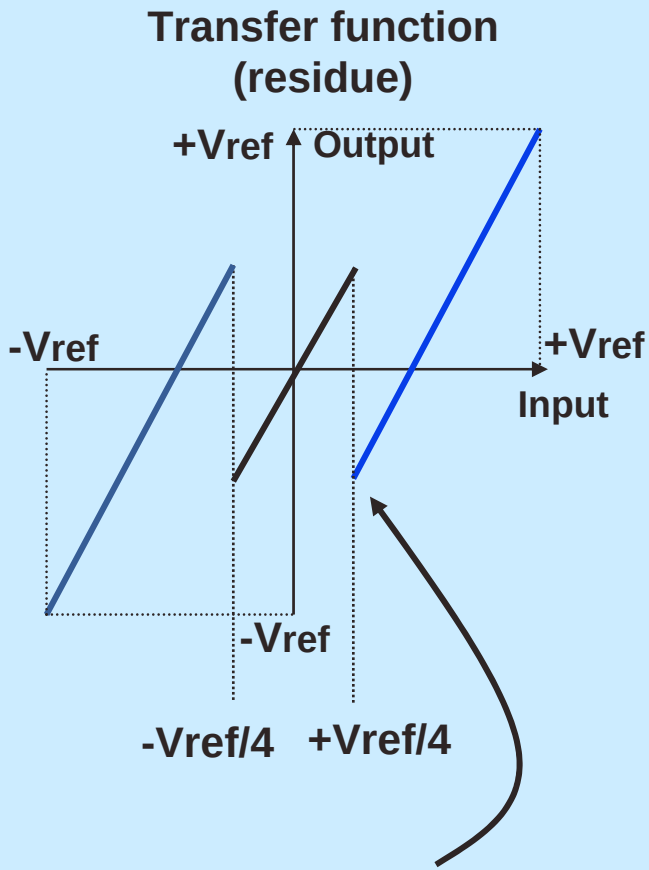
Missing codes due to comparator offset for example

Loss of information when the larger residues saturate the next stage. It could come from charge injection, capacitance mismatch or comparator offset.
Errors can be corrected by digital correction if the conversion range of the next stage is increased to handle the larger residues.

From J-P Walder

1.5-Bit Cell

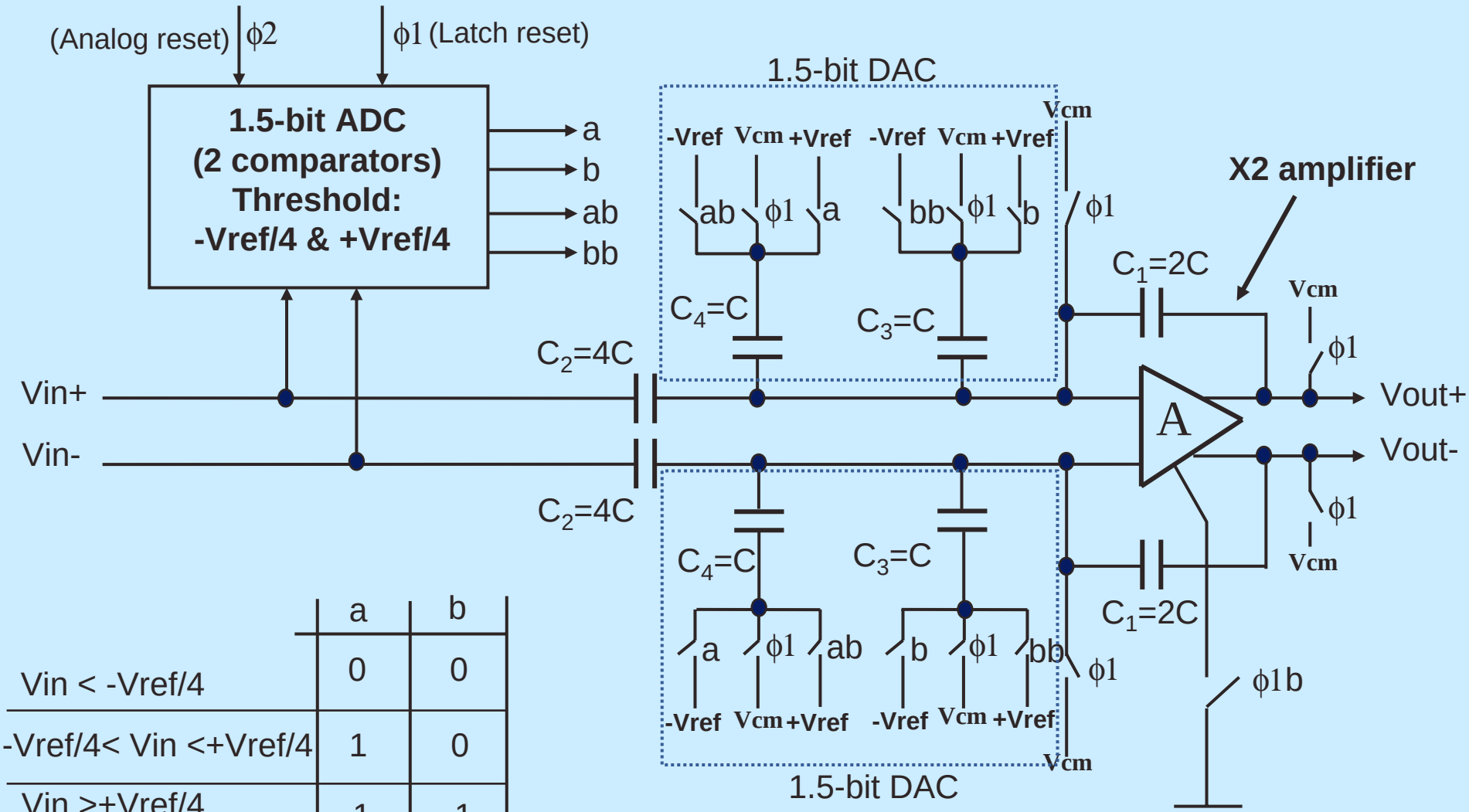




No saturation if +- Vref/4 is moving

From J-P Walder

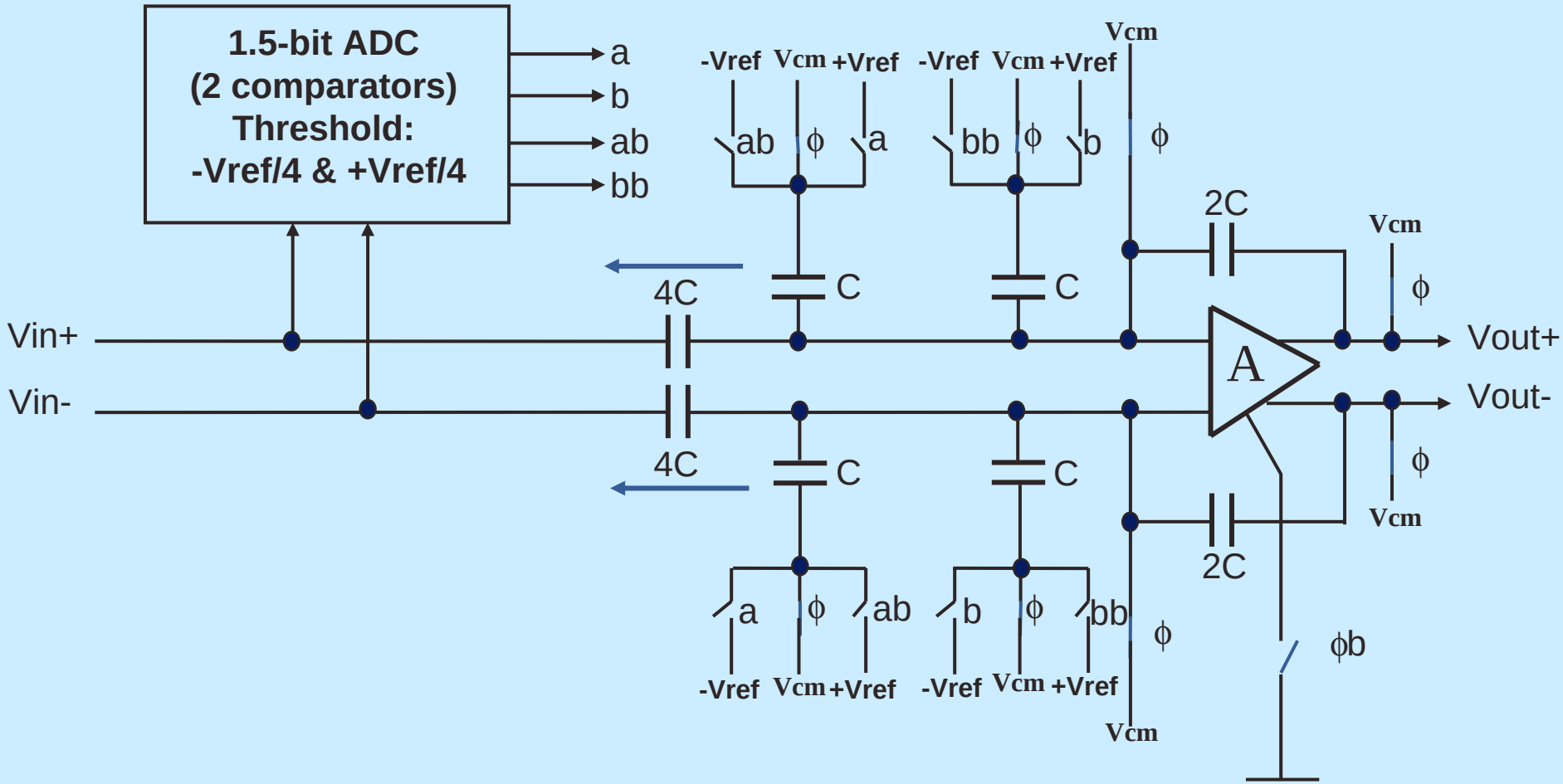
1.5-Bit Cell Implementation



	a	b
Vin < -Vref/4	0	0
-Vref/4< Vin <+Vref/4	1	0
Vin >+Vref/4	1	1

From J-P Walder

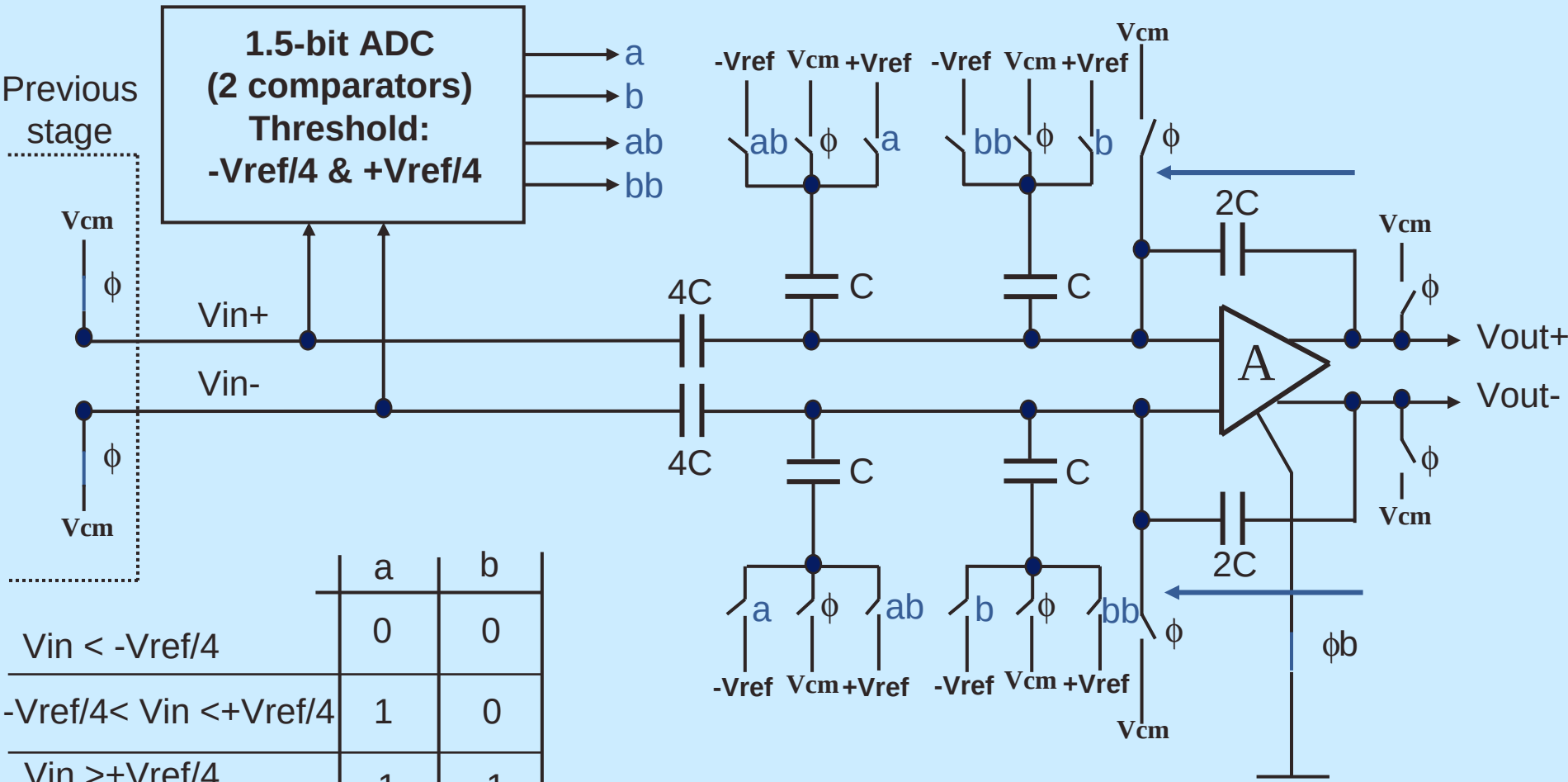
Sampling Phase



Input signal sampled on 4C

From J-P Walder

Amplification Phase



	a	b
Vin < -Vref/4	0	0
-Vref/4< Vin <+Vref/4	1	0
Vin >+Vref/4	1	1

Vout = 2xVin ±Vref/2 ±Vref/2

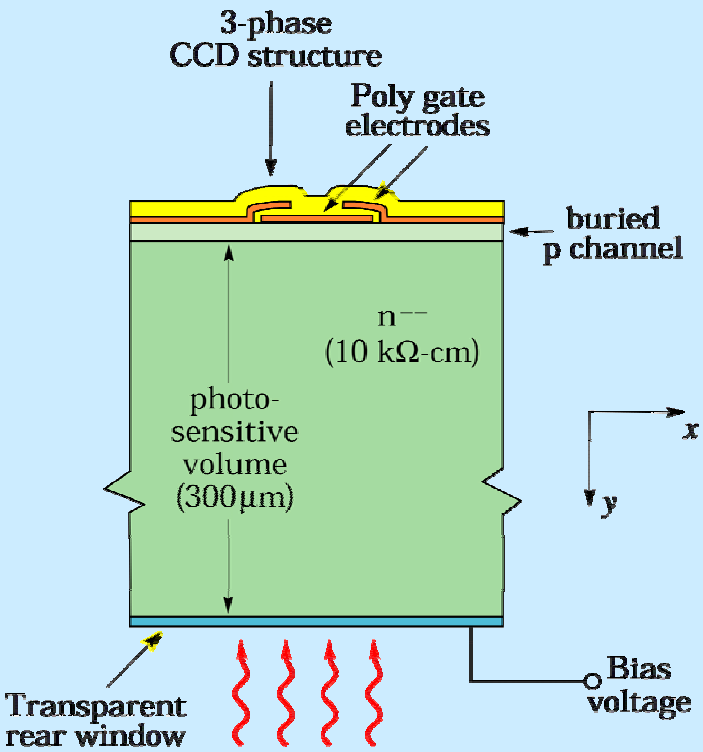
(DC gain infinite)

From J-P Walder

Advantage of On-Chip Pipelined ADC

- Precision
  - *Fixed by capacitor mismatch: higher precision $\Rightarrow$bigger capacitors (space).*
  - *LC needs low precision (~4 bits) $\Rightarrow$small size (targeting 20 µm layout pitch)*
- Speed
  - *Pipelined architecture means that **each stage** runs at f_{ADC}*
  - *Low precision $\Rightarrow f_{ADC} \geq$ 50 MHz feasible*
- Power
  - *(Most) of the current is to slew the caps to the required precision within τ_{ADC}*
  - *Low precision $\Rightarrow$low power (~1 mW or less)*

Also have activities on high-speed CCD

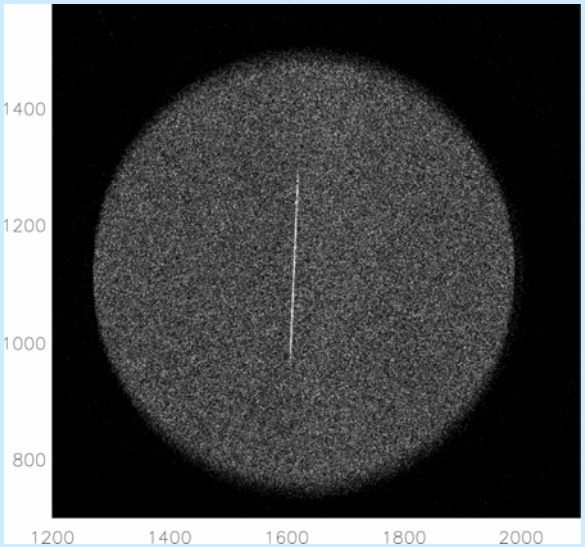


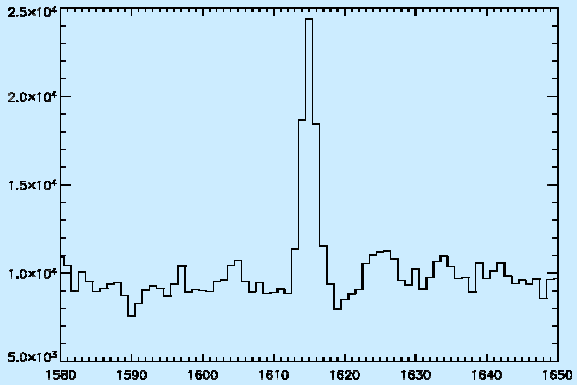
- Driven mostly by synchrotron radiation needs
- Makes use of LBL thick CCD
  - *Used in astrophysics*
- Leverages readout development for SNAP/JDEM
- Initial goal – 1 Mpix/s at ≥14 bits dynamic range, 100-200 fps

CCDs for Synchrotron Applications

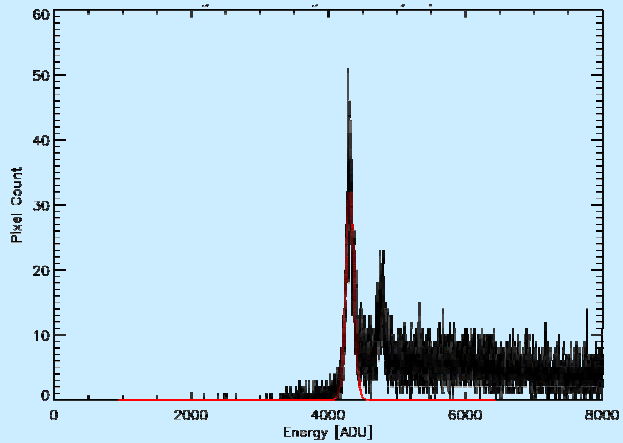
1. high speed (optical) photon readout
2. x-ray detection in thick CCDs

5 µm slit in (partially transparent) steel target

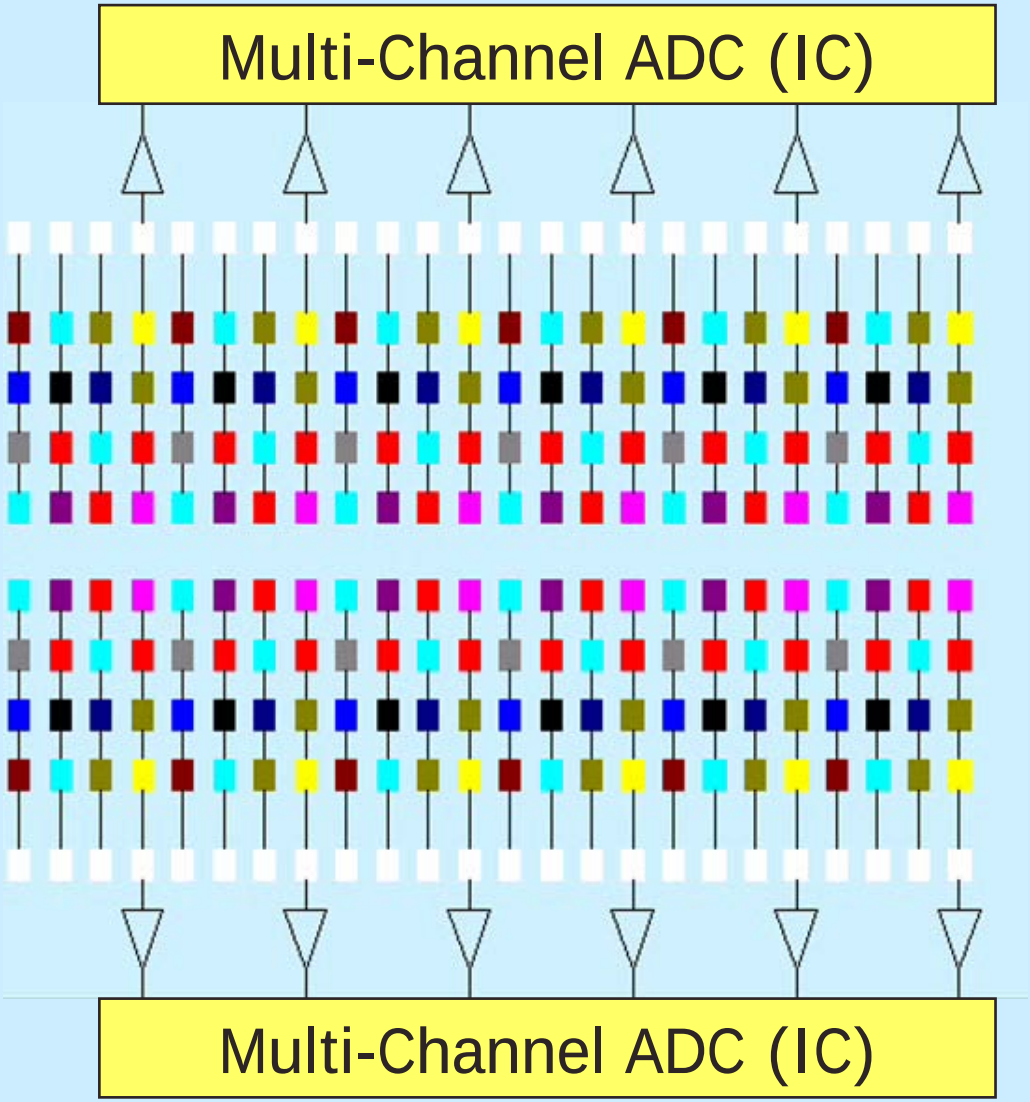




Cu K_α (8.0 keV) and K_β (8.9 keV) lines



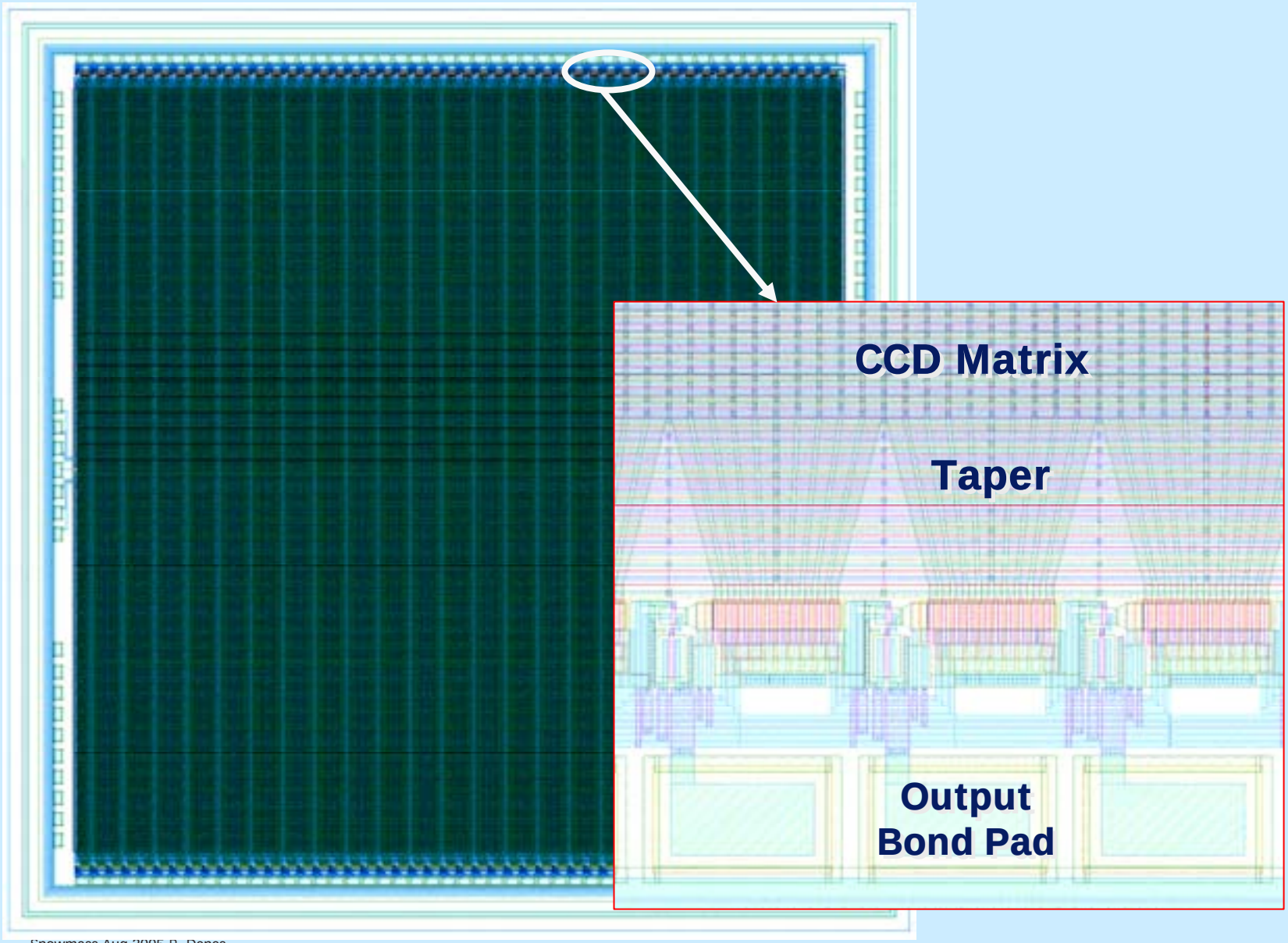
(almost) Column-Parallel CCDs



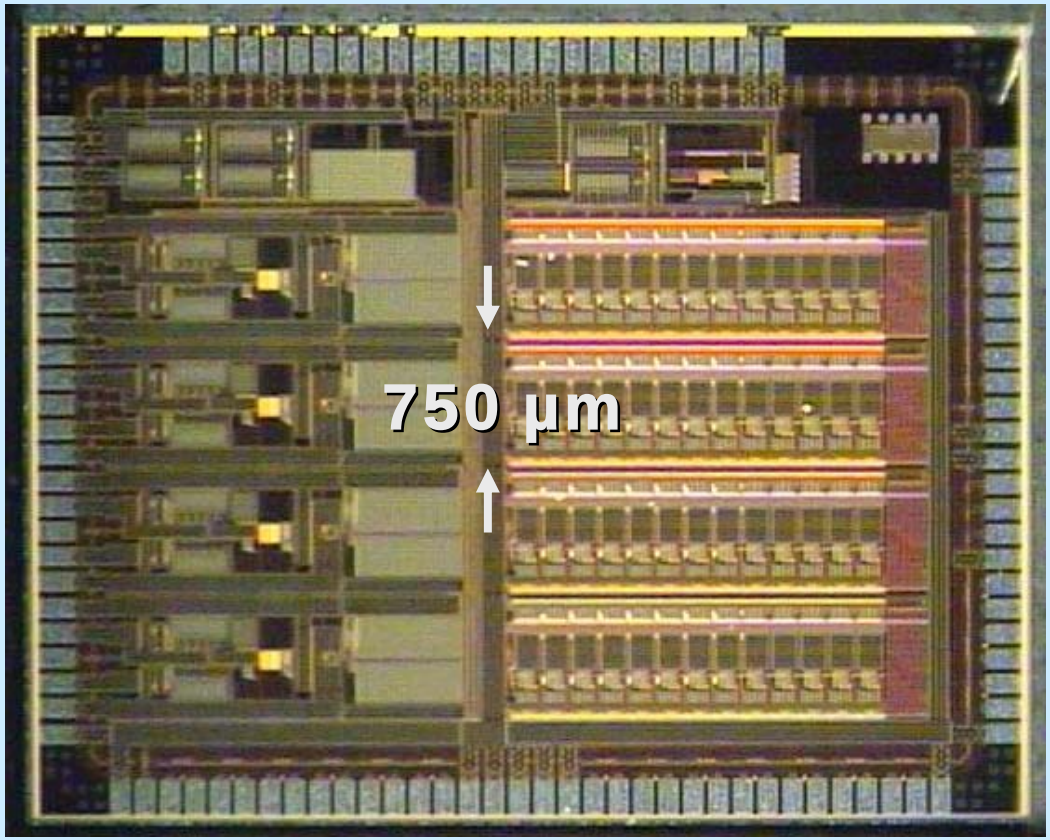
- parallelism $\Rightarrow$ factor of 100+ speed increase
- “almost” allows wire (rather than bump) bonding
- large dynamic range

- Uses LBNL CCD technology
- Based on IC developed by LBNL for SNAP readout

(Almost) Column Parallel CCD



SNAP Pipeline ADC



- 16-bit multi-slope front-end
  - *2 e^- noise at 100 kHz*
- 13-bit pipelined ADC
  - *INL < +/-1.5 LSB*
  - *DNL <+/-0.5 LSB*
- 10 mW/channel
- Space qualified
- 4 channels/chip

Currently making 16-channel version
1 MHz rate, 300 µm bonding pitch

Summary

- Relatively recent start on APS
  - *On-going developments*
  - *Pipelined ADC*
- CCDs
  - *(a) CPCCD for wide dynamic range*
  - *possibly at low-precision, high-speed CPCCDs for certain synchrotron experiments (might be good match for LC)*