Belle Pixel Detector Upgrade

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ILC Workshop @ Snowmass
19 AUG 05

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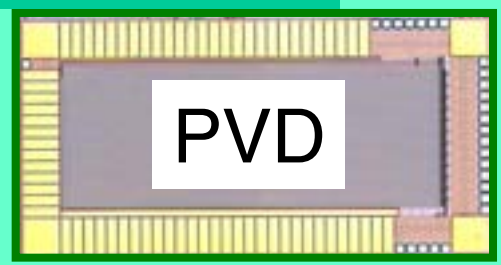
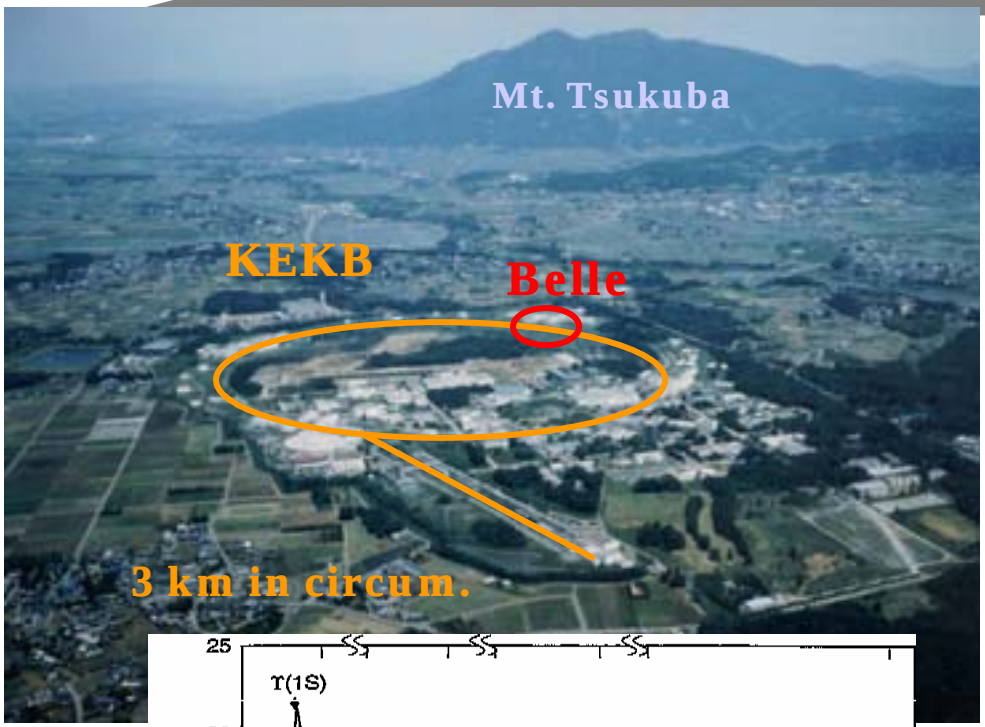


KEK-B asymmetric collider

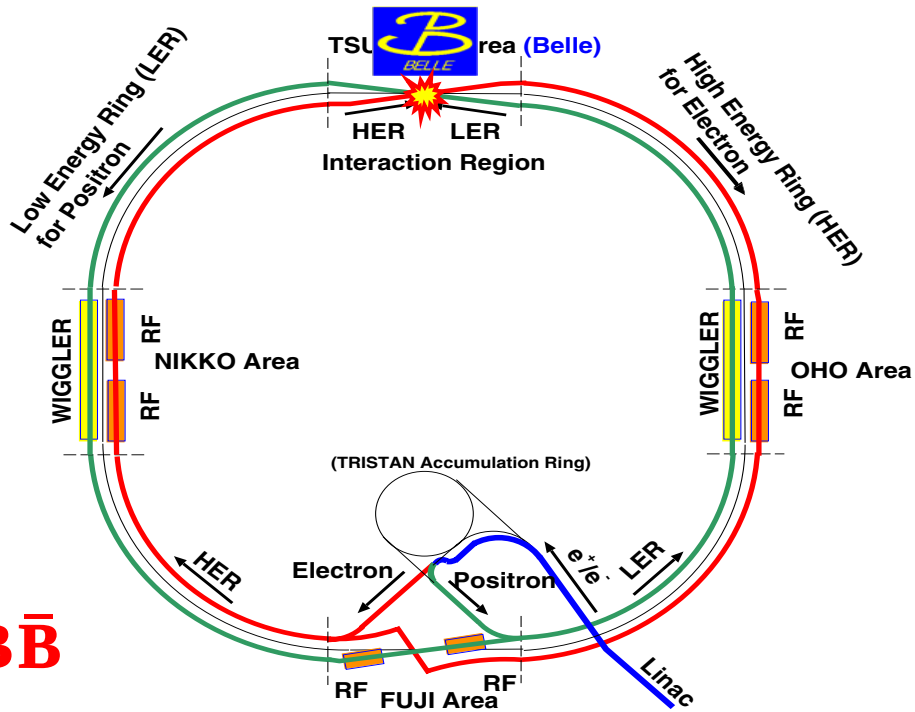


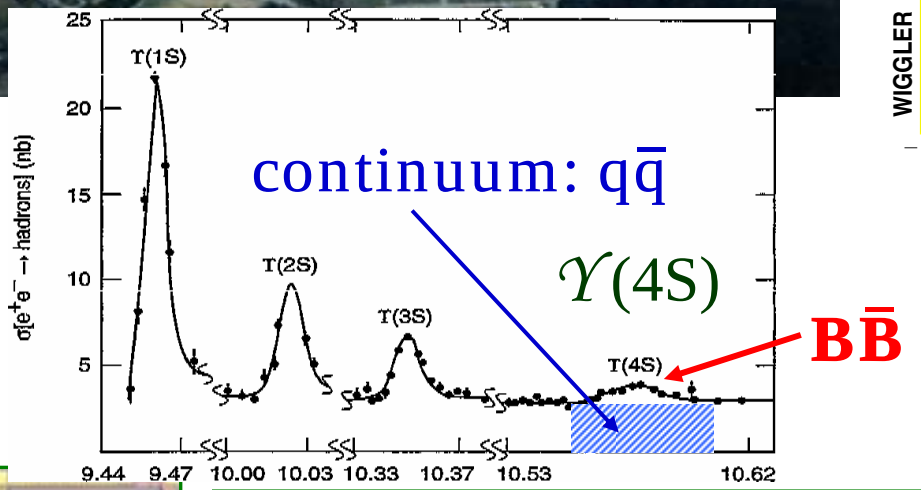
KEKB / Belle started operation in 1999

8 GeV e^- x 3.5 GeV e^+

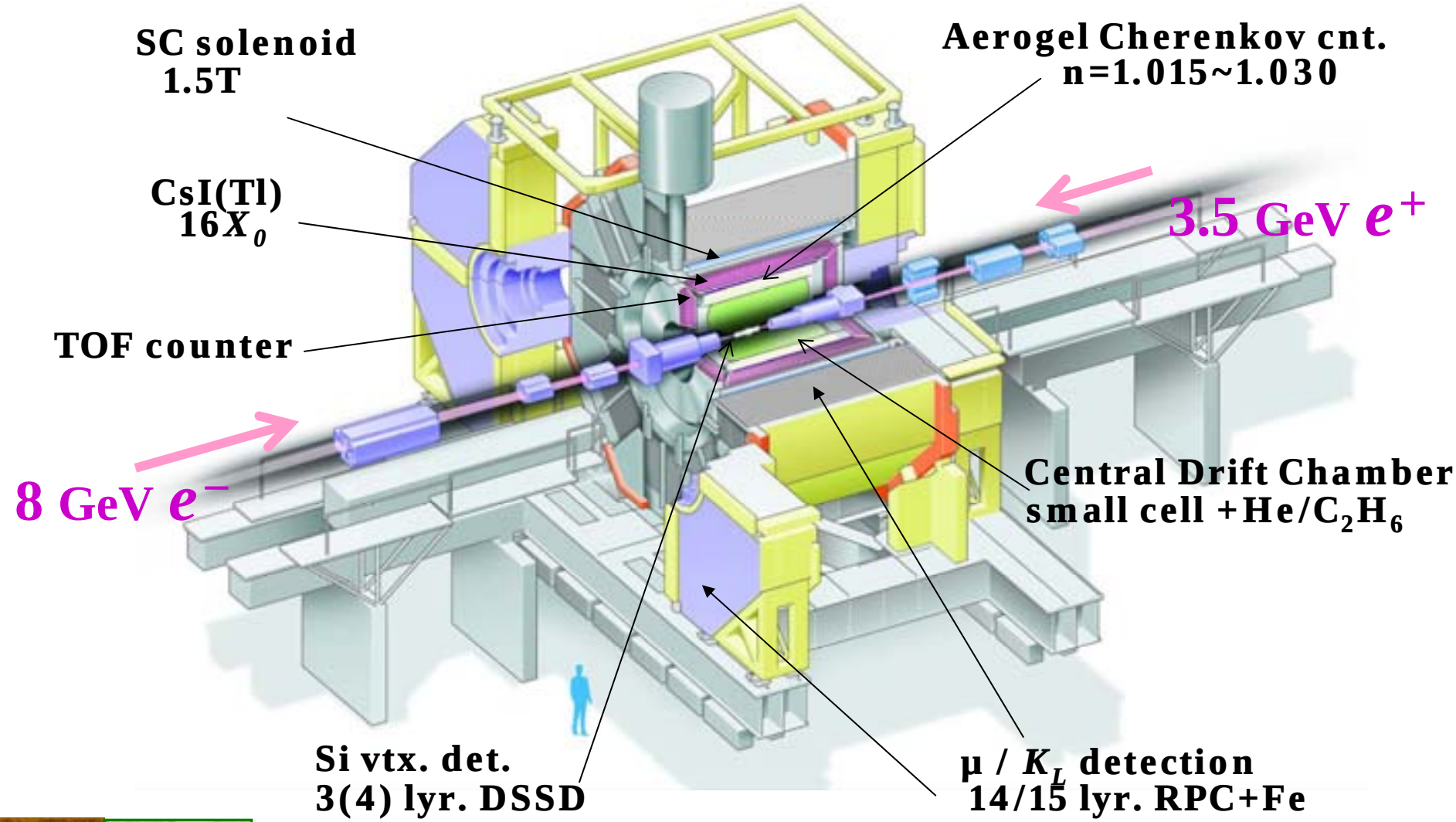
$B\bar{B}$ boost !

±11mrad crossing

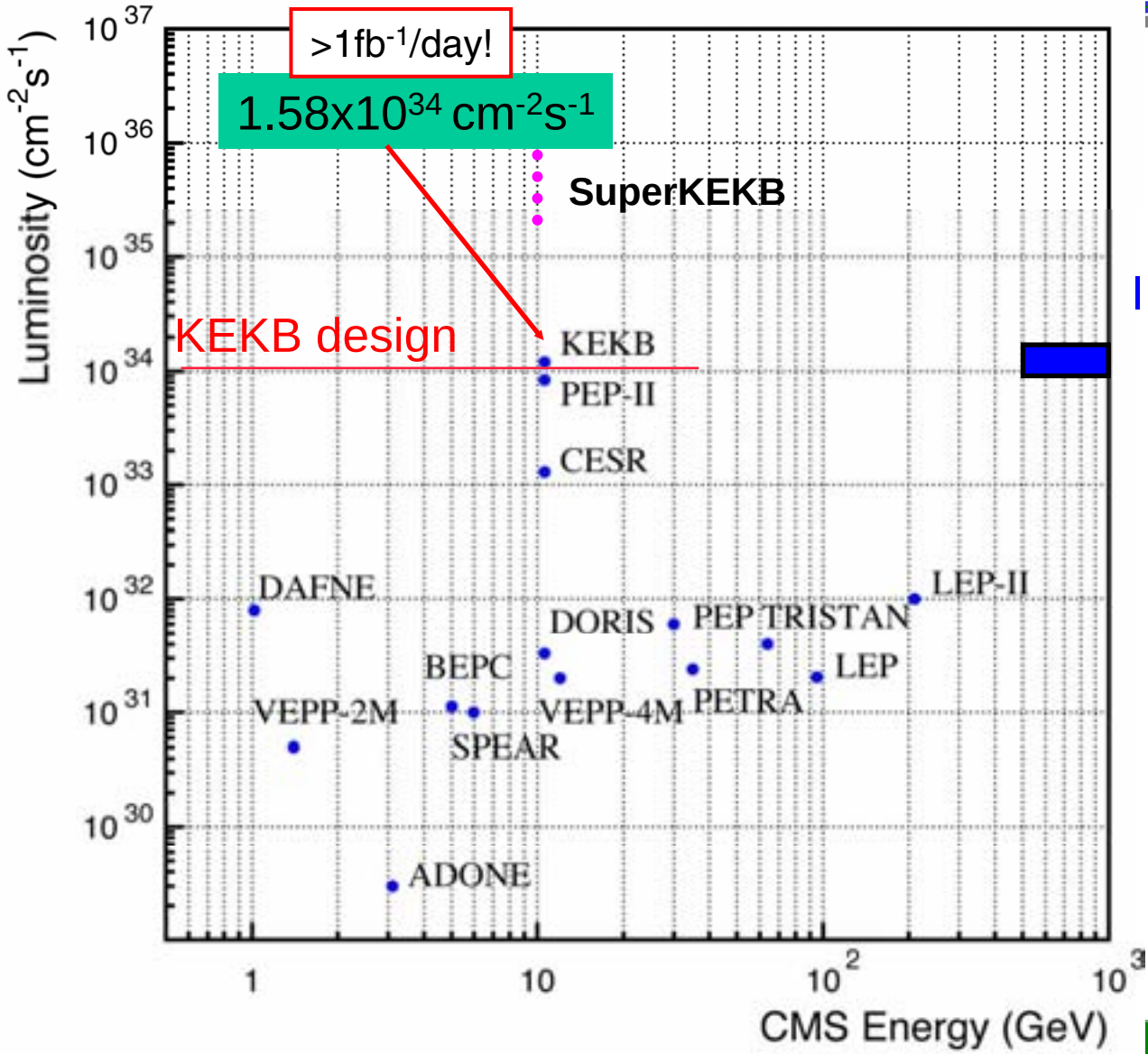




BELLE detector at KEKB

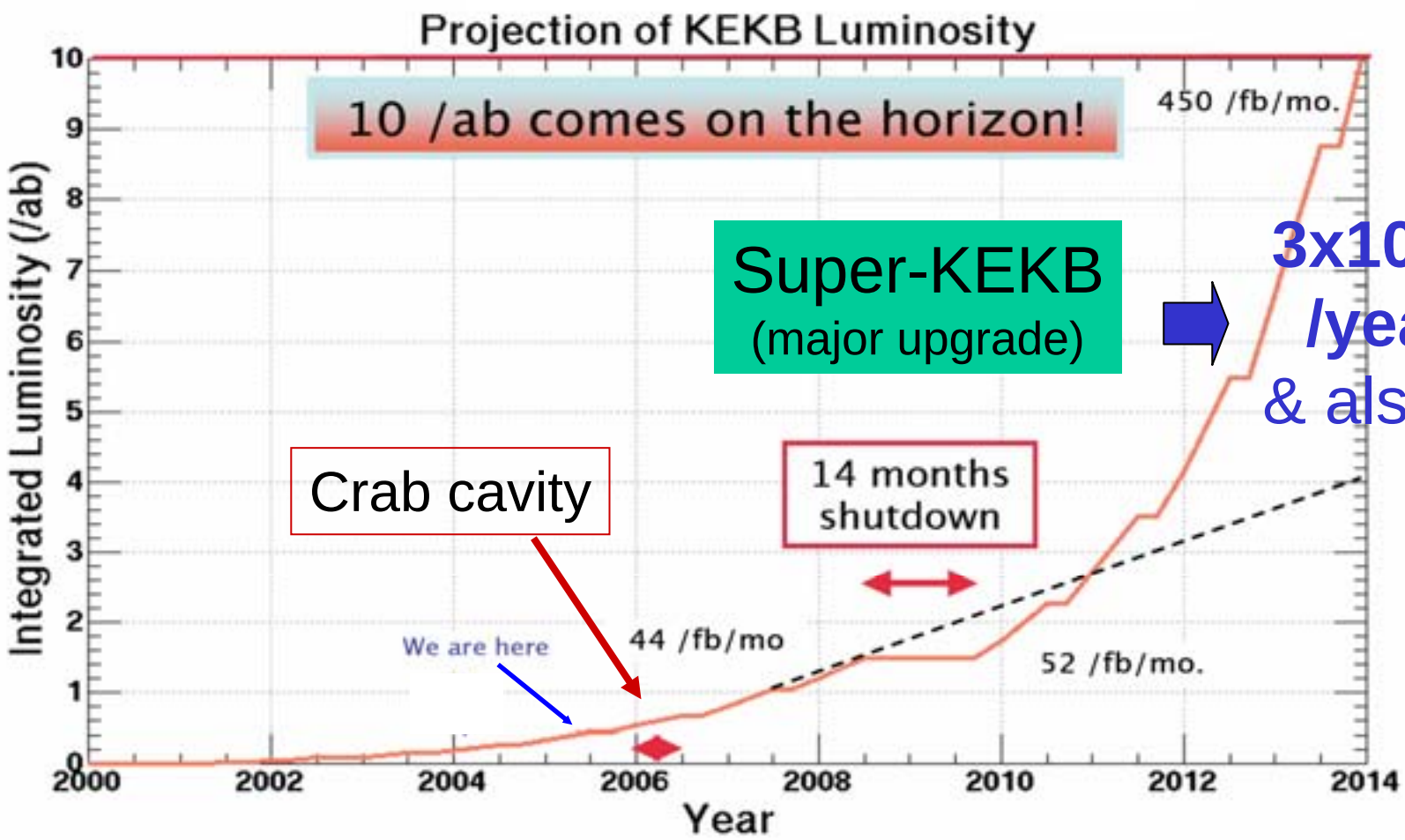


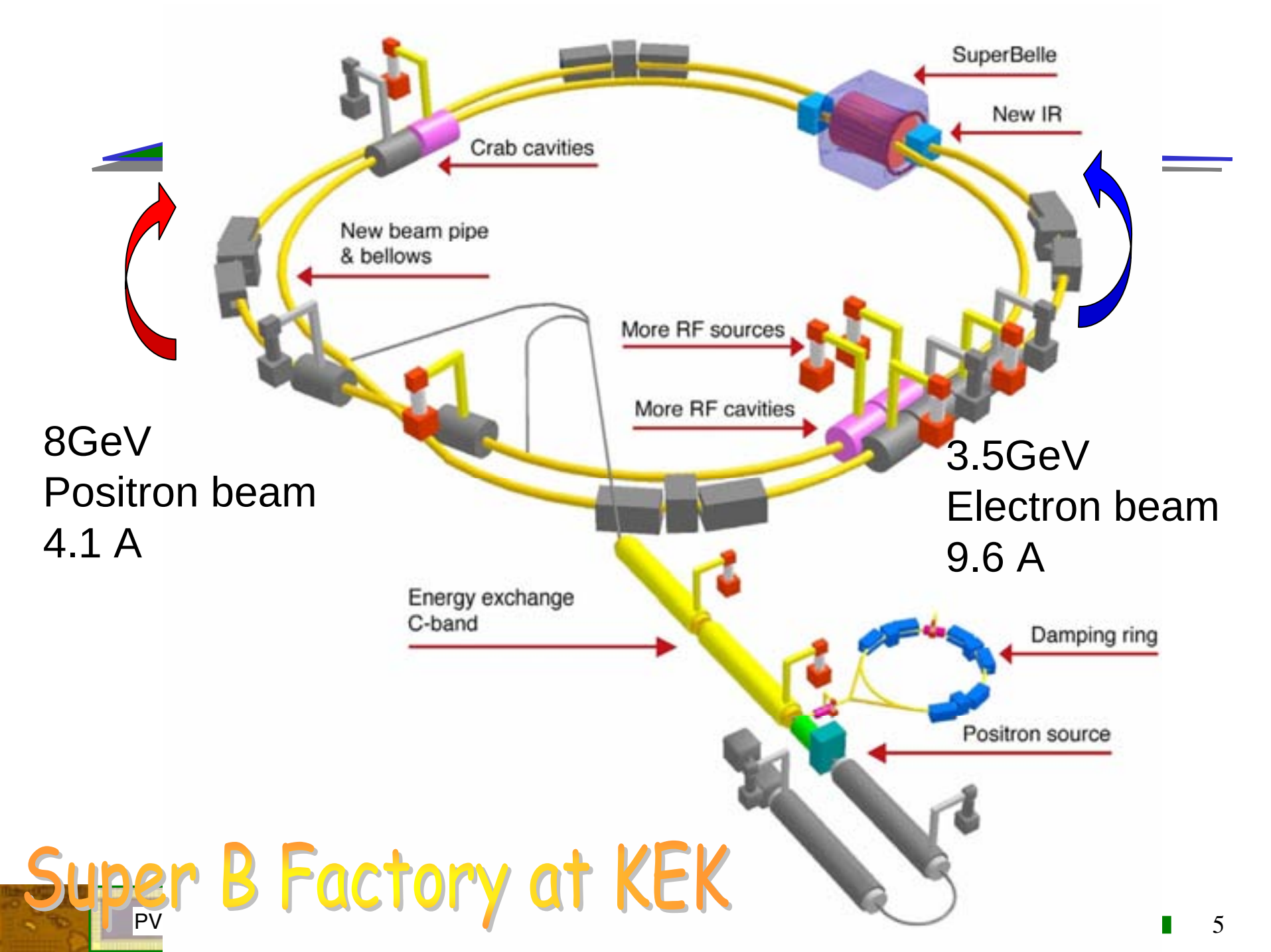
Luminosity goal



KEKB Upgrade Scenario

L_{peak} ($cm^{-2}s^{-1}$)	1.58×10^{34}	5×10^{34}	5×10^{35}
L_{int}	467 fb^{-1}	1 ab^{-1}	10 ab^{-1}





8GeV
Positron beam
4.1 A

3.5GeV
Electron beam
9.6 A

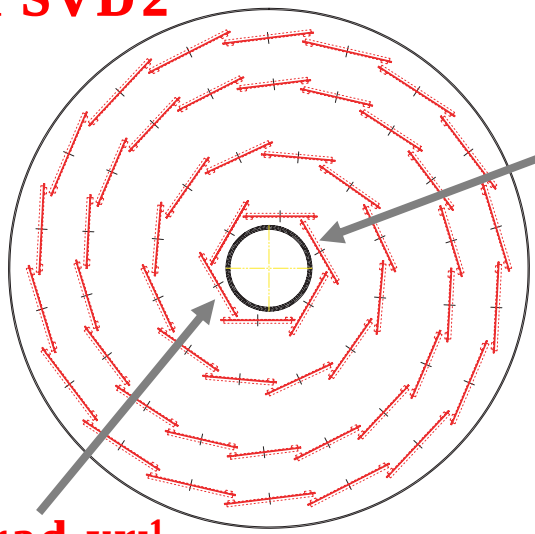
Super B Factory at KEK

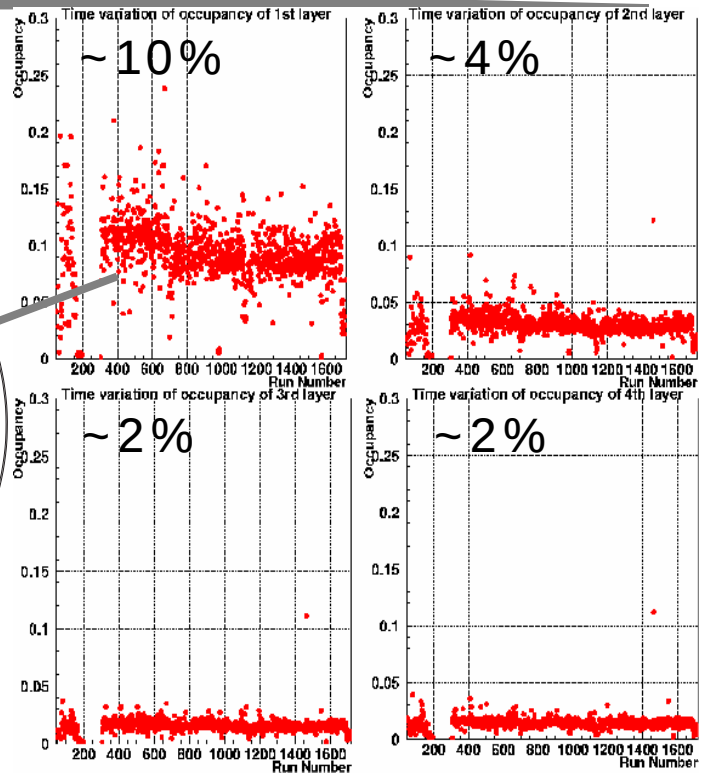
Why bother with a Pixel Detector?

- Occupancy
  - Current SVD simply won't work @ higher Luminosity (instigating progress)
- Improved vertexing (already a Super-B Factory)
  - e.g. better continuum suppression → improve background systematics limited analyses
- Be competetive (aggressive)
  - To remain viable, continue to look for ways to **exploit** B-factory benefits

Occupancy in SVD2

152M $B\bar{B}$ pairs with SVD1
+ ~300M $B\bar{B}$ pairs with SVD2





Present : layer 1 of SVD

~10% occupancy / 200 Krad.yr^{-1}

Upgrade: **L~1.5x10^{34} → L~5x10^{35} cm^{-2}.s^{-1}**

Background increase typ. x20(?! x50?) → Occupancy / dose

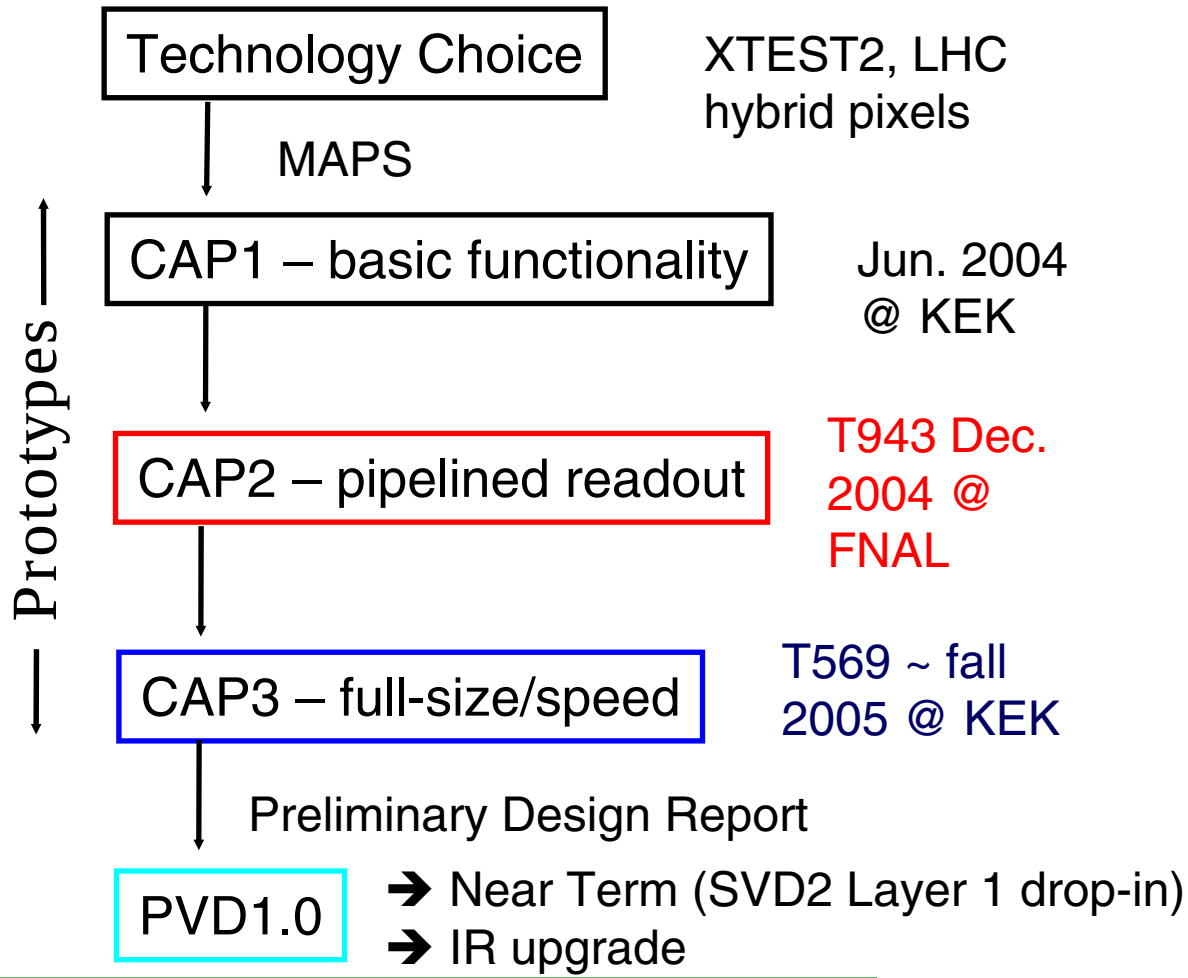
Conventional solutions (Si strips) do not work → Striplet (SVD2.5)

Pixel type sensor – a natural choice

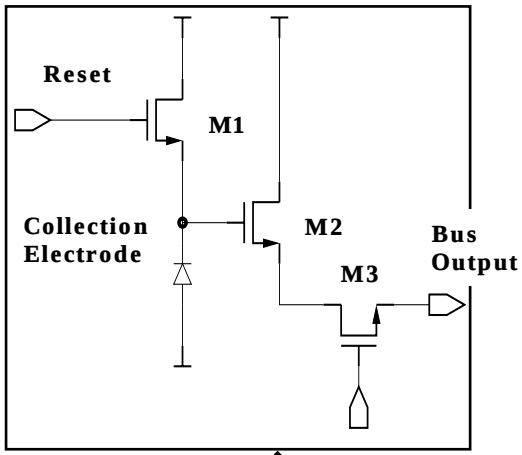
Requirements

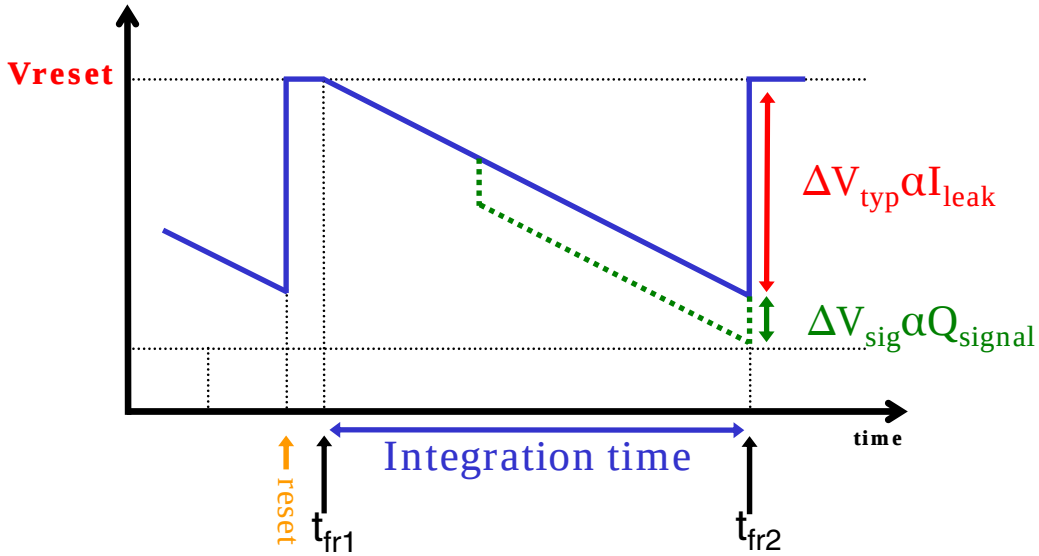
1. Low occupancy
2. Fast Readout Speed
3. Radiation Hardness
4. Thin Sensor
5. Full-sized detector

R&D steps



Continuous Acquisition Pixel (CAP)





Pixel

Array of 132x48 pixels

High-speed

ADC

analog

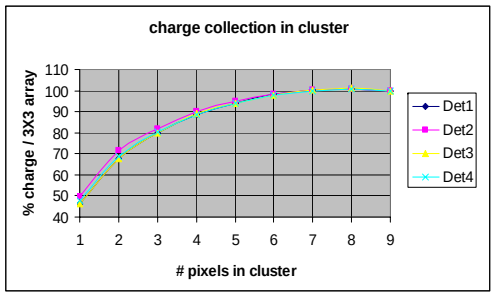
& storage

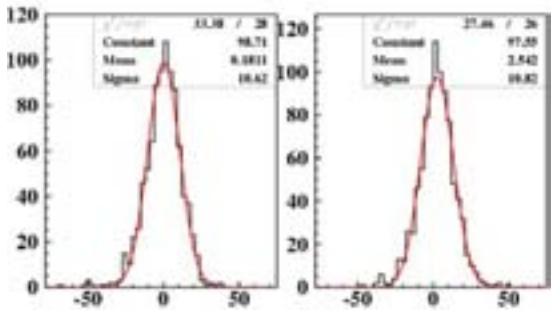
Pixel Array: Column select – ganged row read

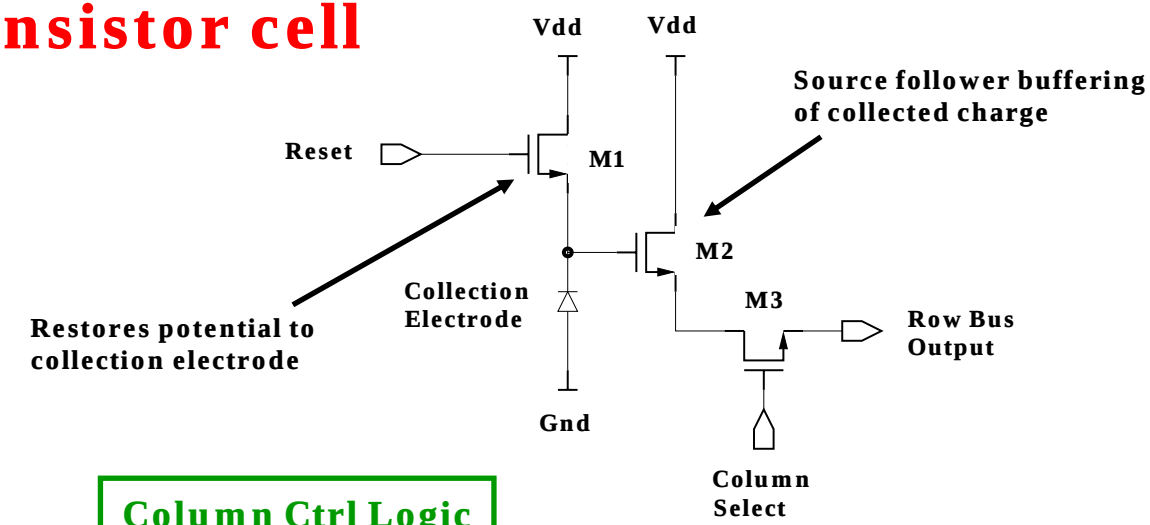
Low power – only significant draw at readout edge

Cont. Acq. Pixels (CAP) 1 Prototype

CAP1: simple 3-transistor cell



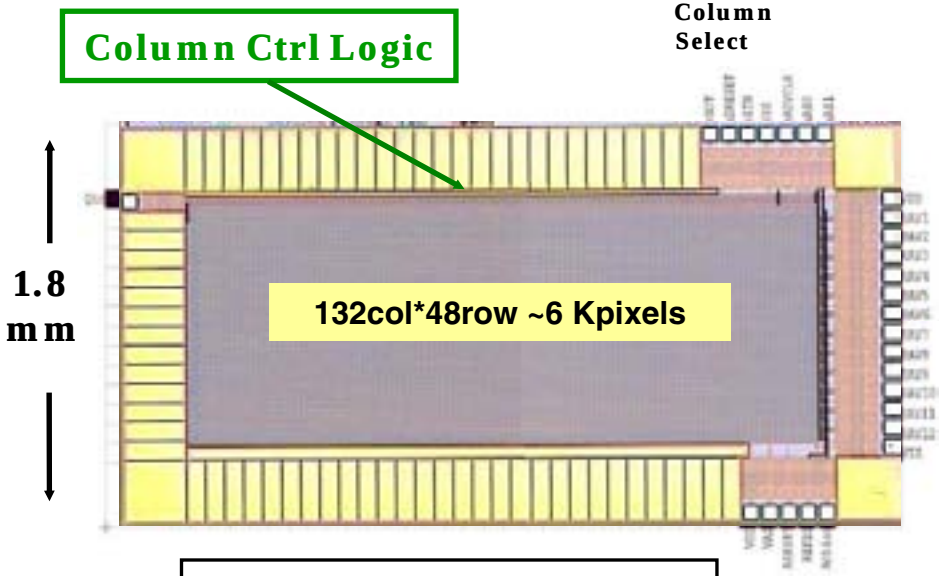




Pixel size:

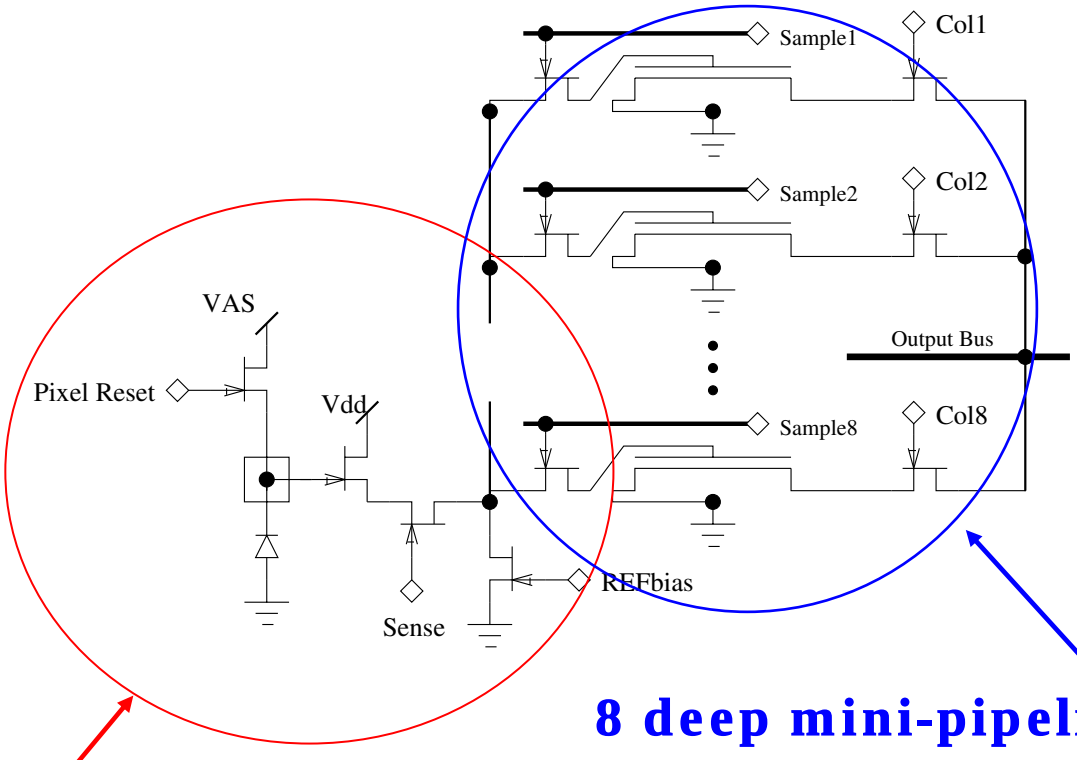
22.5 μm x 22.5 μm

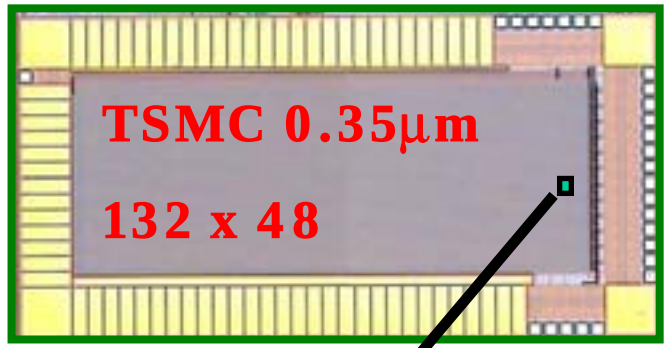
CAPs sample tested: all detectors (>15) function.

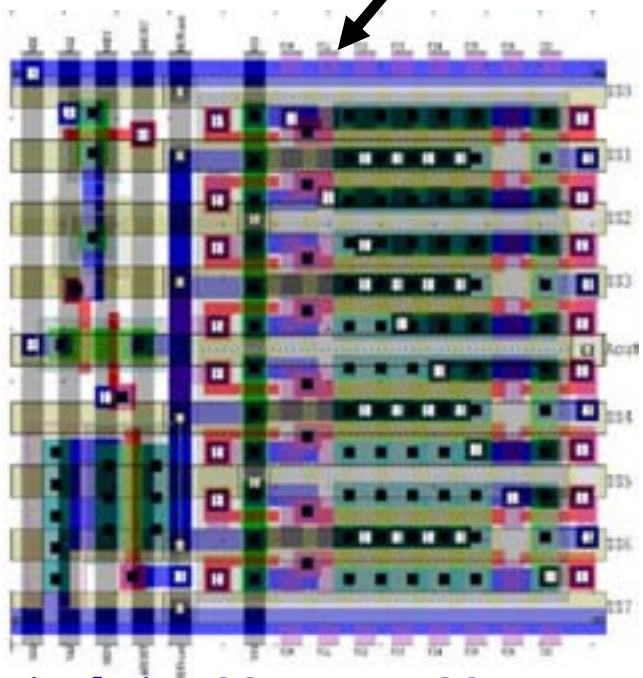


NIM A541:166-171 (2005)

CAP2 – Pipelined operation







Pixel size 22.5 µm x 22.5 µm

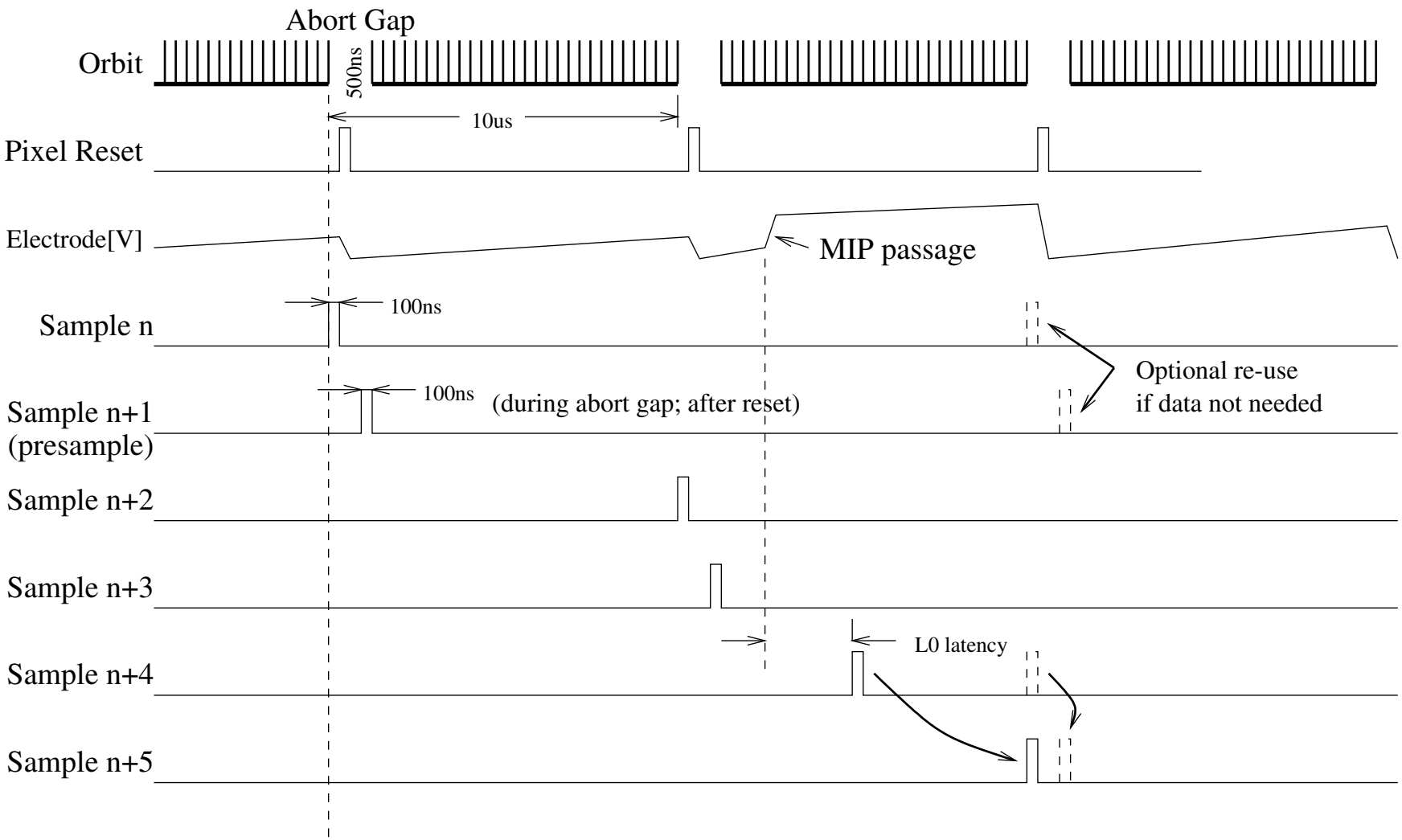
3-transistor cell

8 deep mini-pipeline in each cell

132x48=6336 channels 50688 samples

10µs frame acquisition speed achieved!

Tune for machine operation

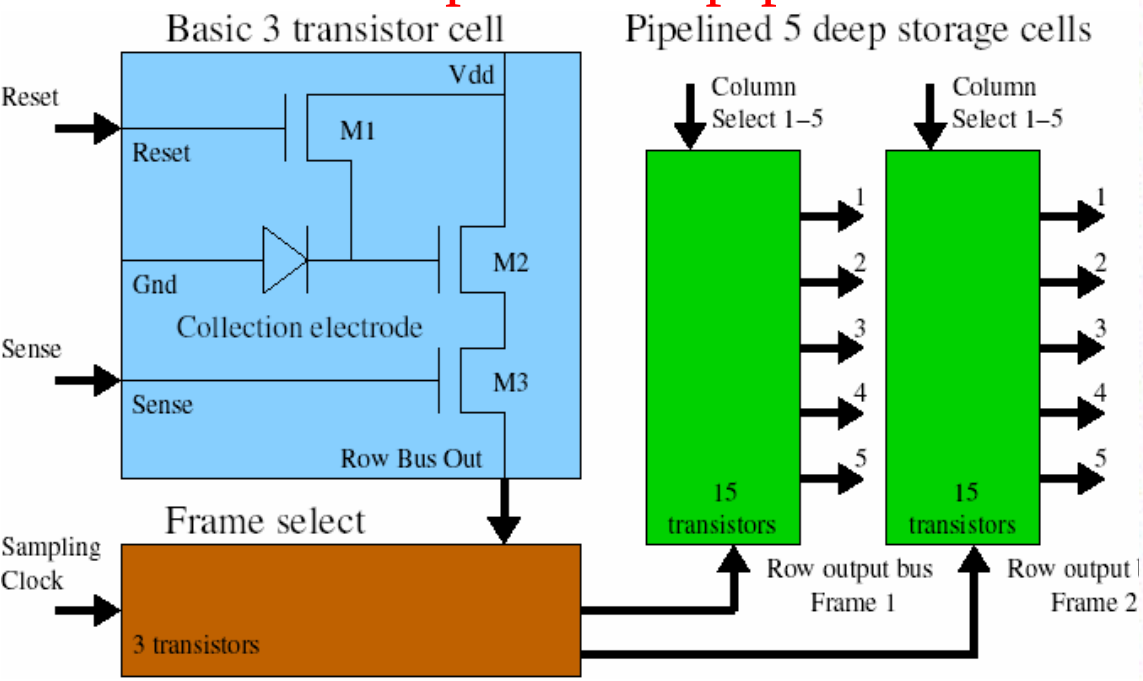


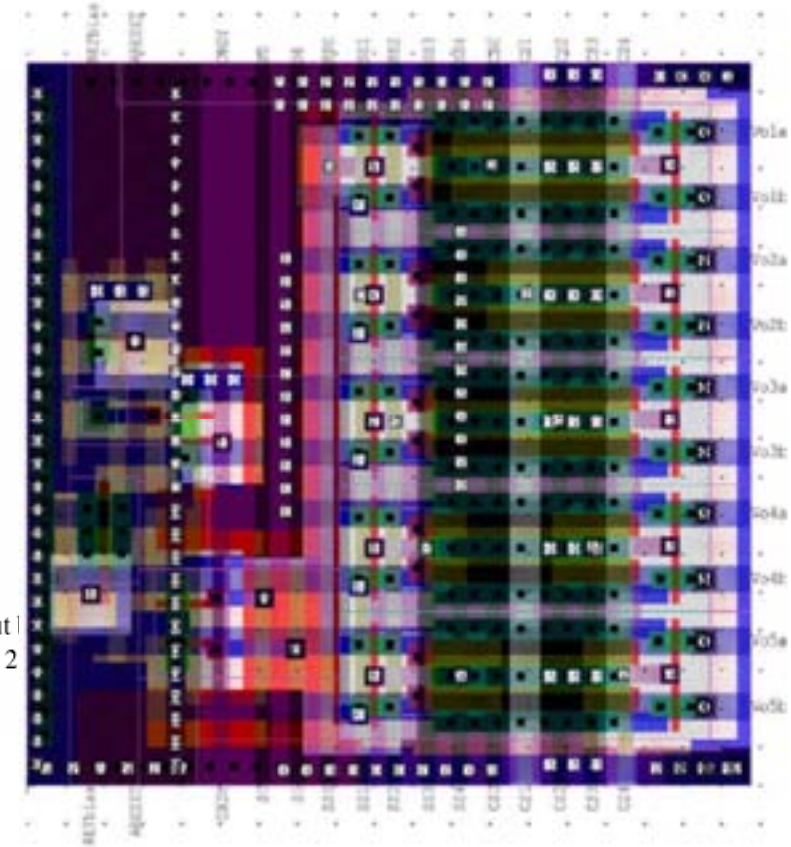
CAP3

120Kpixel sensor (128x928 pix)

TSMC 0.25µm Process

5-deep double pipeline





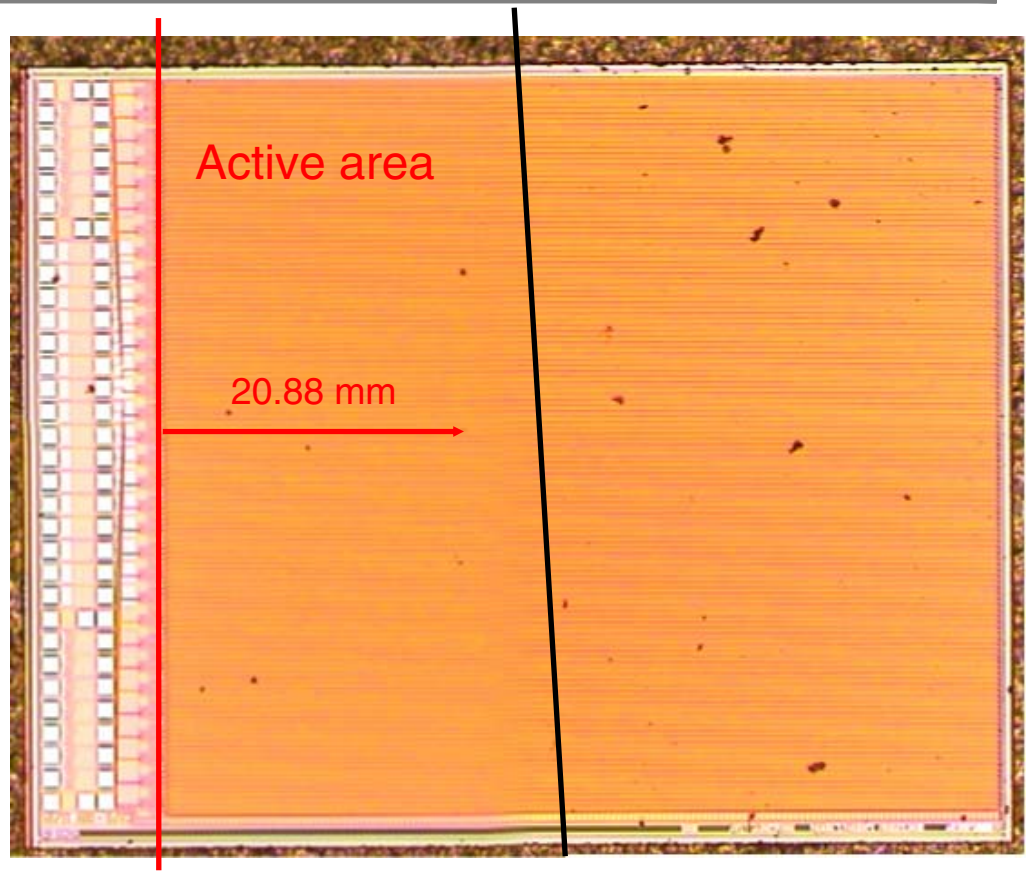
36 transistors/pixel

5 sets CDS pairs

5 metal layers

CAP3 – full-sized!

21 mm

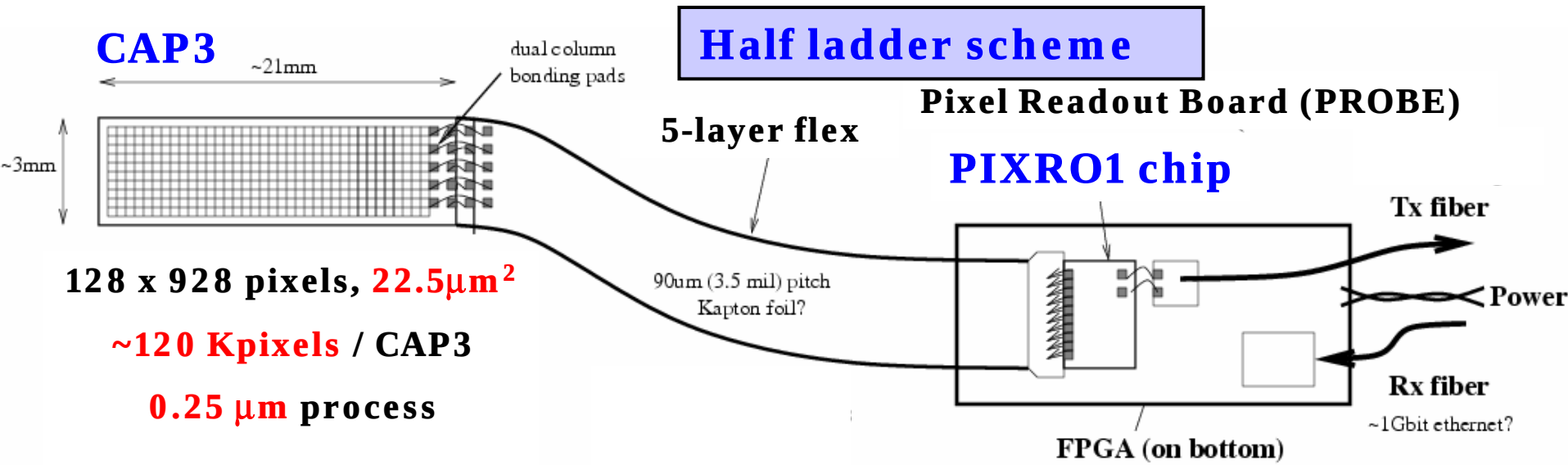


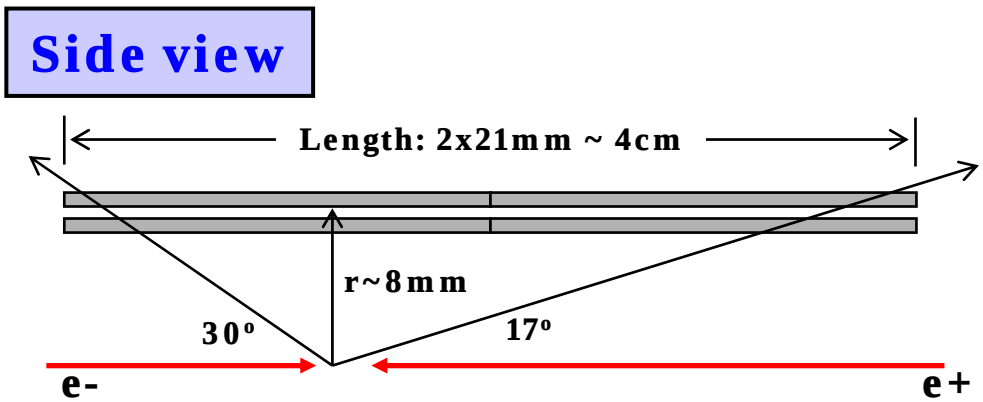
928 x 128 pixels = 118,784

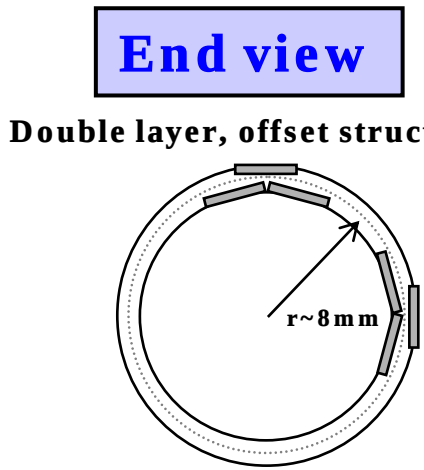
~4.3M transistors

>93% active without active edge processing

CAP3: Full-size Detector

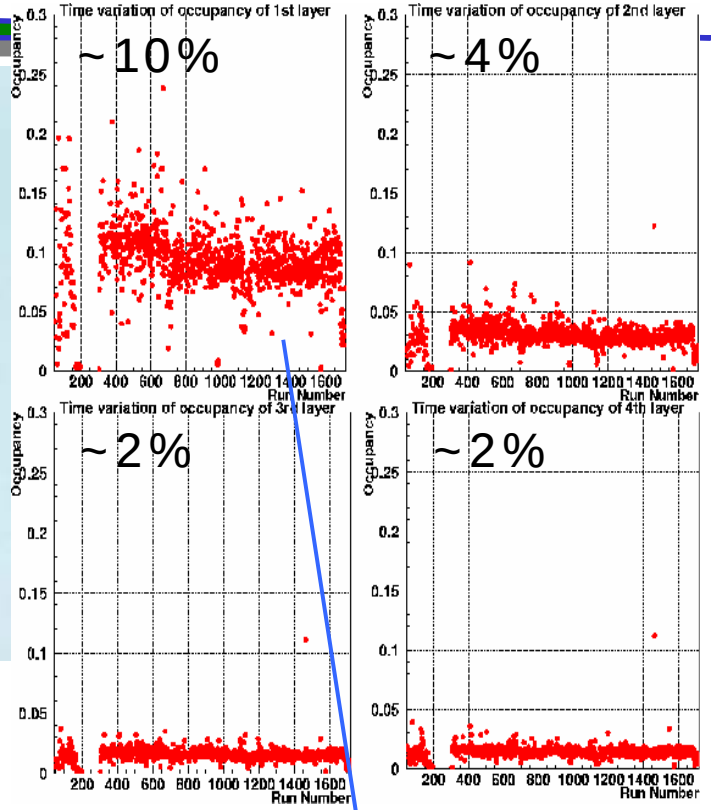




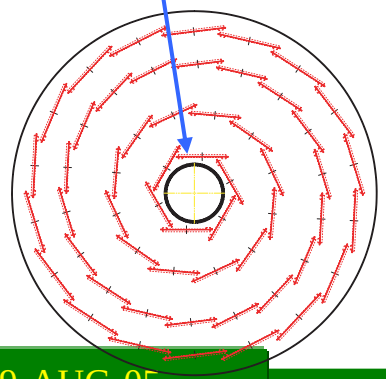


# of Detector / layer ~ 32

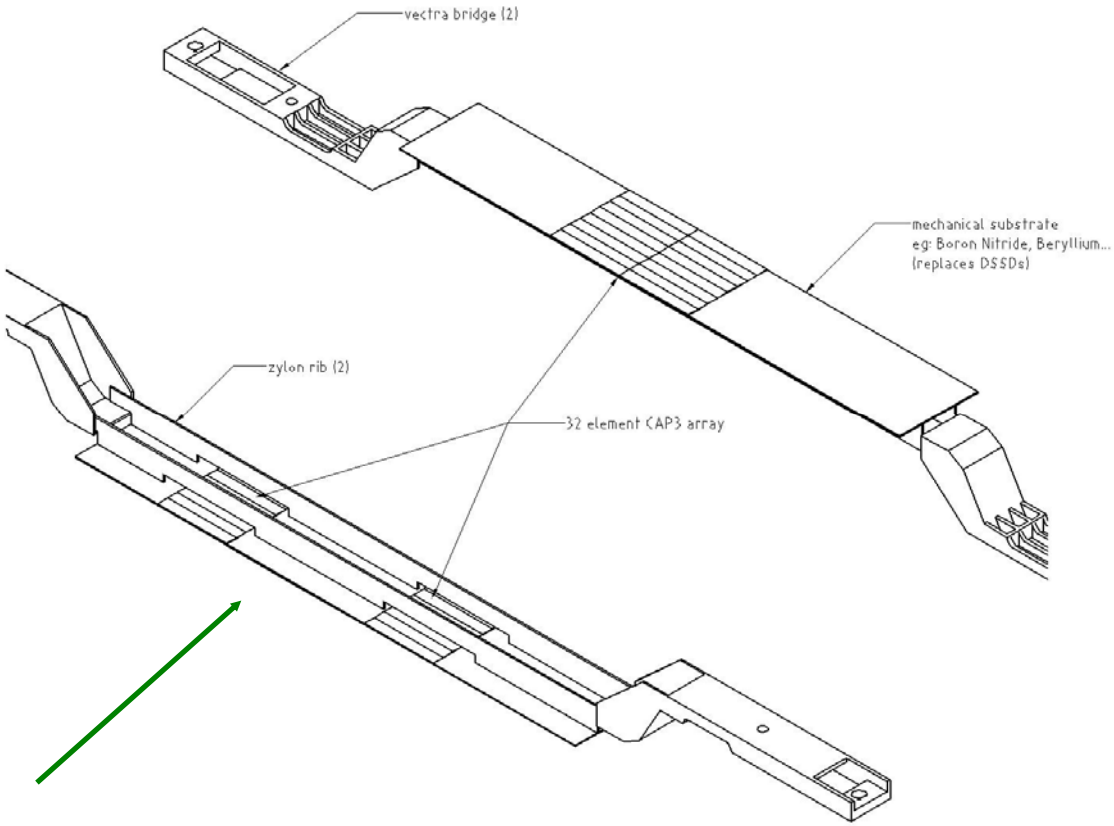
Short-term Upgrade

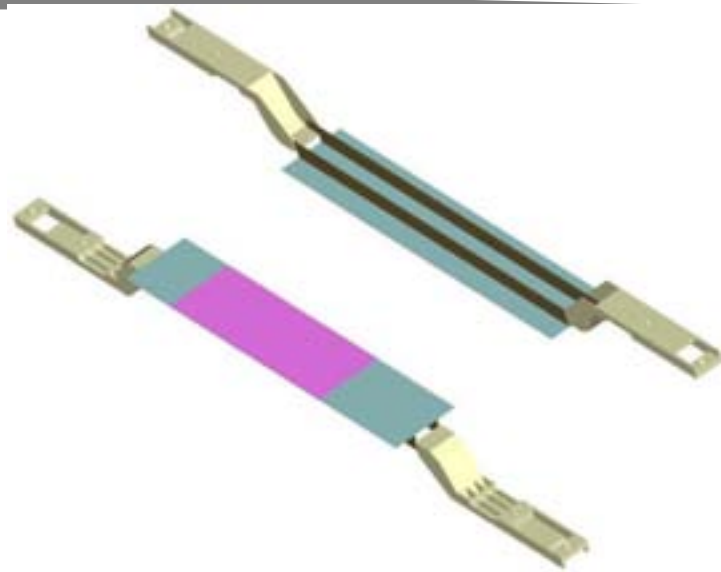


Replace Layer 1 with CAP3 pixels
Mechanically identical (drop in)



Short-term Upgrade (2)

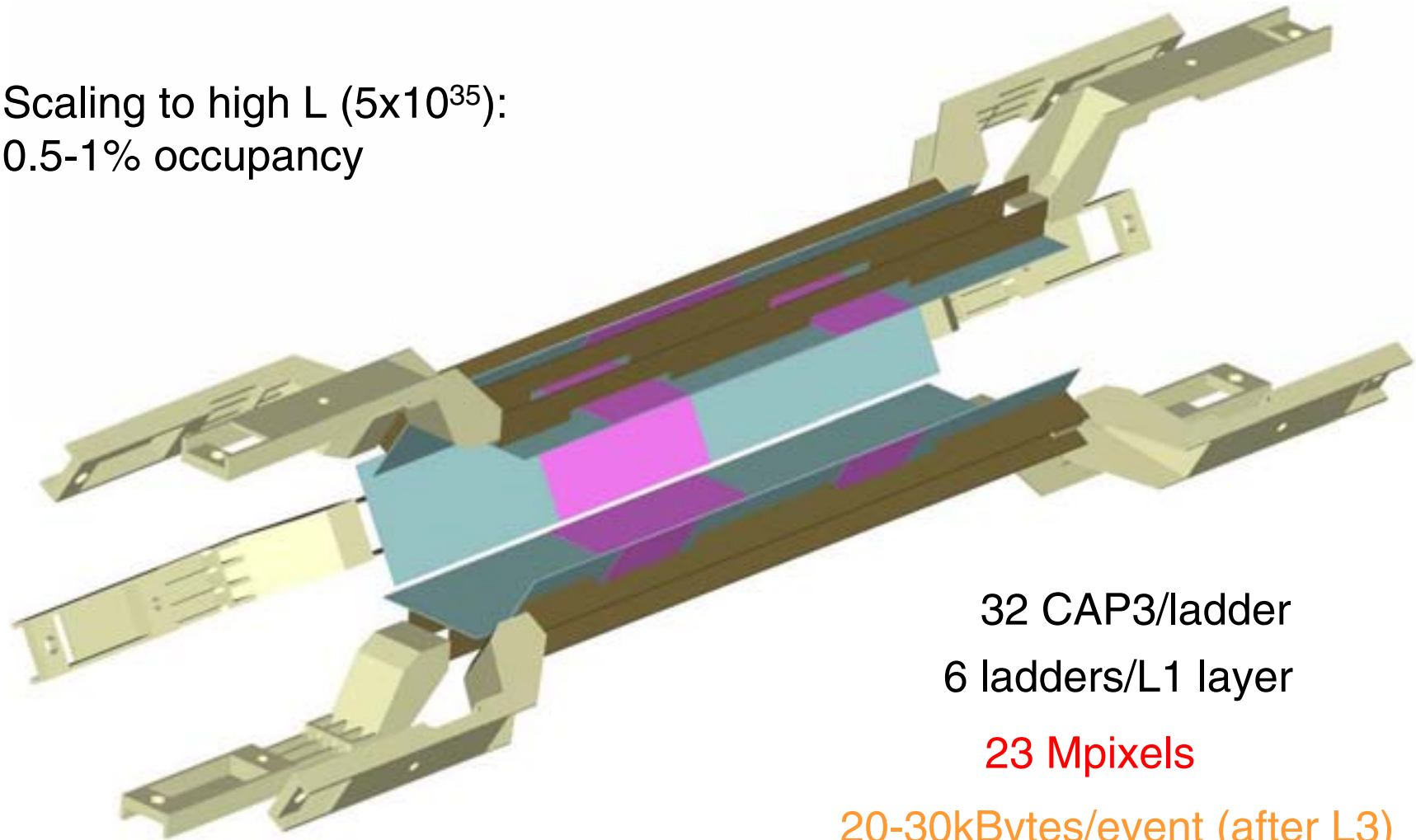




4 x 8 CAP3 basically spans
Belle acceptance

Short-term Upgrade (3)

Scaling to high L ($5x10^{35}$):
0.5-1% occupancy



32 CAP3/ladder

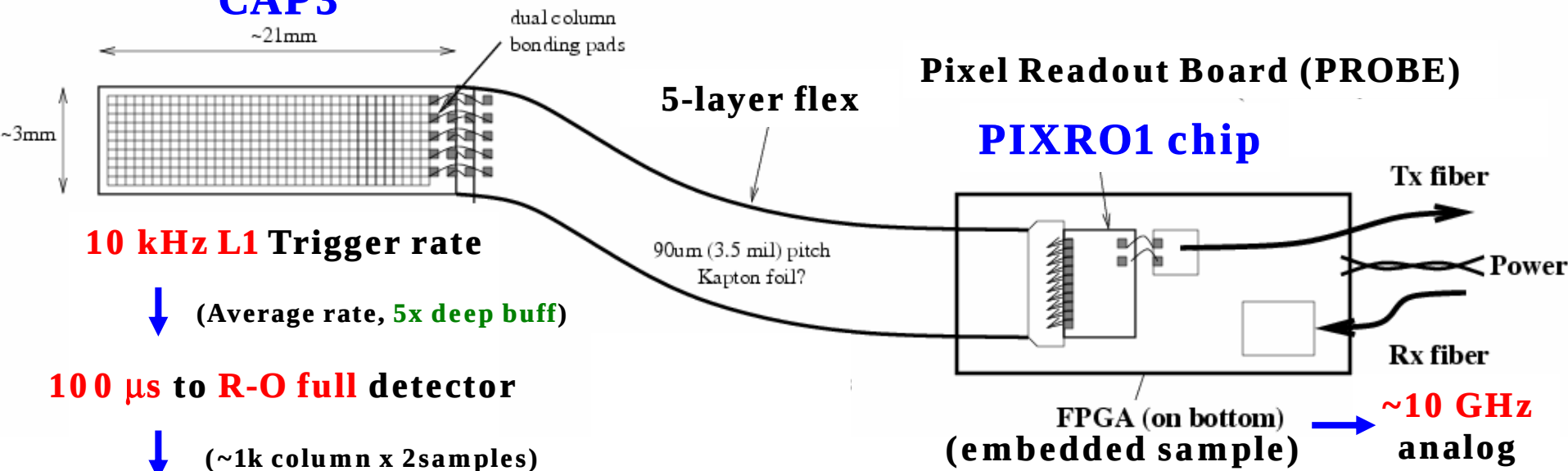
6 ladders/L1 layer

23 Mpixels

20-30kBytes/event (after L3)

Detector concept: data flow

CAP3: 10μs frame rate (experienced with CAP2)
Super-Belle: 10kHz L1 Trigger rate



10 kHz L1 Trigger rate

↓ (Average rate, 5x deep buff)

100 μs to R-O full detector

↓ (~1k column x 2samples)

100 ns / column

↓ (128 rows x2, 32 8:1 MUX)

2o ns bus settl., 10 ns/sample

→ **16 pairs of signals** (100 MHz signals) →

Differential receiver

↑ **16 CDS**

↑ **1.6 GSa/s analog (6 bits)** (high speed analog 16:1 MUX)

↑

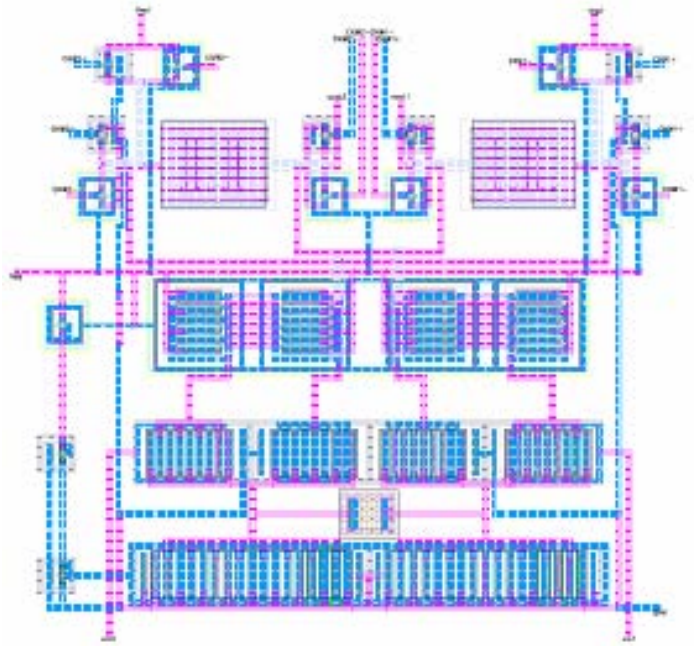
PIXRO1(1): Output Amplif.

In development at present time: **PRELIMINARY**

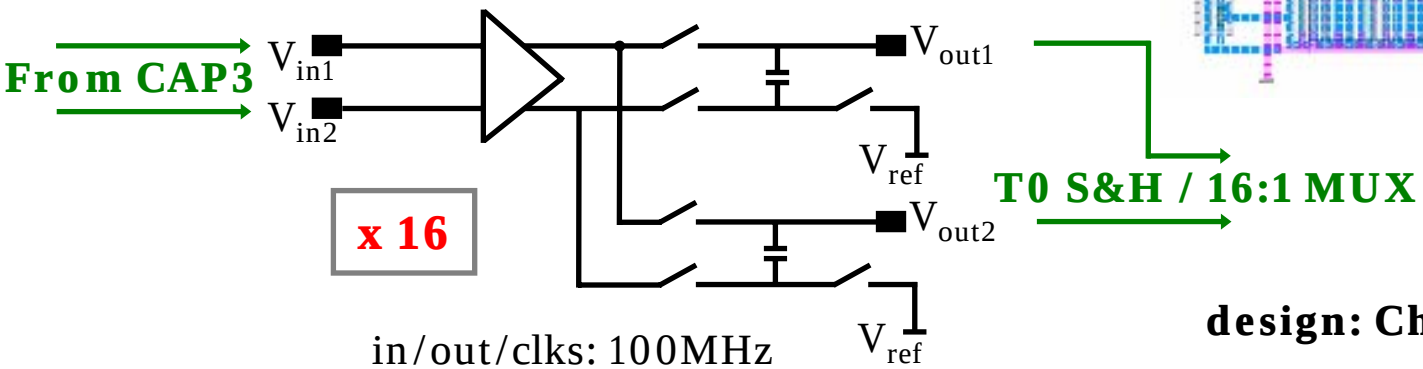
1 CAP ⟷ 1 PIXRO1

SiGe 0.5µm process from IBM

First version of PIXRO chip:
(relative) simplicity



Amplifier: Diff→Single Ended (fr2-fr1)



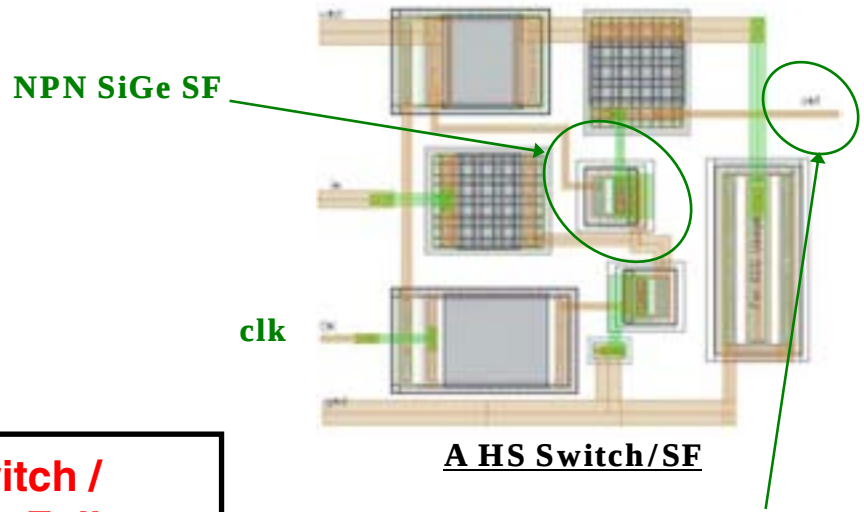
design: Chenyan Song (UH)

PIXRO1(2): S&H and 16:1 MUX

In development at present time: **PRELIMINARY**

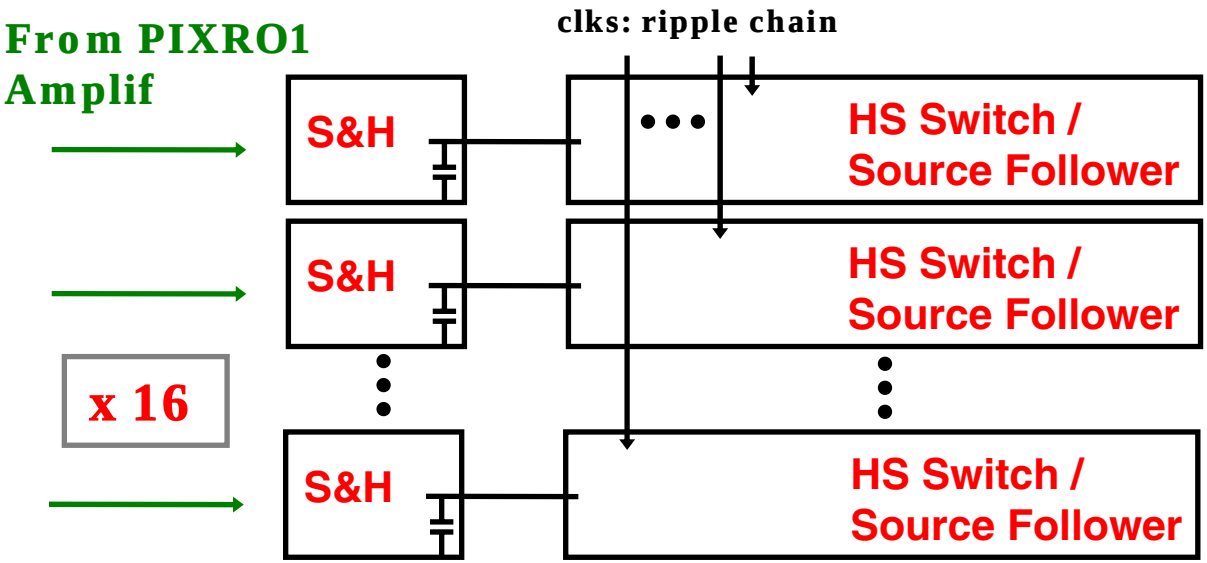
SiGe 0.5µm process from IBM

NPN switches & SF for high speed



A HS Switch/SF

Simul, single switch: 0.15ns settling (1V swing)



design: Qianyi Yang (UH)

Critical R&D Scorecard

1. Readout Speed

100kHz frame rate, 10kHz L2 accept

10μs frame OK (CAP2), CAP3 to test 100μs frame readout

2. Radiation Hardness

>= 20MRad

Leakage current OK (CAP2), q collection efficiency TBD

3. Thin Detector

<= 50μm, double layer <= 200μm

50μm mechanical dummies, CAP3 to be thinned (SNF)

4. Full-sized detector

Span acceptance (reticle limit)

CAP3 fabricated – performance being evaluated

SuperB to ILC

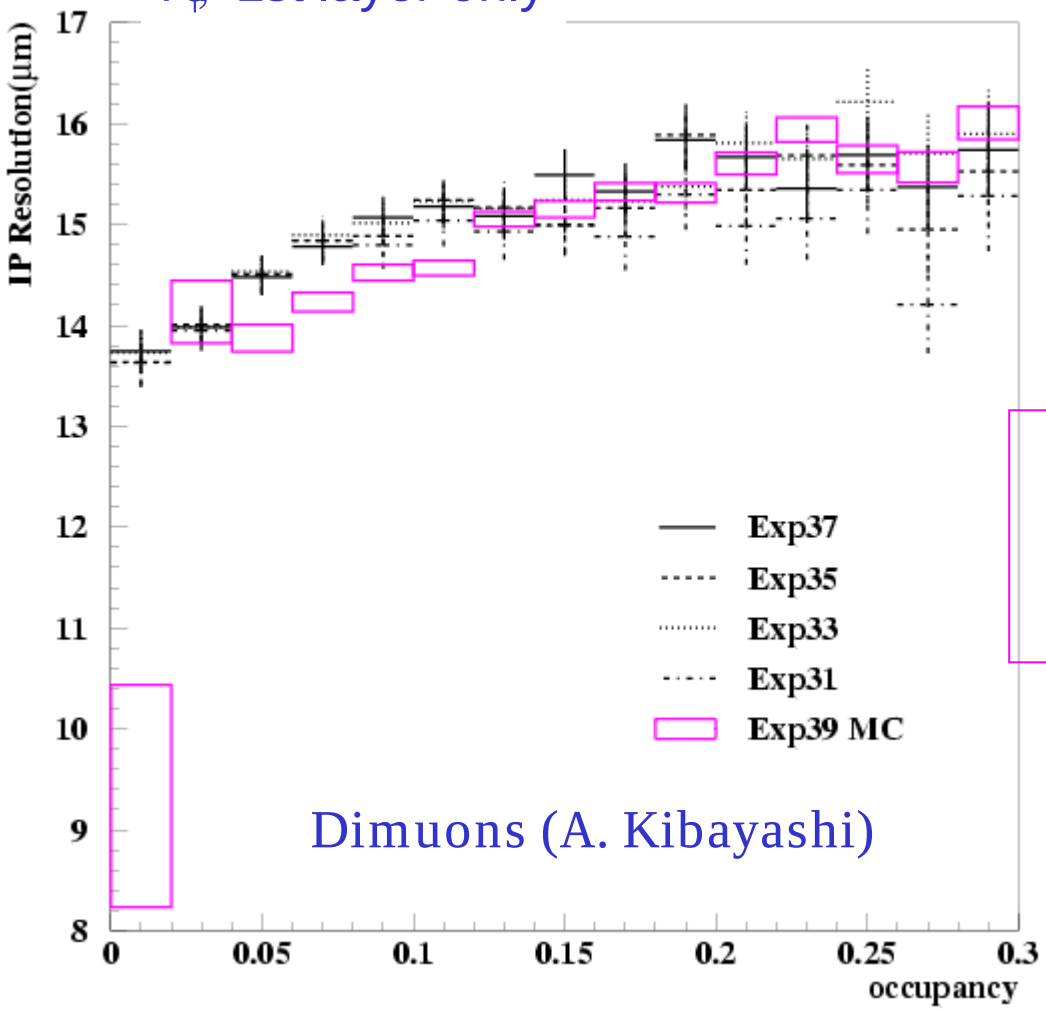
- Operating conditions: not so different

Parameter	ILC	SuperB	Comment
L1 Integration time	25μs/1ms	<= 10μs	Belle (trigger dep.)
BX collision timing	300 (150) ns	2ns	
#bunches/integ time	75(150)/2.8k	1-5k	
Expected Occupany	~1%	0.5-1%	Belle extrap.
# of pixel channels	100's-1k M	10-50M	
Duty cycle (high power)	few %	5-10%	within acceptance
Readout cycle	between trains	continuous	
Pixel readout rate (raw)	500/10 G/s	200-1000 G/s	10kHz trigger rate
Radiation requirements	50kRad/yr	few MRad/yr	NIEL not considered

- Prototype for ILC detector (?)

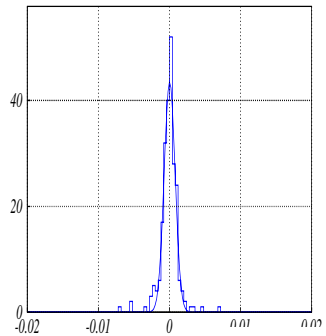
A Comment on Occupancy

rϕ 1st layer only

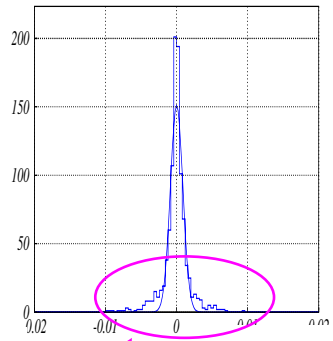


Dimuons (A. Kibayashi)

occupancy < 0.04 occupancy≈ 0.3



residual



residual

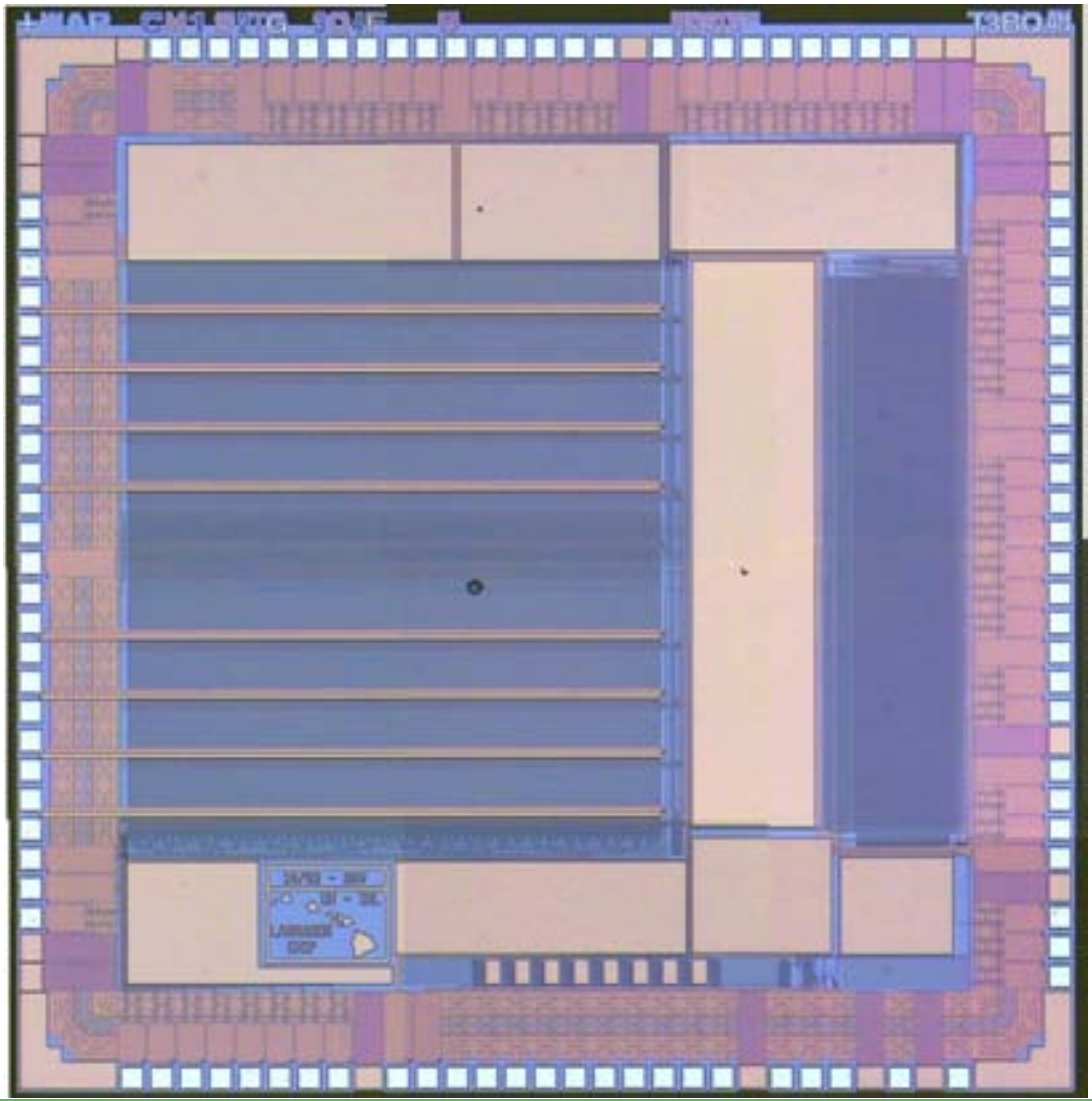
This widened residual distribution causes intrinsic resolution degradation at higher occupancy.

⇨ Degradation of IP resolution ~10% for 2~6 GeV tracks.

Summary

- Great Progress toward Pixel Vertex Detector
- Looking ahead:
  - KEK beam test :
    - “ultimate” resolution, triggered/pipelined readout, SNR/hit efficiency of irradiated detectors with CAP3
  - SVD2 L1 “drop in” design started
    - Exploring optical high-speed links
    - “prototype” for VTX (merge CAP+PIXRO)
  - SOI process evaluation (w/KEK)

Back-up slides

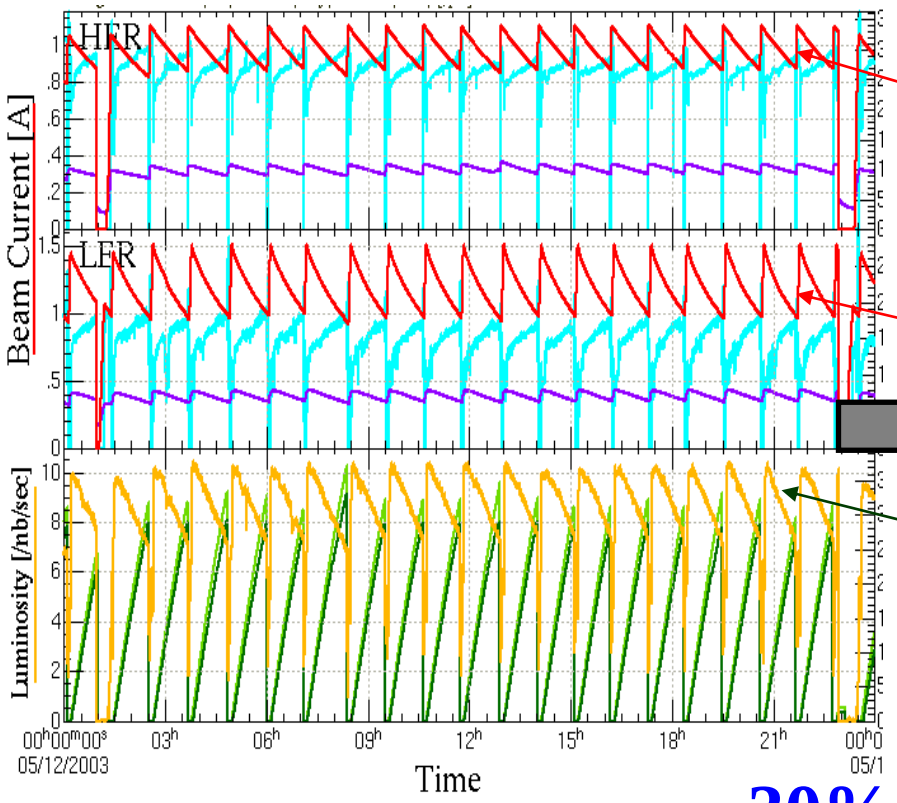


Continuous Injection

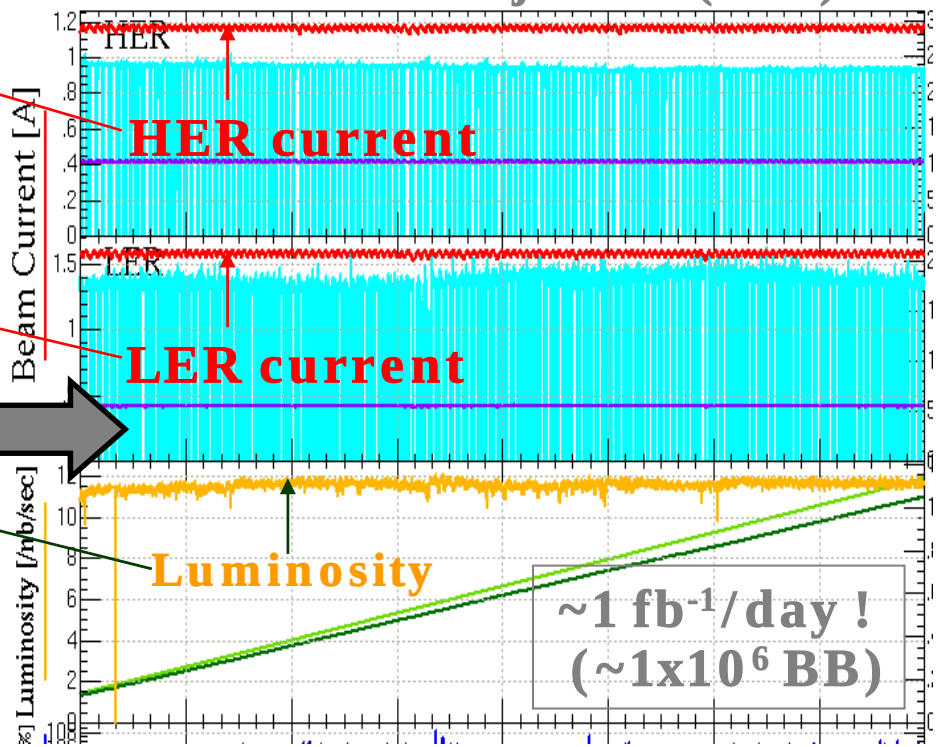
No need to stop run
Always at ~max. currents, luminosity

[CERN courier Jan/Feb 2004]
both KEKB & PEP-II

normal injection (old)

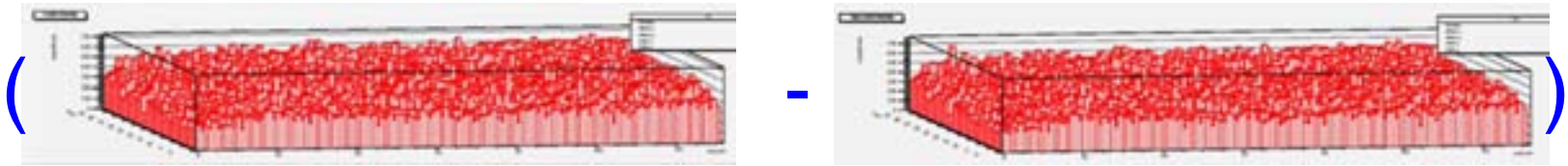


continuous injection (new)



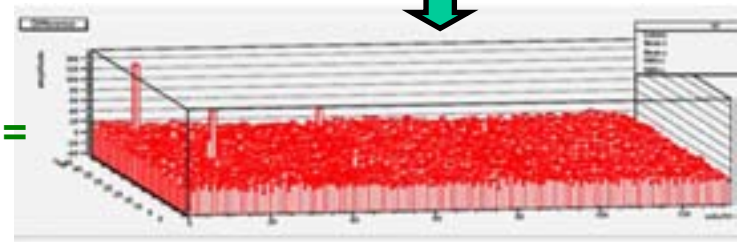
~30% more $\int L\,dt$

Correlated Double Sampling (CDS)

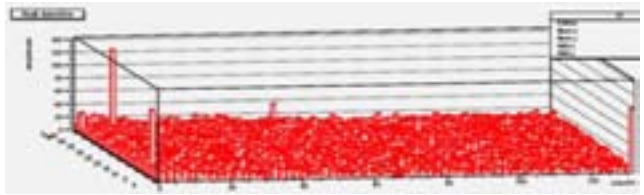


8ms integration

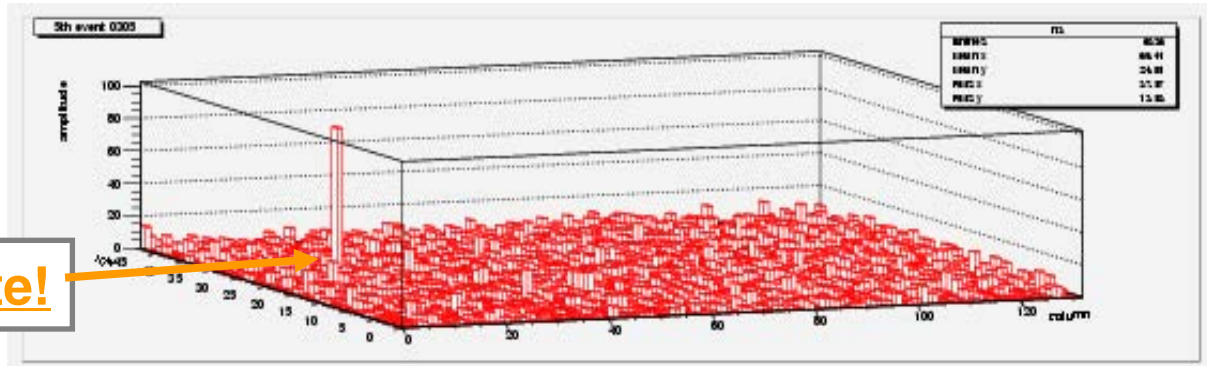
Frame 1 - Frame 2 =



- Leakage current Correction



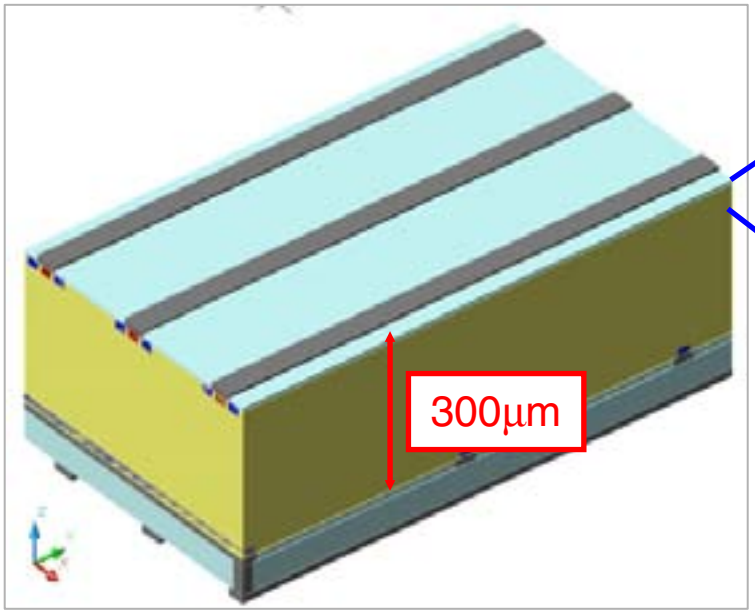
~fA leakage current (typ)
~18fA for hottest pixel shown



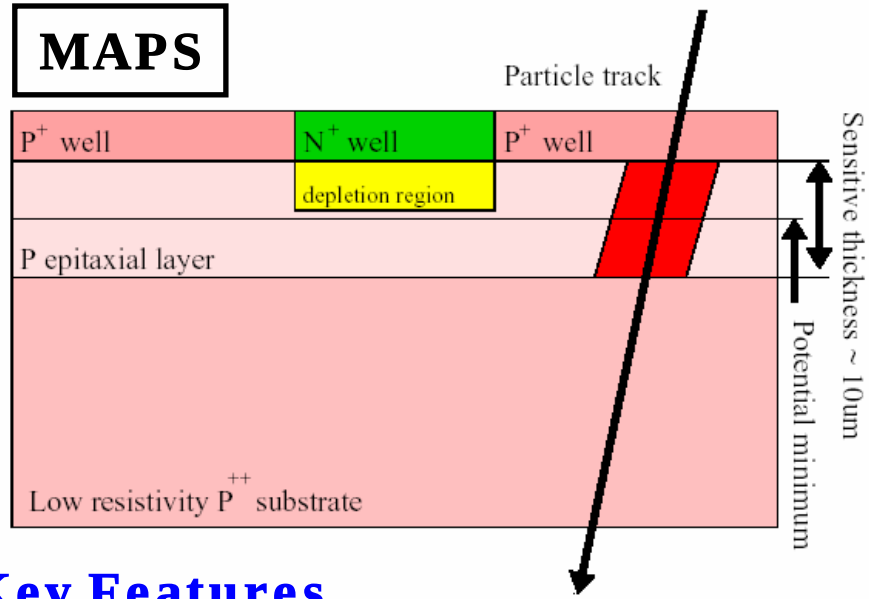
Hit candidate!

Candidate: Monolithic Active Pixel Sensor

Current DSSD



MAPS



Because of large Capacitance, need Thick DSSDs -- APS can be VERY Thin

Key Features

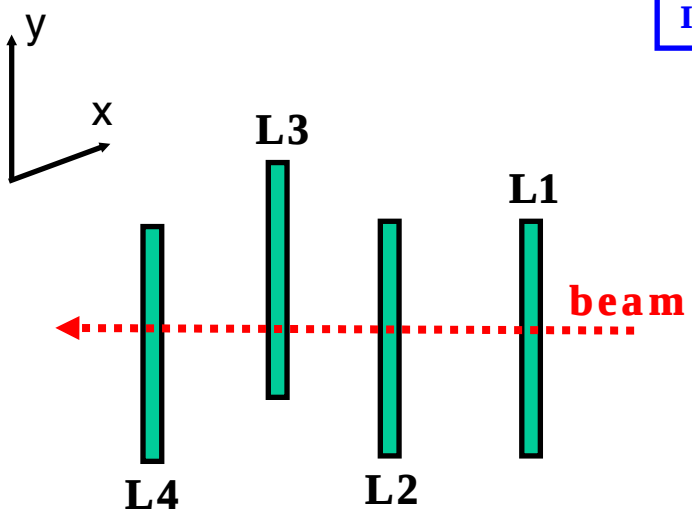
- Thermal charge collection (no HV)
- Thin - reduced multiple-scattering, γ conversion, background γ target
- NO bump bonding – fine pitch possible (8000x geometrical reduction)
- Standard CMOS process - "System on Chip" possible

CAP Comparison

	Technology	# channels (# cells)	spatial resolution	Noise	Rad hardness I_{leak}	Rad hardness Q_{col}	Problem
CAP1	TSMC 0.35μm	6336 (6336)	<11μm (~3μm)	16e-	> 2MRad	unmeas.	too slow
CAP2	TSMC 0.35μm	6336 (50688)	unmeas. (3-4μm)	30-50e-	>=20MRad	unmeas.	poor power
CAP3	TSMC 0.25μm	118,784 (1.18M)	**TBD** (3-4μm)	**TBD**	**TBD**	**TBD**	**TBD**

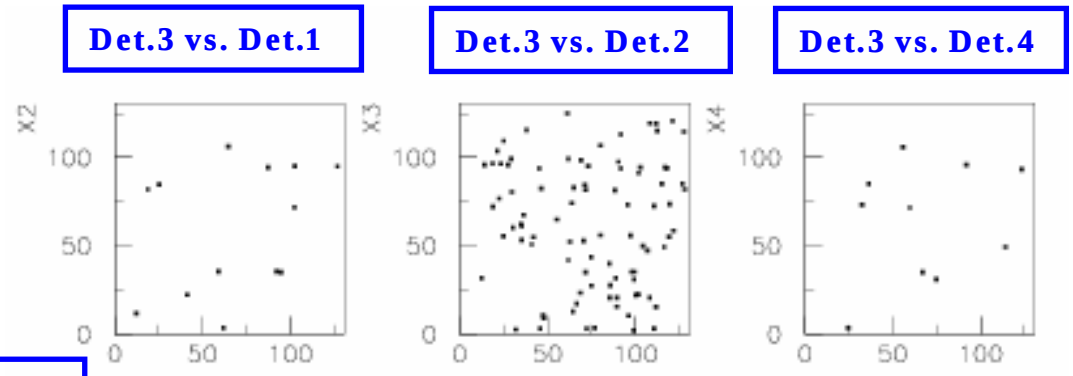
Mechanical alignment

~1mm x 3mm "rice grain"

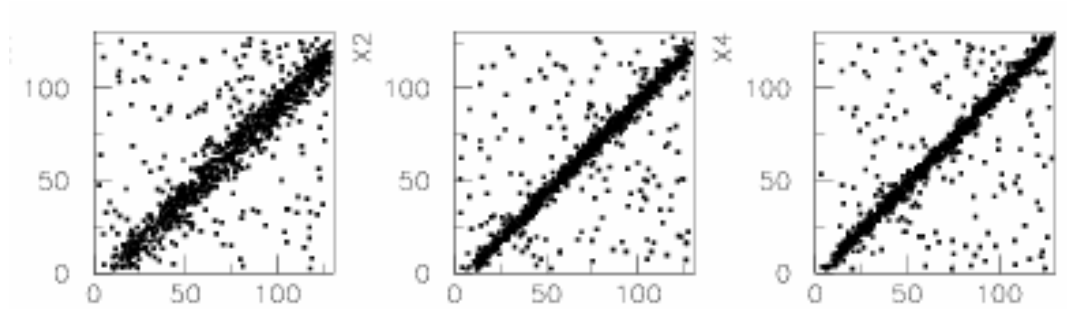


Initial Det. /Det. correlations

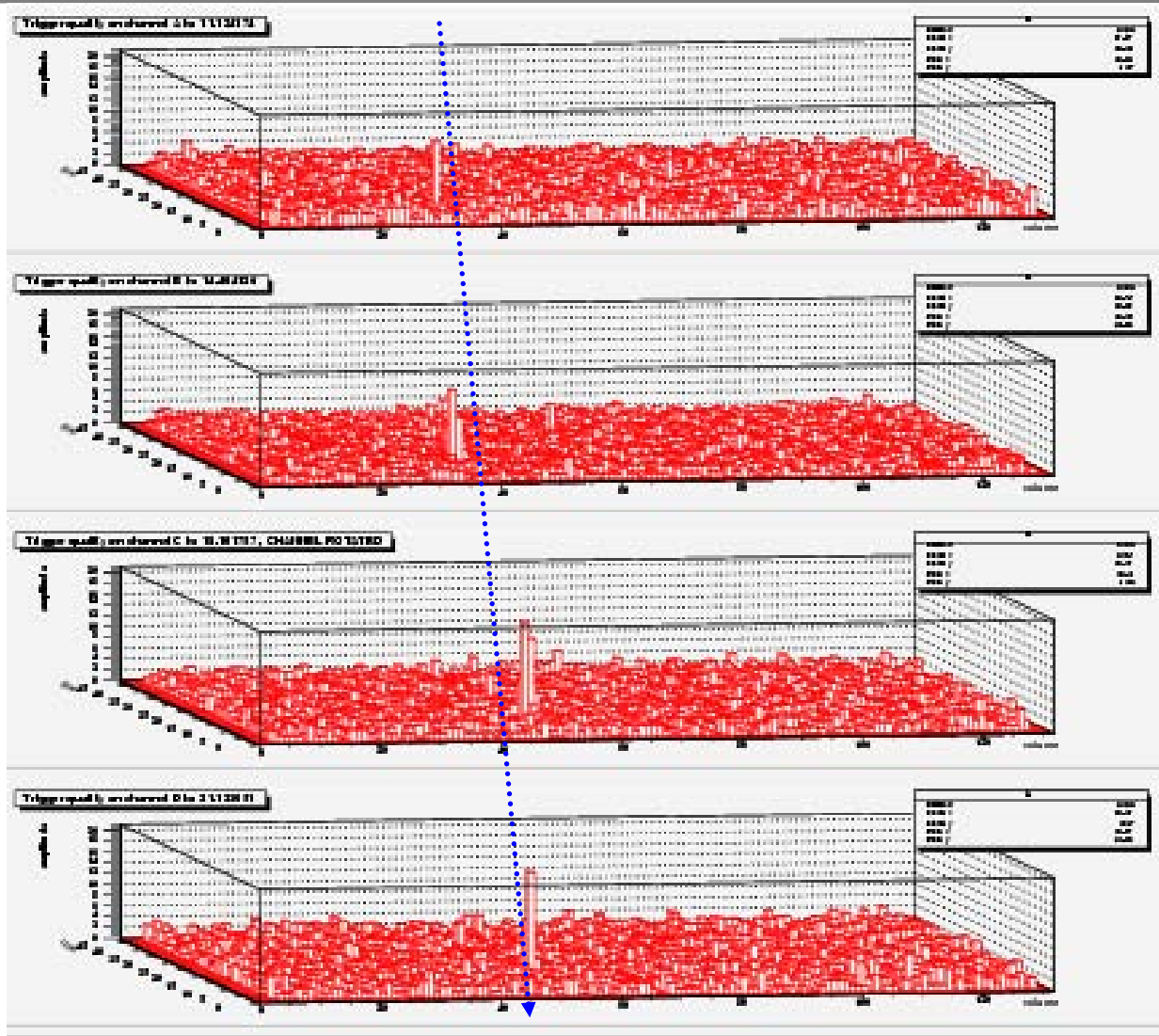
In X



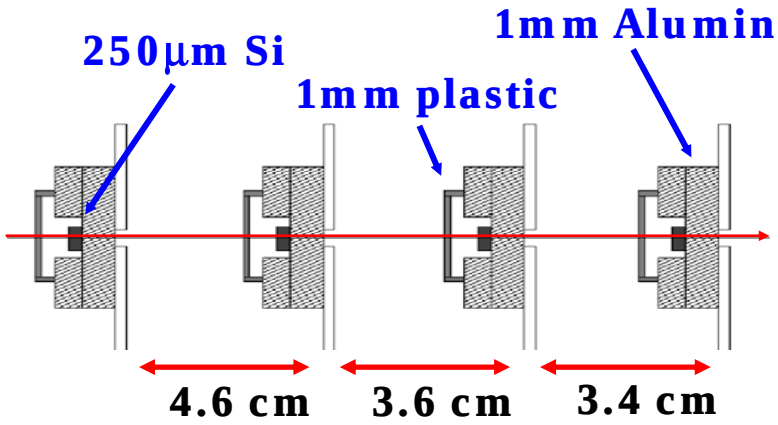
Improved correlations

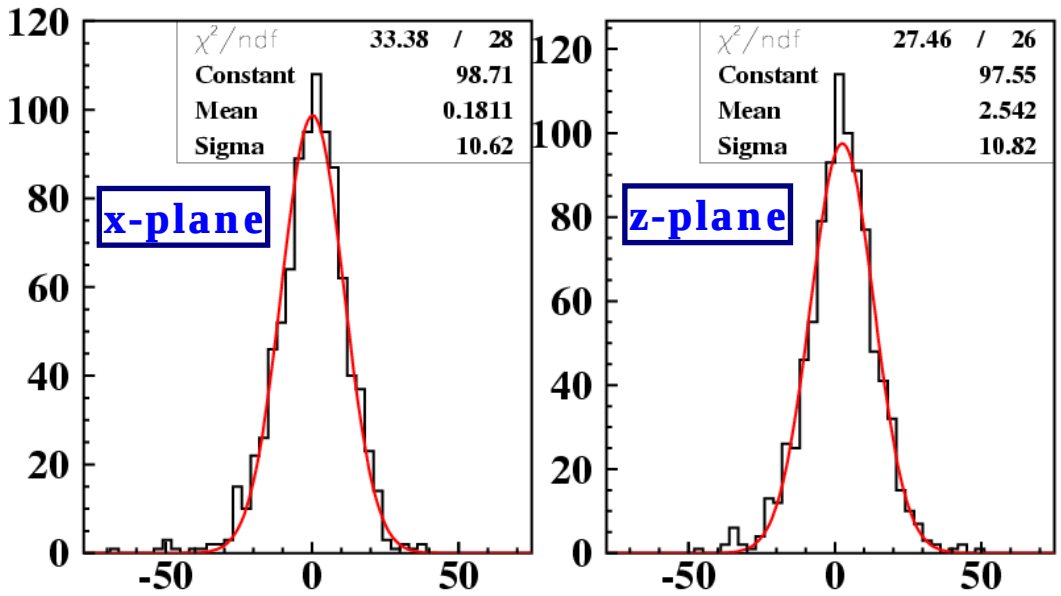


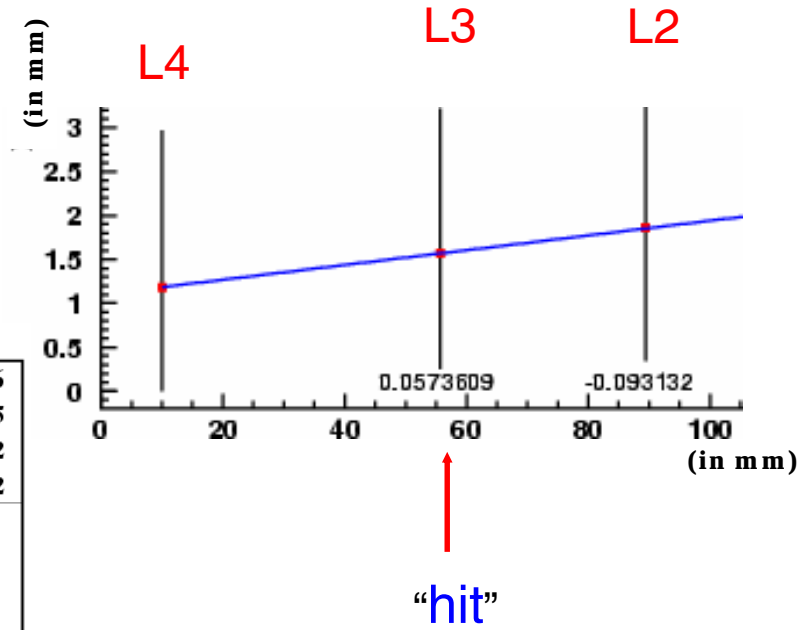
Hits! alignment proof



Hit resolution measurement







Residuals for 4GeV/c pions:
- <11μm (in both planes)

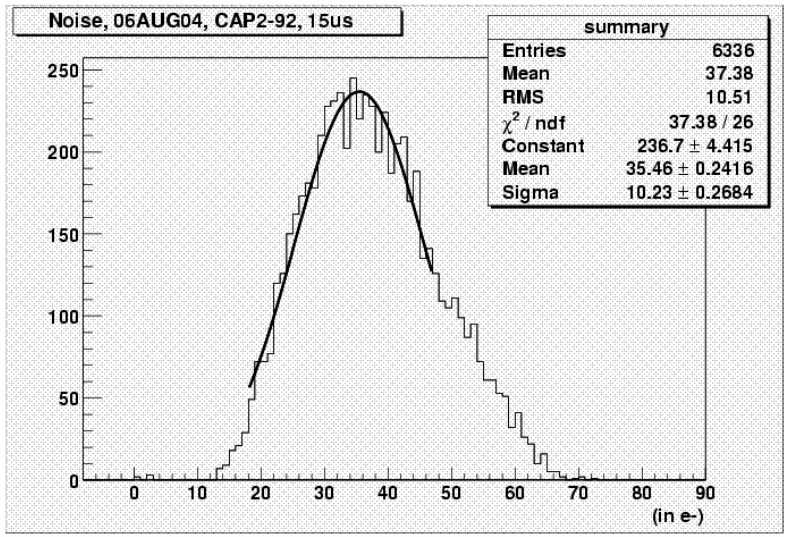
Increased readout speed: CAP2

15μs operation of CAP2:

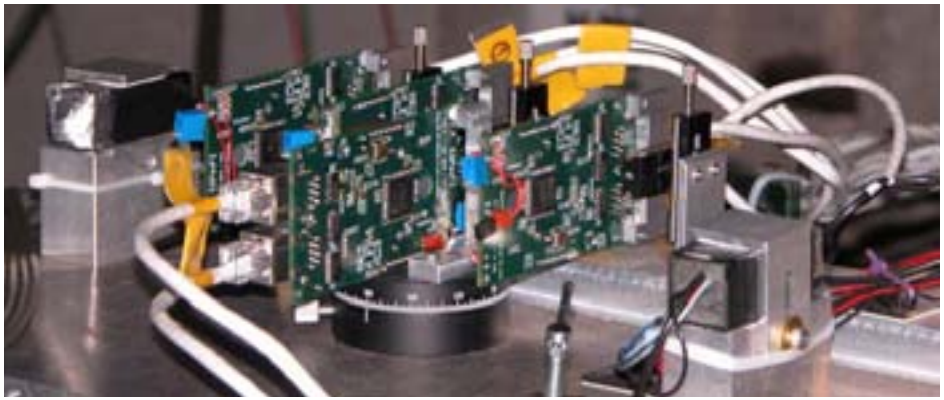
Current status:

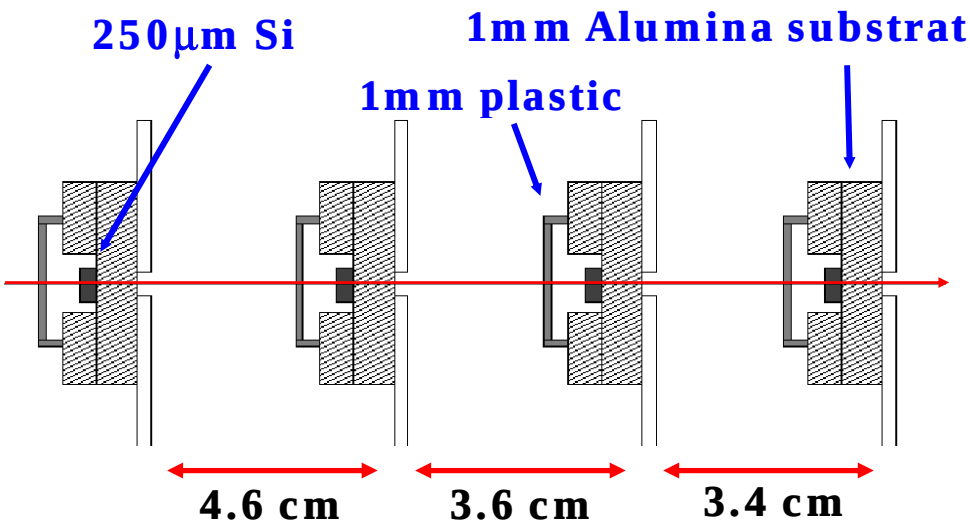
- **Noise higher than what is observed with CAP1/F2/B2 (~30 to 50e- vs. 16e-). Related to digital activity → better shielding**
- **Mini-pipeline output level dispersion rather large → Larger storage cells**
- **CAP2 testing demonstrated weakness Bus voltage drops during readout → Improved power routing**

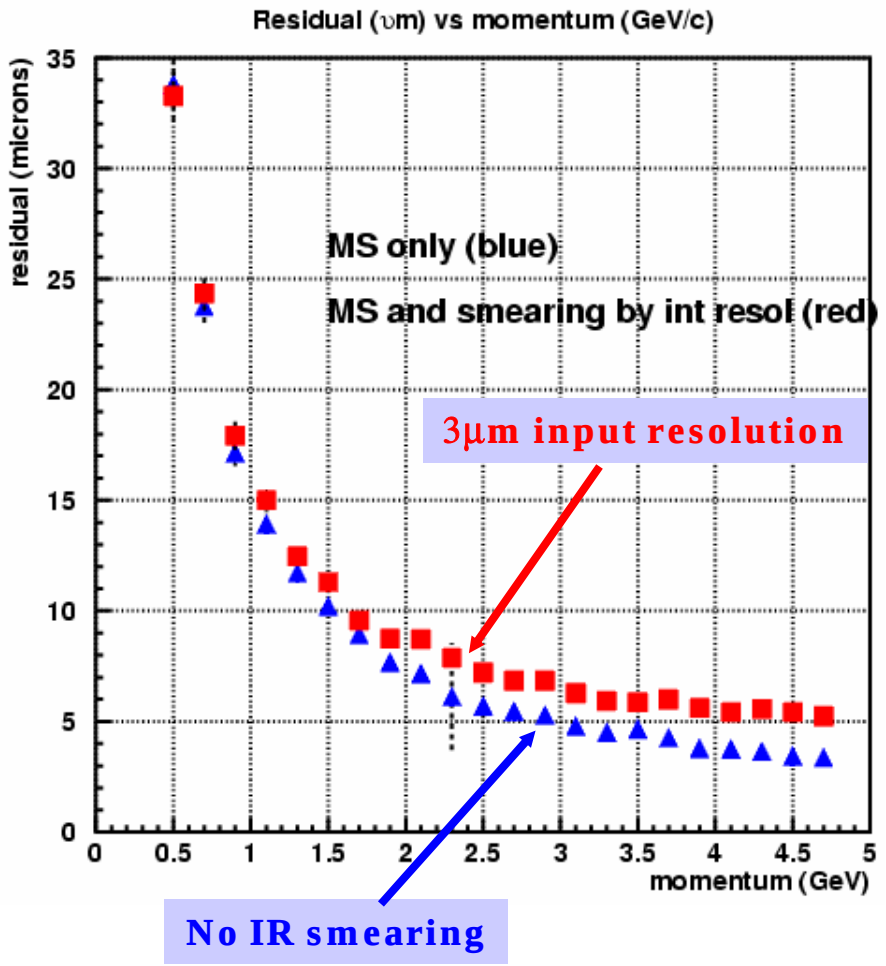
Items improved in CAP3



Resolution: GEANT Expectation



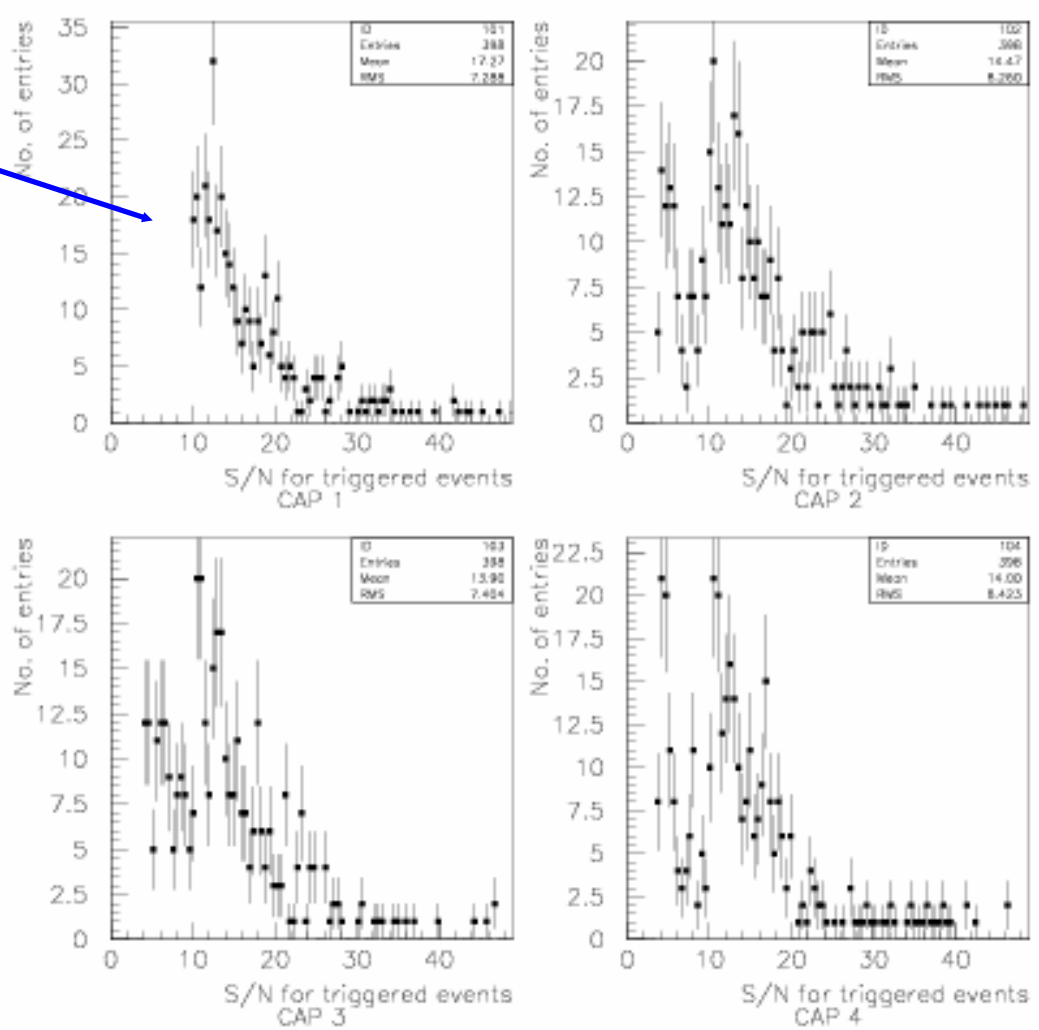




S/N for correlated hits

Triggering on Layer 1

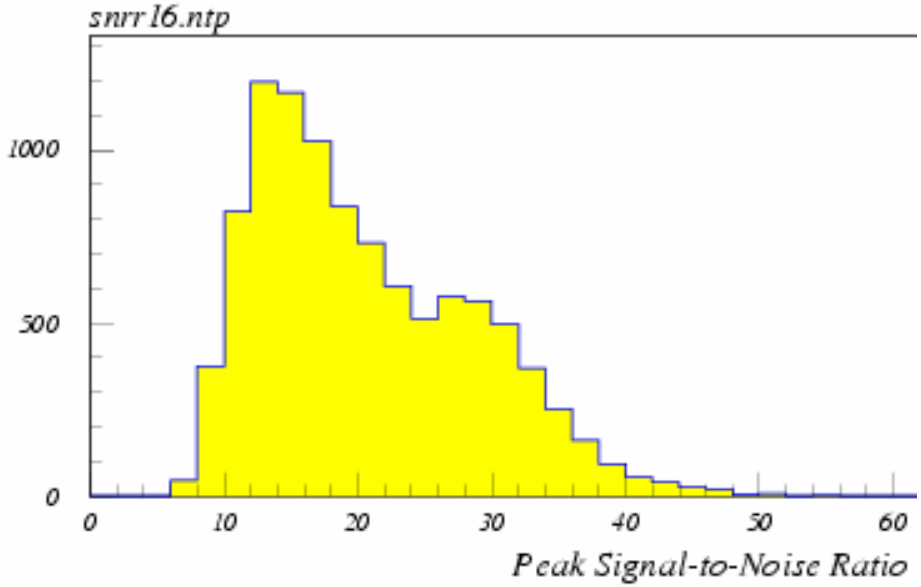
What should we expect?

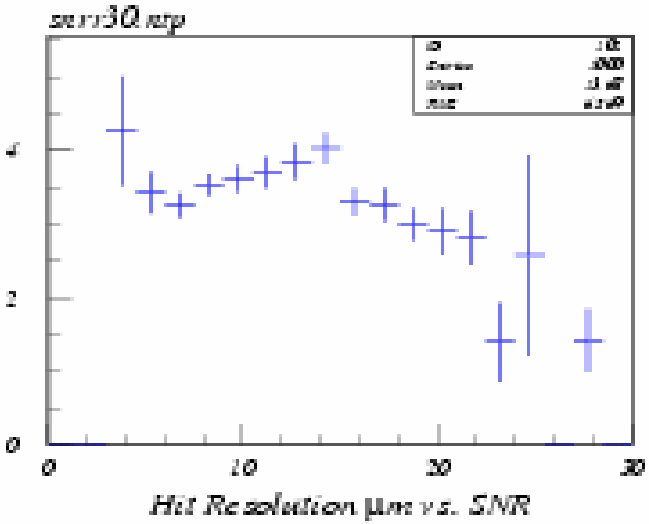


Hit resolution vs. SNR MC

Toy MC:

1) Generate random impact parameter
2) Landau fluctuation of signal
3) Charge diffusion (thermal)
4) Add noise (16e-/30e- system)
5) CoG of hit calculation

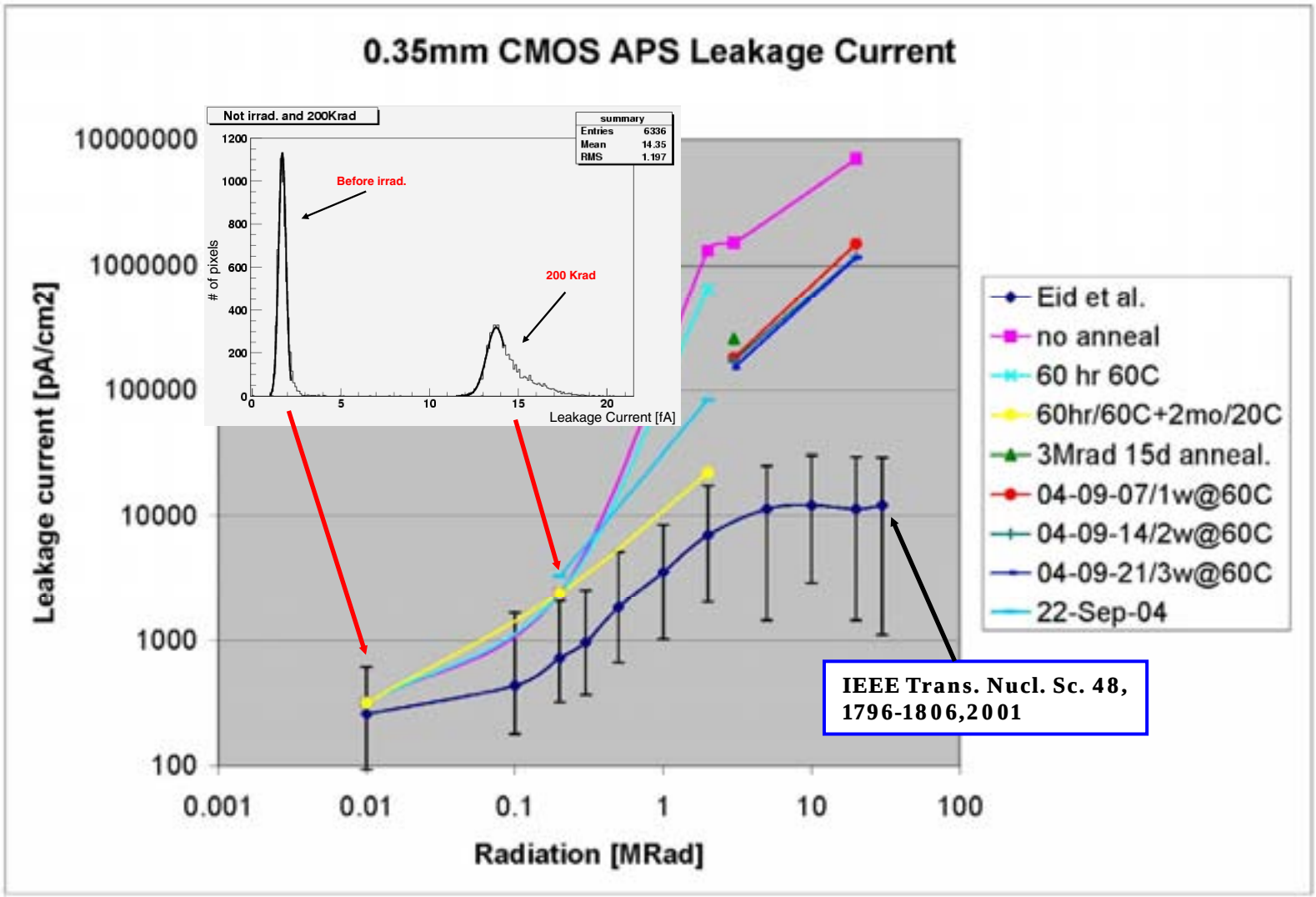




Good hit resolution even at low SNR

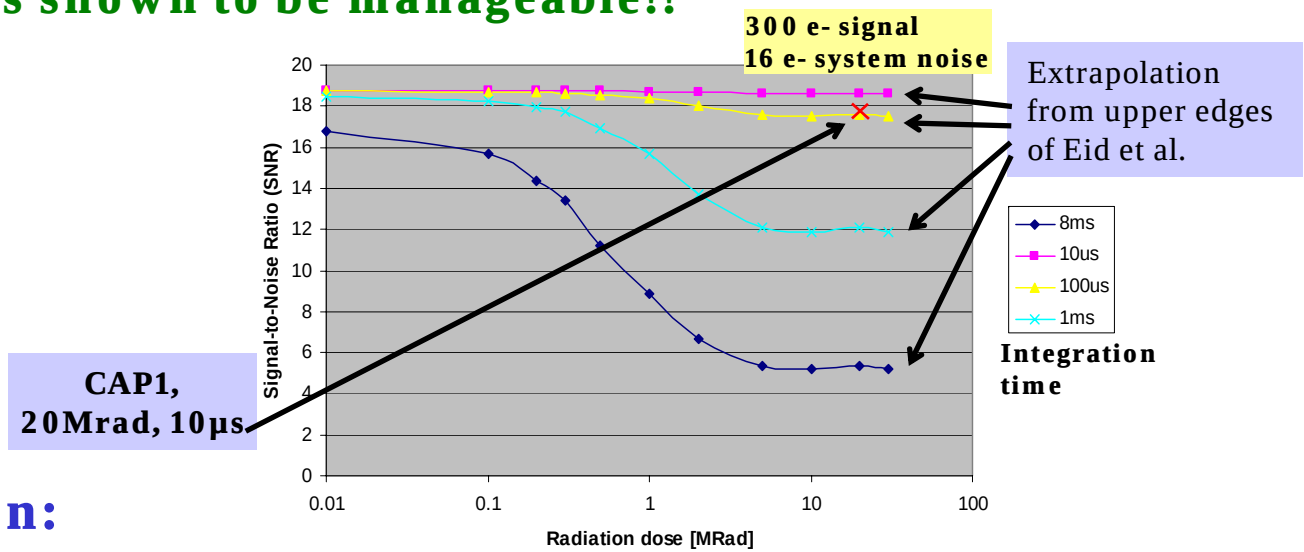
Note binary limit:
22.5µm/sqrt(12) ~6.5µm

Irradiation: leakage current



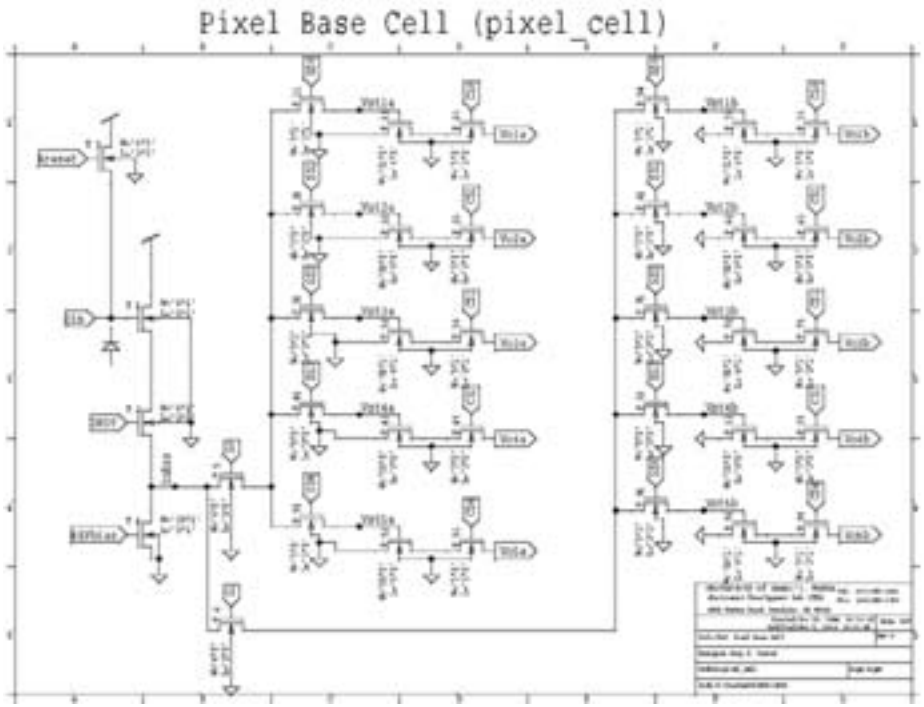
Status of irradiation studies

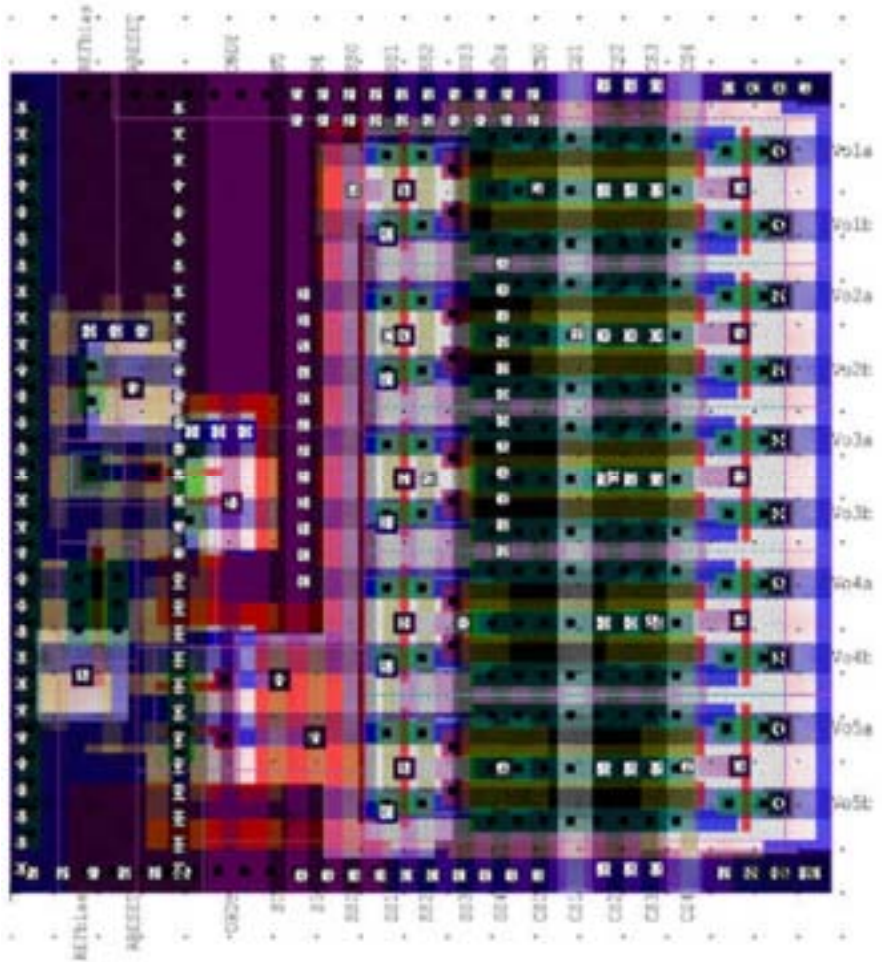
- **Leakage current:**
  - **At 200 krad, leakage current increase a factor ~10. At 20Mrad, leakage current increase a factor ~10000 (fast dose)**
  - **Annealing of detector reduces Ileak 1-2 orders of magnitude**
  - **In simul, the contribution of the leakage current to the SNR degradation is shown to be manageable!!**



- **Signal collection:**
  - **Bulk damage → trapping centers → signal loss.**
  - **To be studied in a beam test.**

CAP3 – 0.25µm TSMC process





36 transistors/pixel

5 sets CDS pairs

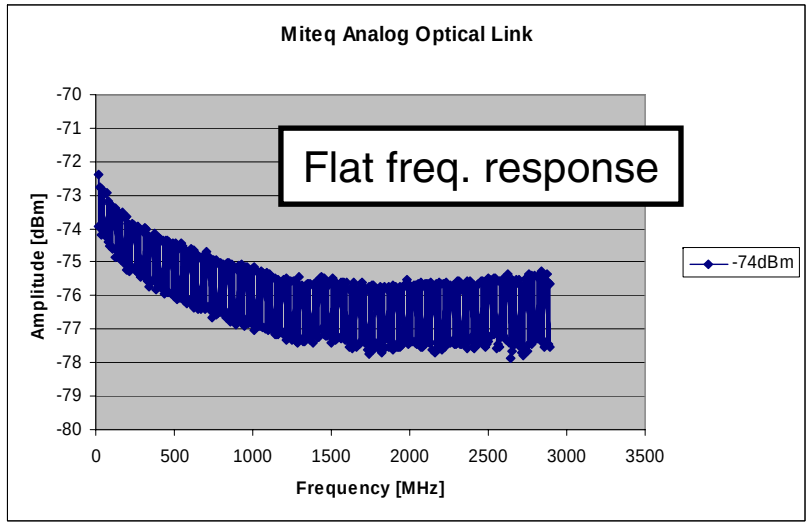
5 metal layers – improved routing

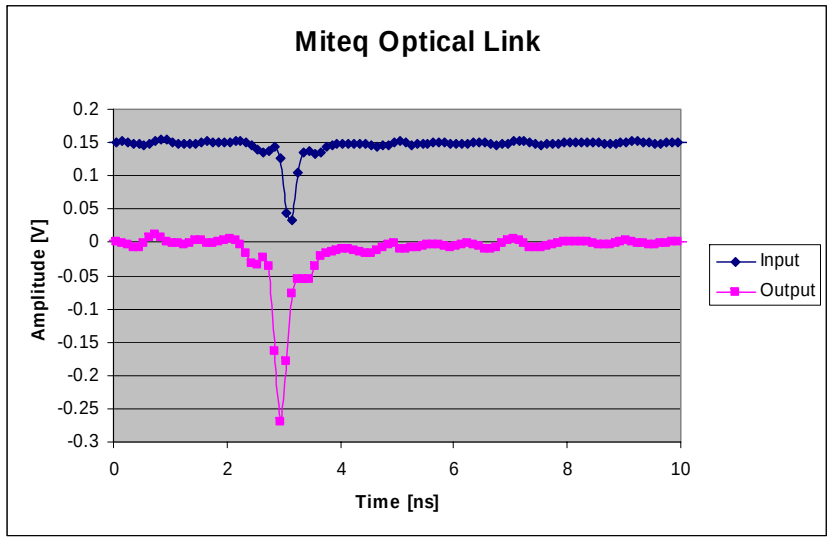
Occupancy Scaling

- Work from following assumptions:
  - Super-B canonical x20 background increase
    - Assume 10% Layer 1 occupancy as "current"
    - Strip area (L1) = 85mm x 50μm = 4.25M μm^2
  - Pixel spatial reduction:
    - Pixel area = 22.5μm x 22.5μm = 506 μm^2
    - Reduction factor ~8400
    - Low E γ, reduced cross-section (~3% active thickness)
  - Pixel temporal loss:
    - 0.8μs SVD vs. 10μs PVD (could be improved)
    - Increase factor ~ 12.5
  - Grand total:
    - 10% * 20 * 8400^{-1} * 12.5
    - Can expect ~ 0.3% occupancy (no ghosting)

Optical Link Evaluation

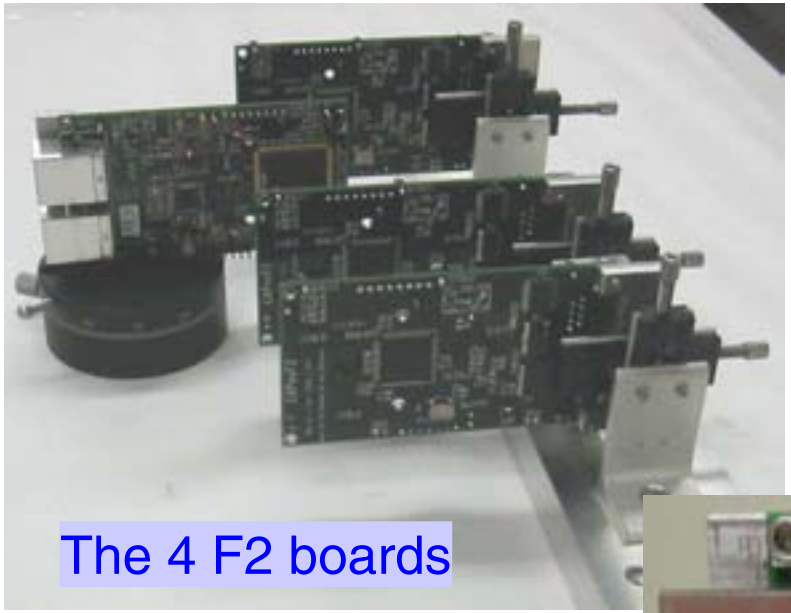
Potentially small, evaluating bare die



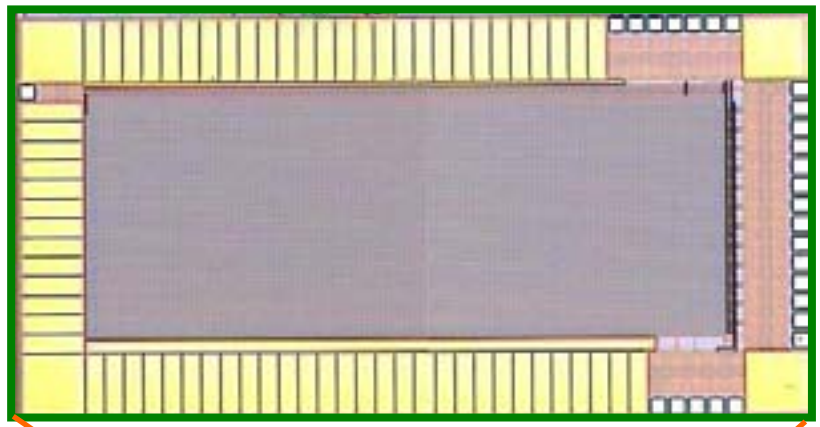


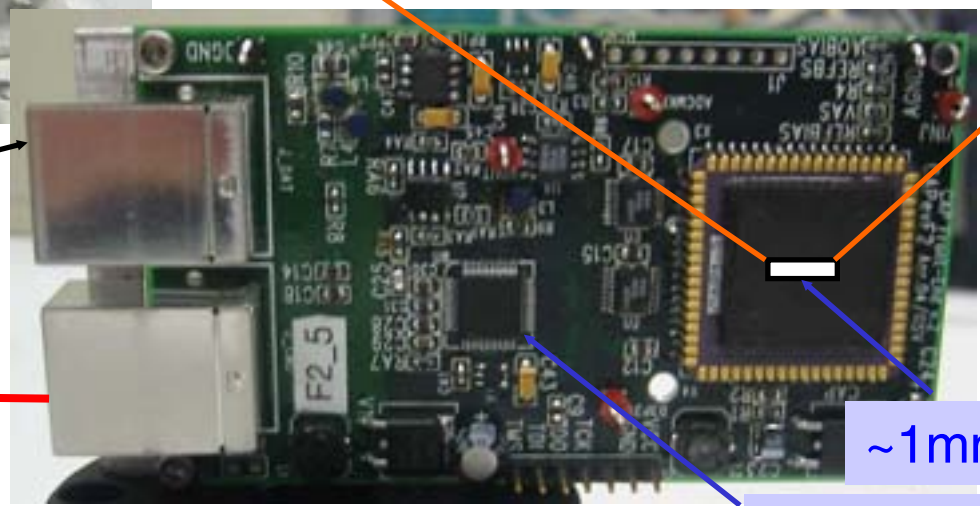
CAP on Front-End Board

Pixel chip: 132x48=6336 channels



The 4 F2 boards





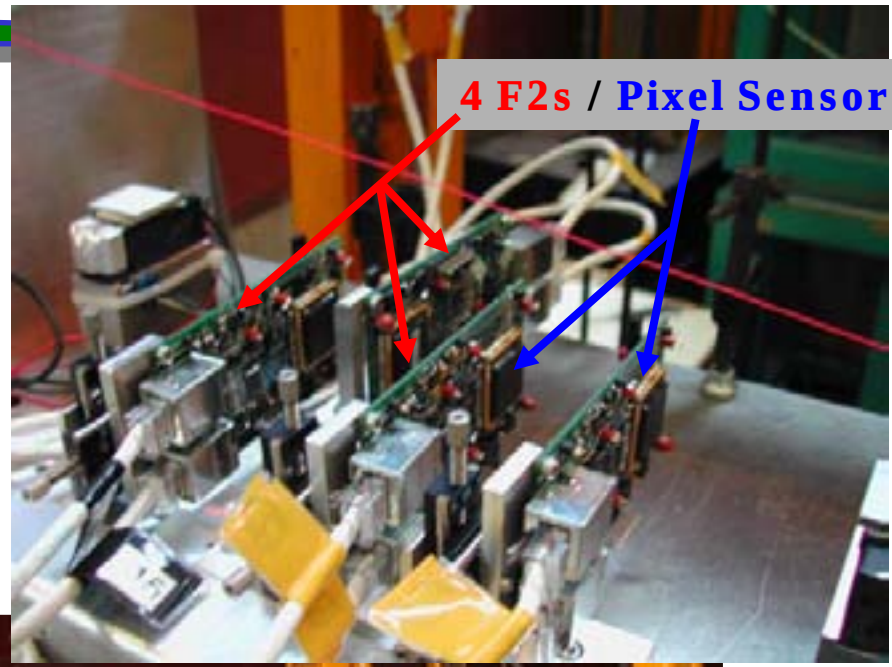
All LVDS digital I/O

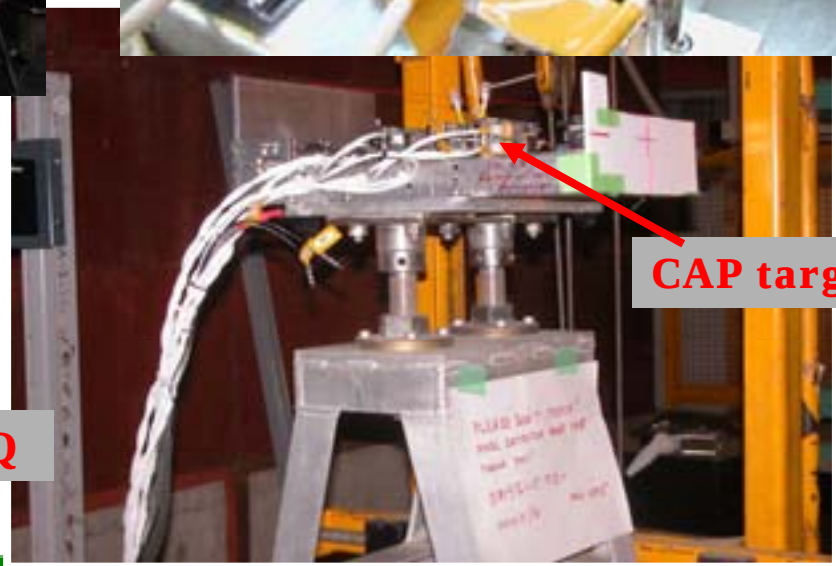
300-600Mbaud link

~1mm x 3mm

On board ADC

Jun.04 KEK Test Beam

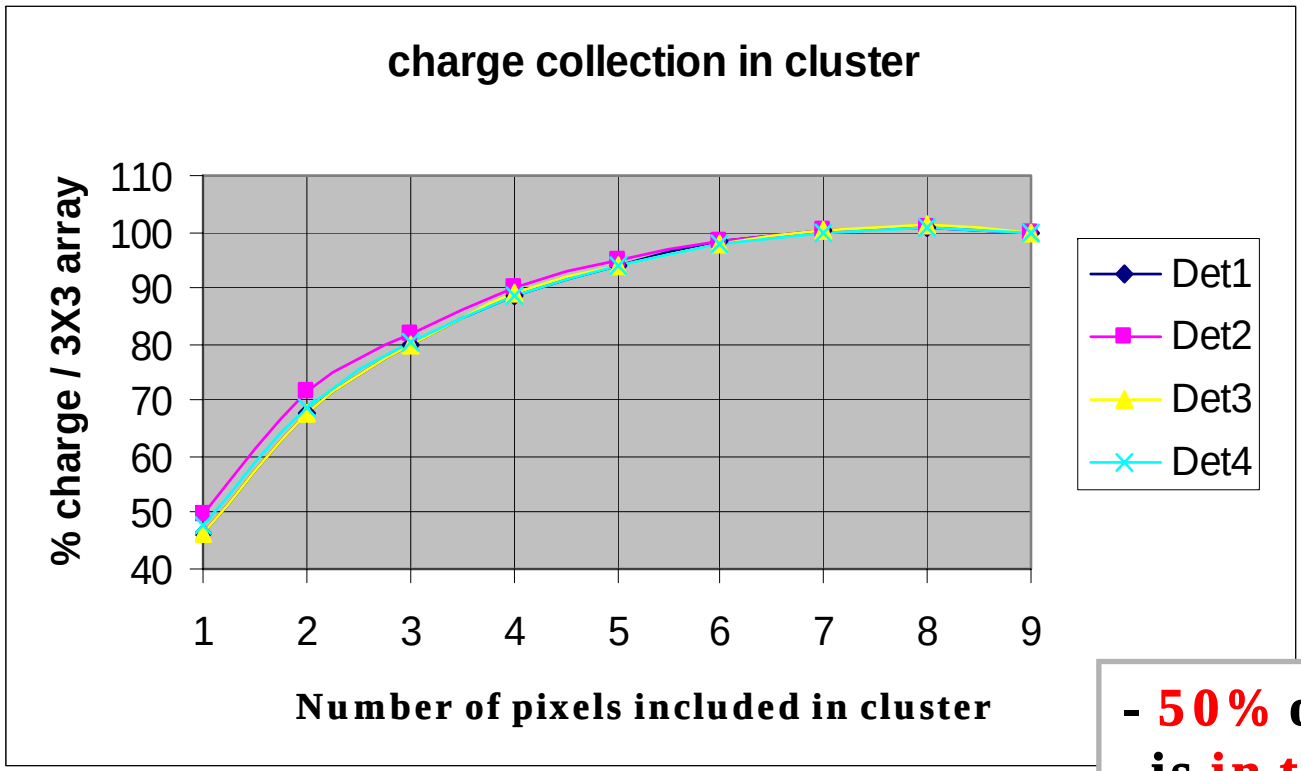




Some pixel technologies

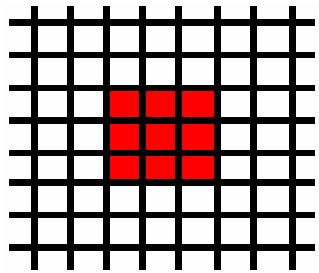
Technology:	Hybrid	CCD	MAPS	3D
Who/where?	LHC: CMS, ATLAS, ALICE	SLD, TESLA	R&D: LEPSI/ IReS, RAL, Hawaii, DESY /Hamburg, STAR,LC	S. Parker, ATLAS upgrade?
Rad-hard?	Yes	Rad-soft	to be demonstrated	Very
Speed?	25ns bunch	Slow?	we'll get back to that	Fast
Thickness?	Sensor + RO Chip ~500µm+	Thin	Sensor/electronic (SoC) . Can be thinned to <50µm.	Sensor + RO Chip ~500µm+
Process ? (hence costs?)	ROC process (+ special techniques)	Standard process	Standard process	Custom made
Development status	Relatively well "established" technology	well establ.	A lot of new developments in recent years	Pioneering idea

Charge Spread in CAPS



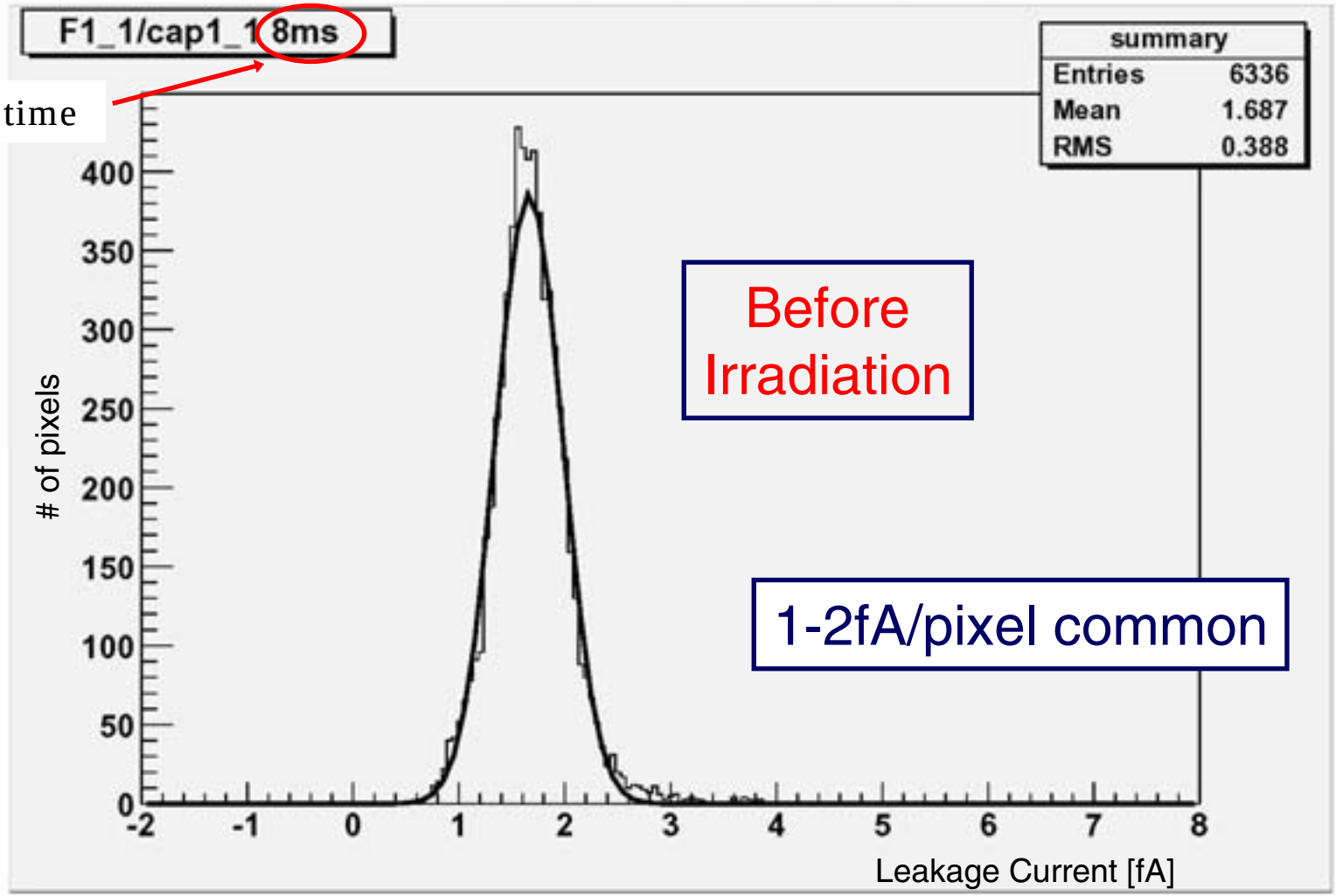
(MPV of landau fit)

Hyp: charge entirely collected in 3X3 pixel array.



- **50%** of the charge is **in the peak pixel**.
- **90%** in the **4 largest**.

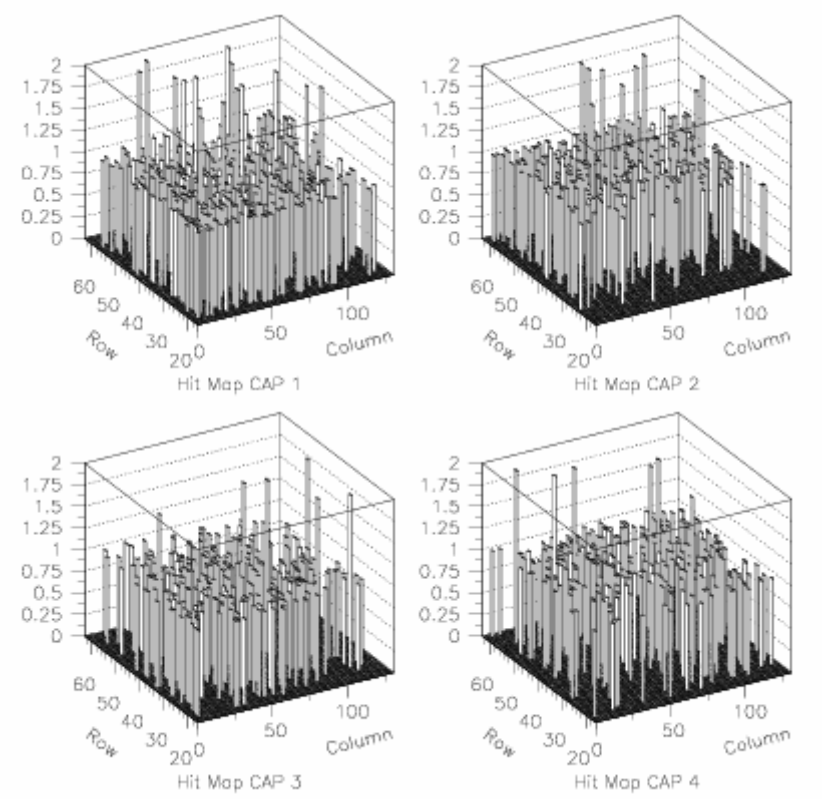
Leakage Current



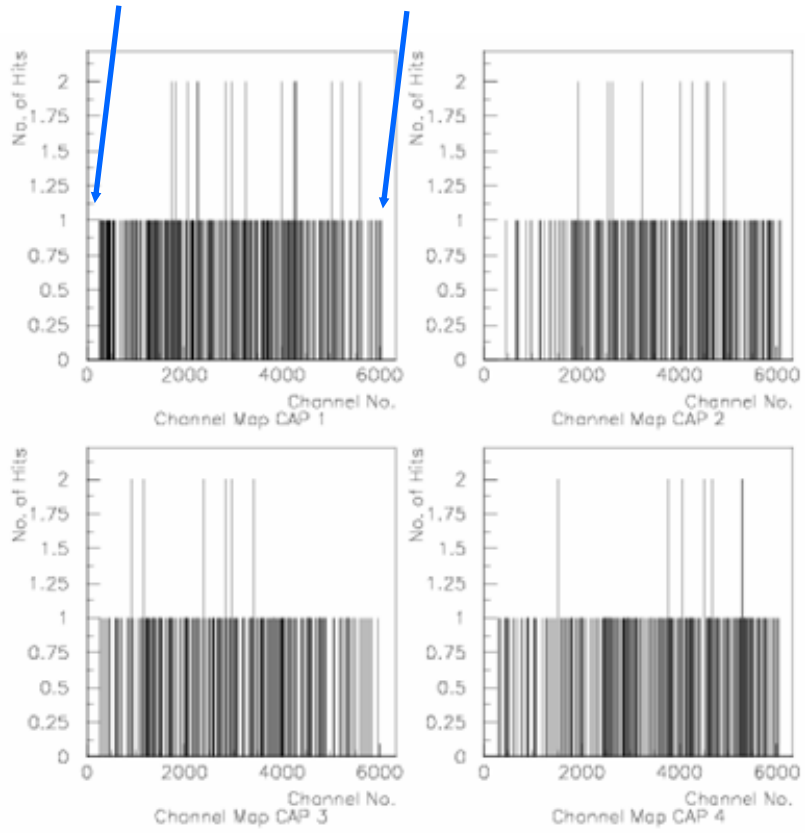
DAQ Requirements

- If use 4 fiber links/FINESSE (FC fiber connectors)
  - Only pull data from CAP at L1 trigger rate
    - Data reduction on FINESSE during readout
    - Cluster finding (plus window or direct c.o.g.?)
  - Channel/Board count:
    - 12 CAP – FINESSE links/COPPER (including downstream)
    - 3 COPPER/"SVD L1" ladder equivalent
    - 18 COPPER total (1 crate)
  - Data volume:
    - ~ 1k per CAP3 [0.5% occupancy]
    - 4-5kBytes/L1 from each FINESSE, 360kB/event total
  - Track match (Level 3)
    - 216 trigger sectors (assuming <16> candidates)
    - Total event size 25-30kB/event

Uniformity



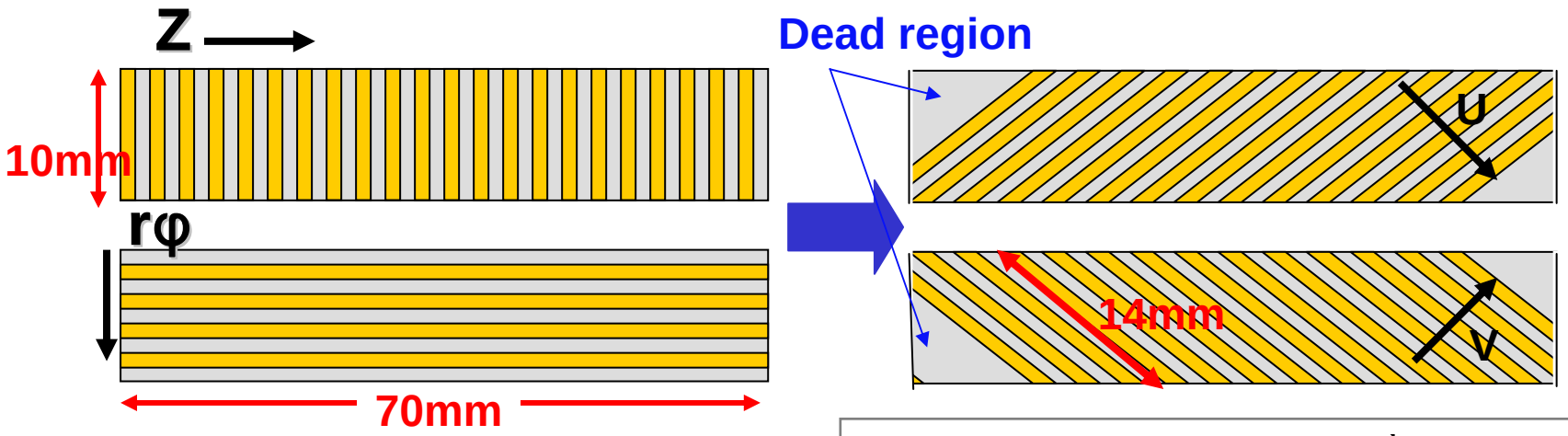
Outer 2x rows/columns excluded



<= 10 hot pixels excluded per layer

Short strip DSSD (Striplet)

- New type of DSSD: Striplets T.Tsuboyama-san & M.Hazumi-san, KEK
  - Strip length is shortened.
  - Arrange strips in 45 degrees wire-bonding eased.
  - Small triangle dead region exists (about 7 % in layer1).
  - Occupancy is reduced to ~5% @L= $10^{35}/cm^2/s$
  - Higher luminosity case needs pixel type sensor

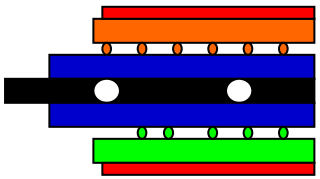


From T.Kawasaki-san, Niigita-U, 6th HL WS, 2004/11

Resolution, hybrid vs. MAPS

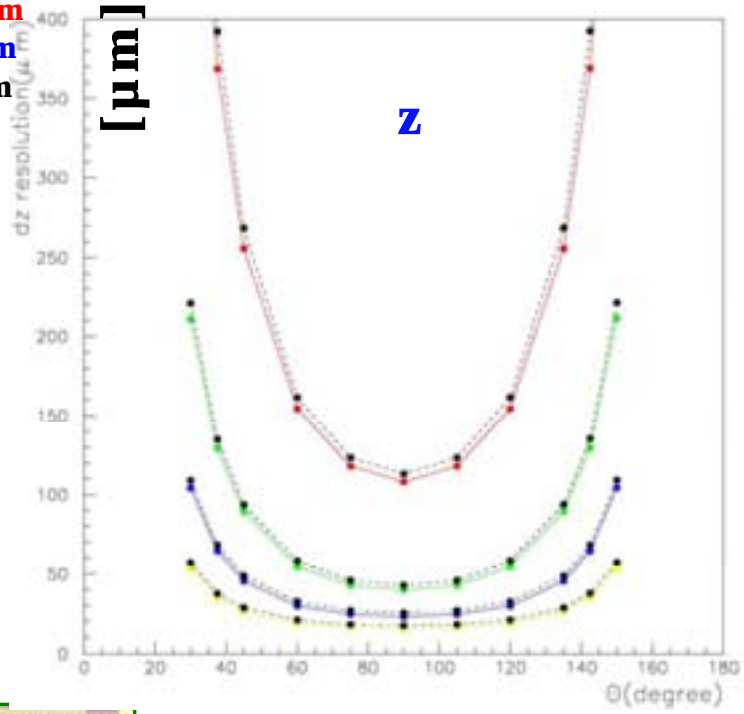
early simulation
Karim Trabelsi (UH)

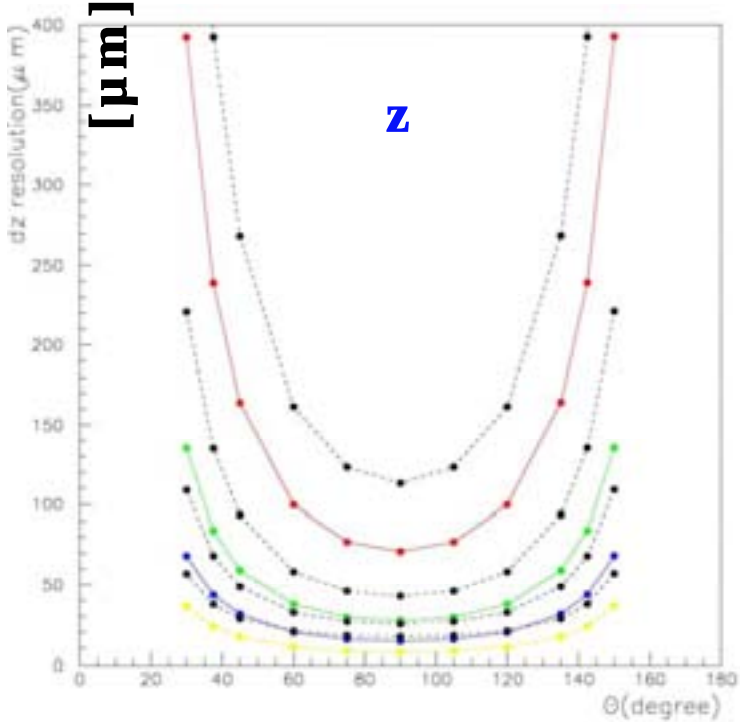
- 2 layer ALICE-type
  - Pixel size =50*400μm
  - Thickness: 700μm
- 2 layer MAPS
  - Pixel size =25*25μm
  - Thickness: 200μm



Sens 250μm
ROC 150μm
Sup 300μm

Impact parameter resolution





SVD2

0.2GeV

0.5GeV

1.0GeV

2.0GeV