CMOS - Sensor development for the ILC in Europe

Michael Deveaux (GSI/IReS), on behalf of:

IReS: A. Besson, G. Claus, C. Colledani, (G. Deptuch), M.Dorokhov, W. Dulinski, M.Goffe, D. Grandjean, F.Guilloux, A. Himmi, Ch. Hu, K. Jaaskelainen, M.Pellicioli, E. Scopelliti, A.Shabetai, M. Szelezniak, I.Valin, M. Winter (Project coordinator)

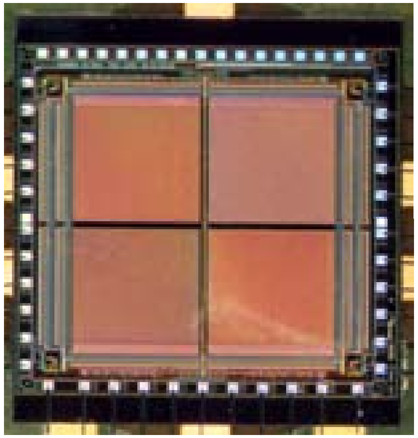
GSI/IReS: M. Deveaux, S. Heini, H. Souffi-Kebbati

CEA: Y. Dergerli, N. Fourches, Y. Li, P.Lutz, F. Orsini

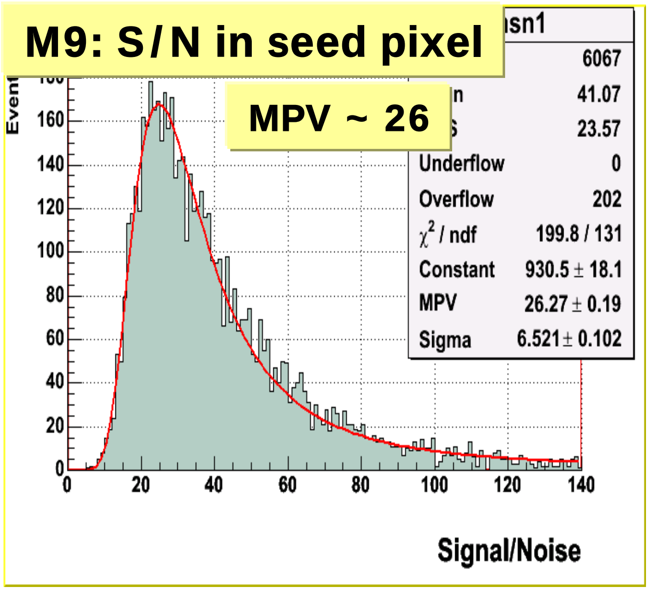
Acknowledgements to the SUCIMA collaboration

The MIMOSA - Technology

Minimum Ionizing Particle MOS Active Pixel Sensor



MIMOSA IV



Typical features of the MIMOSA – detectors:

20 µm pixel pitch, 12 bit serial readout:

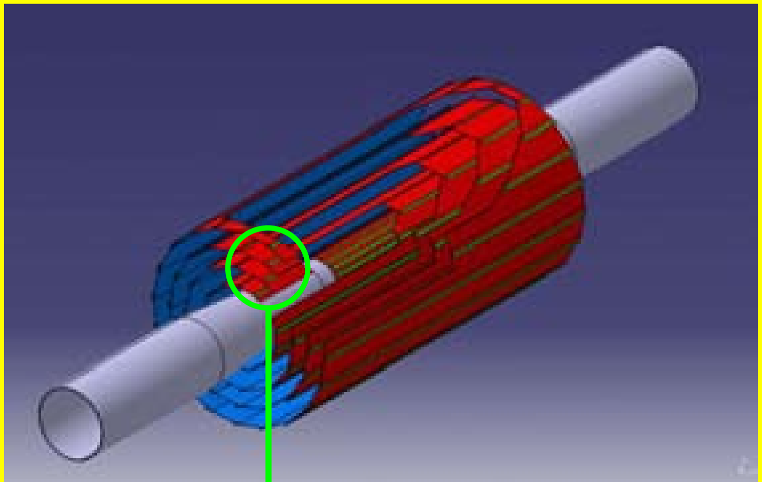
- Single point resolution 1.5µm - 2.5µm
- $\sigma_{2hits} \geq\sim 30$ µm

- S/N for MIPs (~100 GeV/c): 20-30 (MPV)
- Detection efficiency: $\varepsilon_{det} \sim 99\text{-}99.9$ %
- Standard sensor: 1MPixel, 120µm thickness
- 3 Wafers were thinned to 50µm...*
- Produced in:

  AMS-0.6µm, AMI-0.35µm, AMS-0.35µm, AMS-0.35µm opto, IBM-0.25µm, TSMC-0.25µm
- Further Applications: STAR, CBM

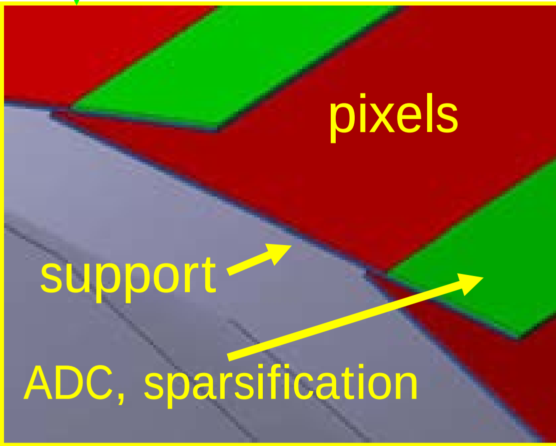
* see talk from H. Wieman, LBL

CMOS sensors in the ILC VD



Overall design a priori very similar to TESLA TDR concept (CCD):

- 5 cylindrical layer
- R = 15 – 60 mm
- surface ~ 3000 cm^2



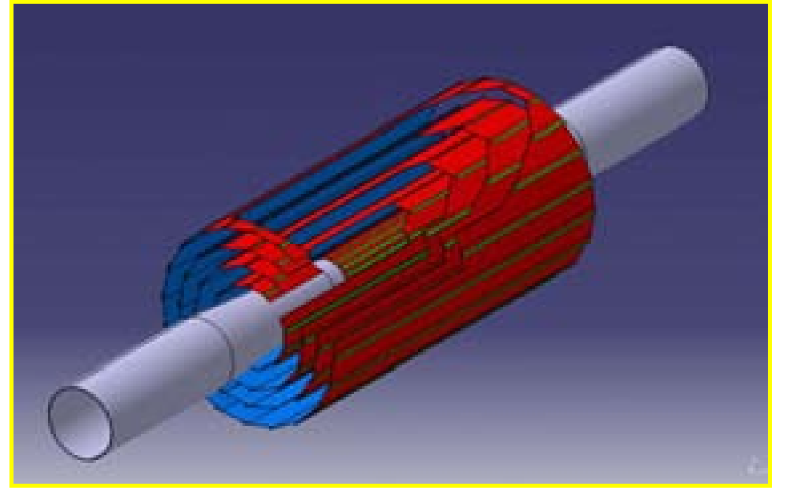
Basic characteristics:

- sensor thickness: ~ 25-50 µm
- support thickness: ~ 50 µm carbon fiber
- total number of pixels: ♦ 300 millions
- < 3-30W (full detector, 1/200 - 1/20 duty cycle)

See talk of D. Grandjean for more details

Requirements on the sensors

Expect up to ~15 hits/cm²/BX from beamstrahlung



Readout speed required:

- ~ 25 µs in Layer 0
- ~ 50 µs in Layer 1
- < 200 µs in Layer 2 - 4

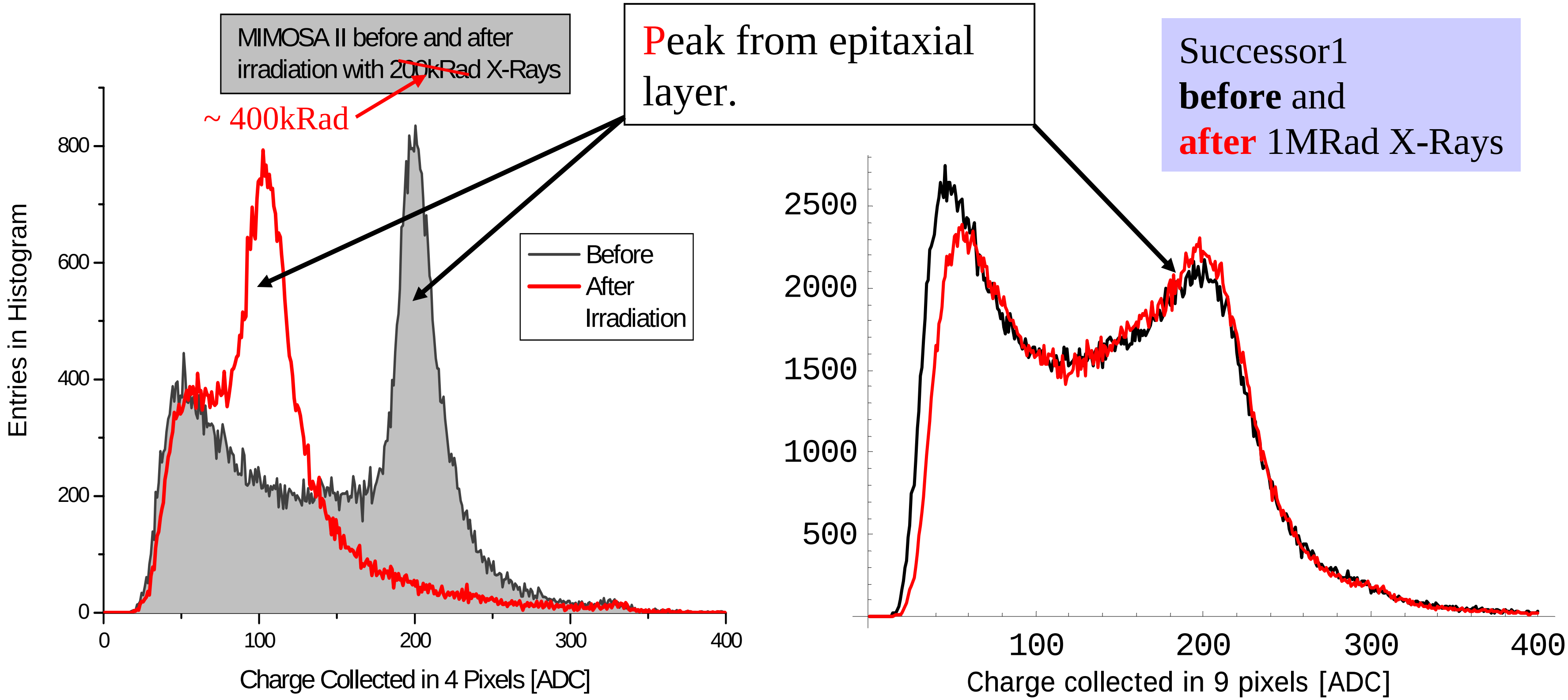
Corresponding radiation dose (3 years):

- 3×10^{10} n_{eq}/cm^2 due to neutron gas
  (safety factor = 10)
- 6×10^{12} $e^{\pm}$ $/cm^2$ due to beamstrahlung
  (2×10^{11} n_{eq}/cm^2 with mean NIEL-Factor assumed = 1/30)
- Ionising damage: ≙ 50 kRad / year

See talk of D. Grandjean for more details

Status: Resistance against ionising doses

Testing the detector with an ^{55}Fe source before and after irradiation

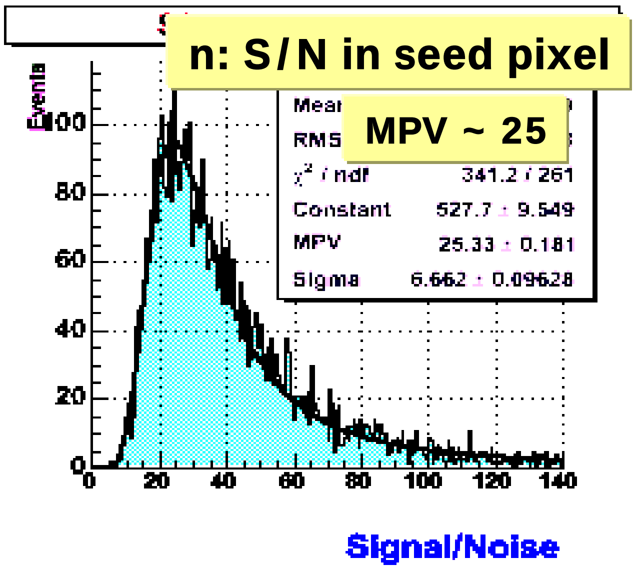


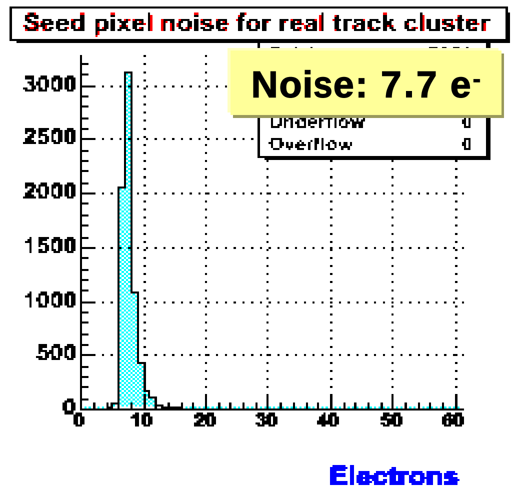
- First prototypes (MIMOSA2) were radiation soft.
- Key problem: Charge collection.
- Weak point has been identified and fixed in SUCCESSOR1
  (SUCCESSOR 1 was provided by the SUCIMA coll. – FP5)

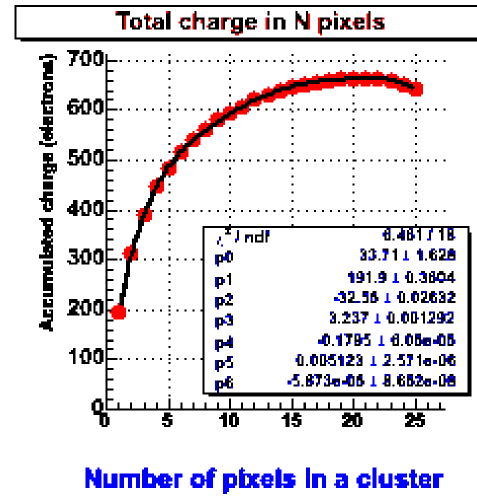
Assuming fast readout and moderate cooling, 1MRad can be tolerated.
Technology improvements for room temperature operation under study (Mi11,15)

Status: Tolerance to neutron irradiation

Beam test on MIMOSA9 irradiated with 10^{11} n_{eq}/cm^2 (1MeV)







Preliminary calibration

(Absolute numbers on S and N not valid, relative numbers and S/N OK)

20 µm pixel pitch, -20°C, 3.4 x 4.3 µm² diodes

Equivalent to ♦ 10 years of operation at the ILC:

- Efficiency: 99.97 +/- 0.02 %
- No obvious reduction in charge collection
- No obvious increase of noise (-20°C)

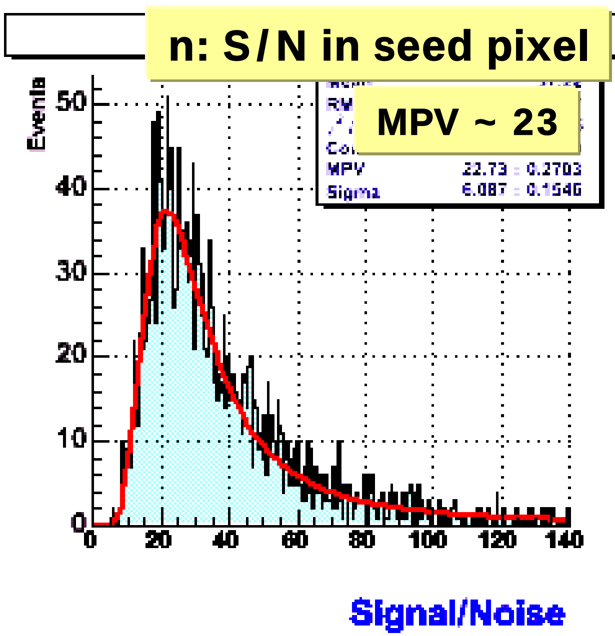
were observed.

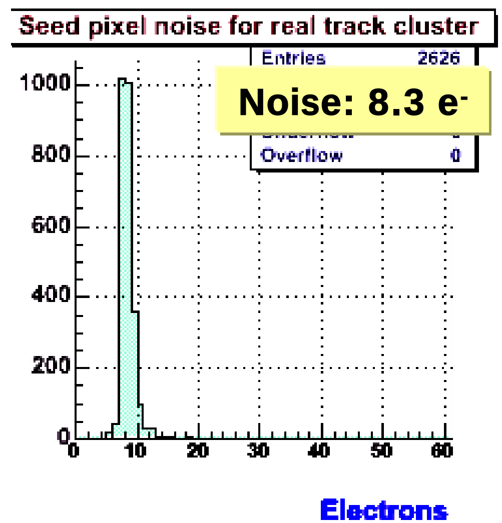
S/N and detection efficiency remain excellent.

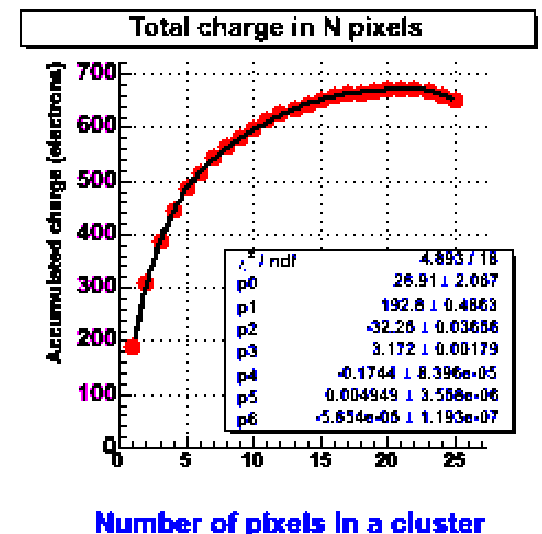
10^{12} n_{eq}/cm^2 has also been tested with very good results

Status: Resistance against electron doses

Beam test on MIMOSA9 irradiated with 10^{13} e^-/cm^2 (~10 MeV)







Preliminary calibration

(Absolute numbers on S and N not valid, relative numbers and S/N OK)

20 µm pixel pitch, -20°C, 3.4 x 4.3 µm² diodes

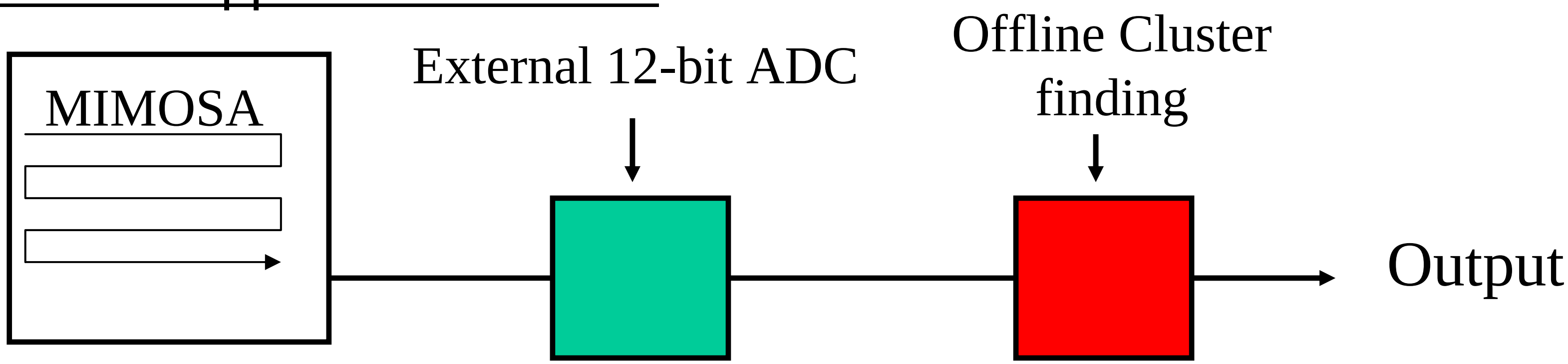
Equivalent to ♦ 5 years of operation in the ILC (with safety factor 3):

- Detection efficiency = 99.4 +/- 0.2 %
- Charge collection slightly degrades
- Noise slightly increases (-20°C).

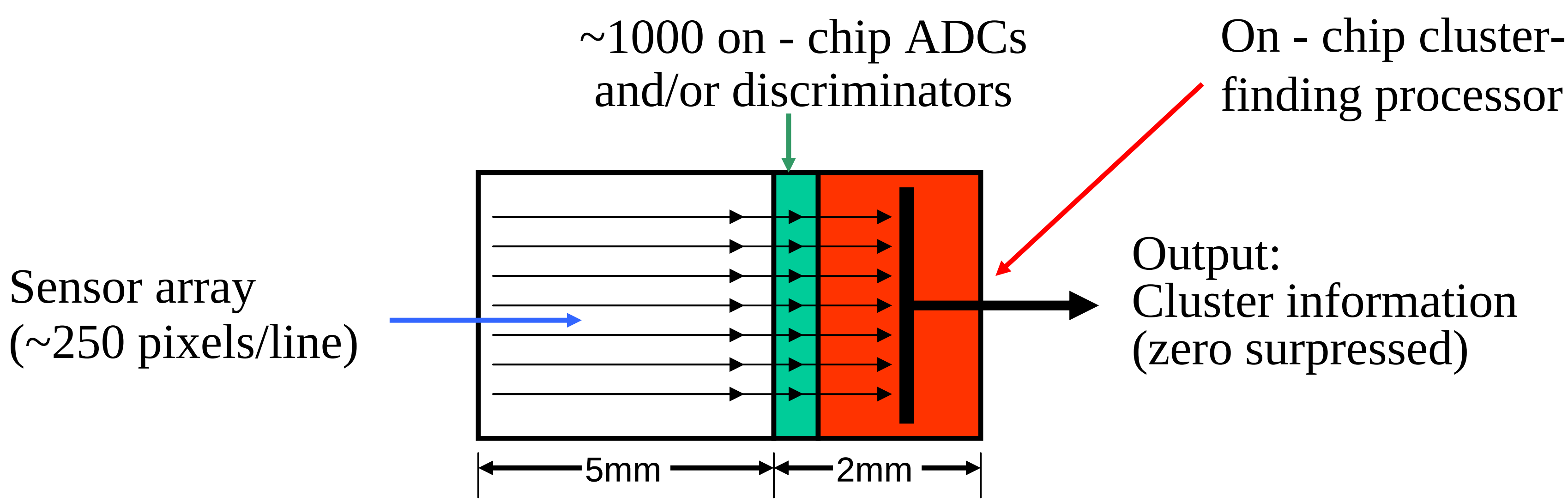
S/N and detection efficiency remain excellent

Fast readout speed, the inner layers

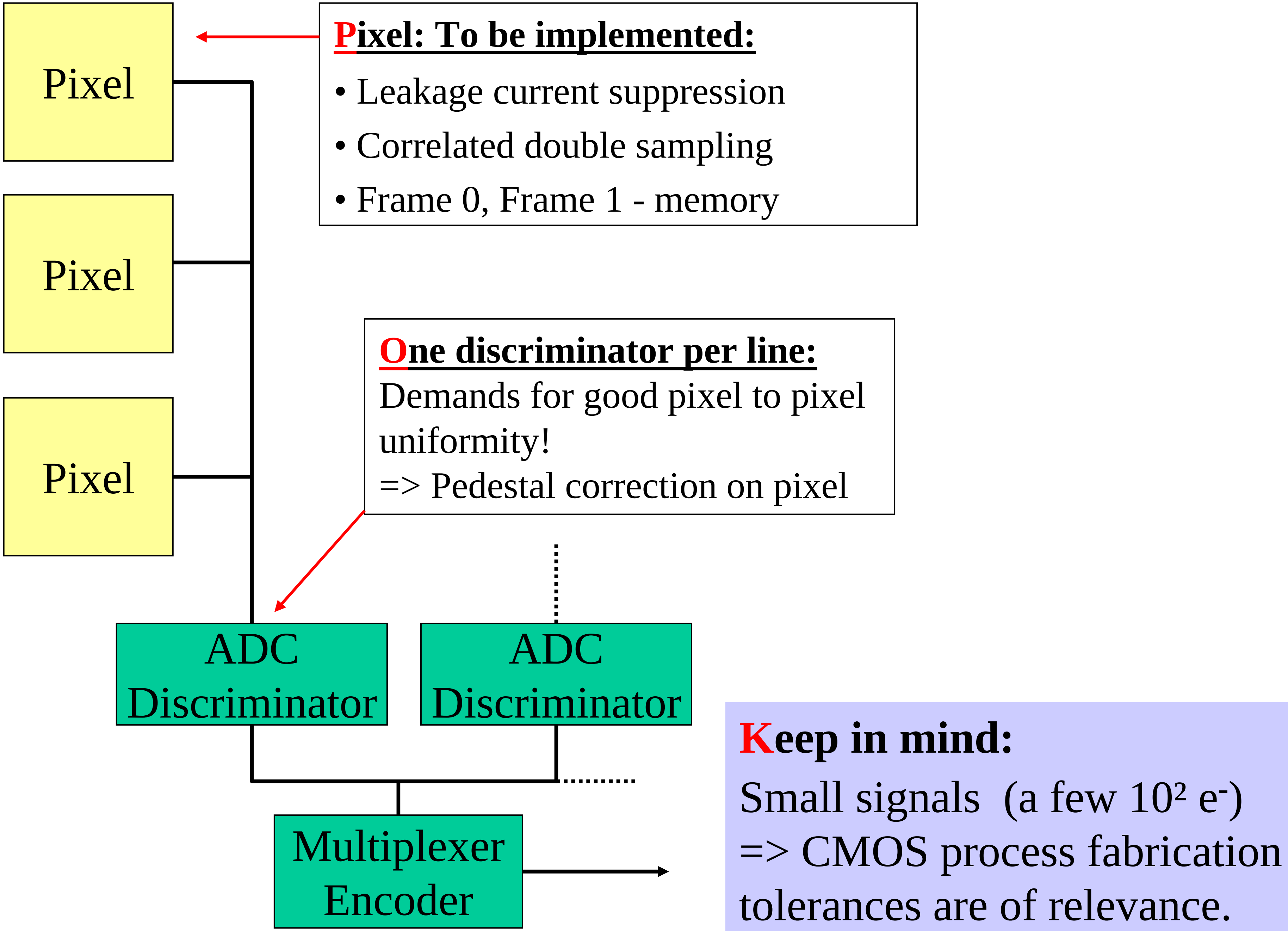
Standard approach for MAPS:



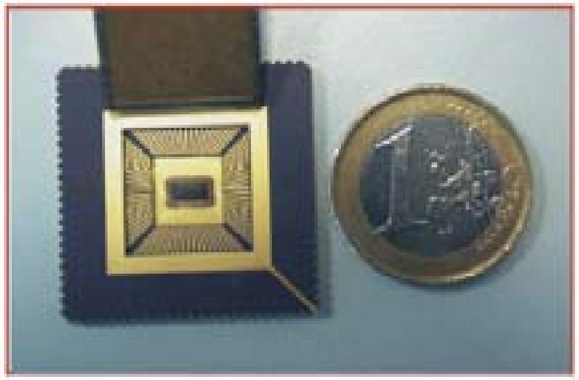
The design concept for the ILC inner layers:

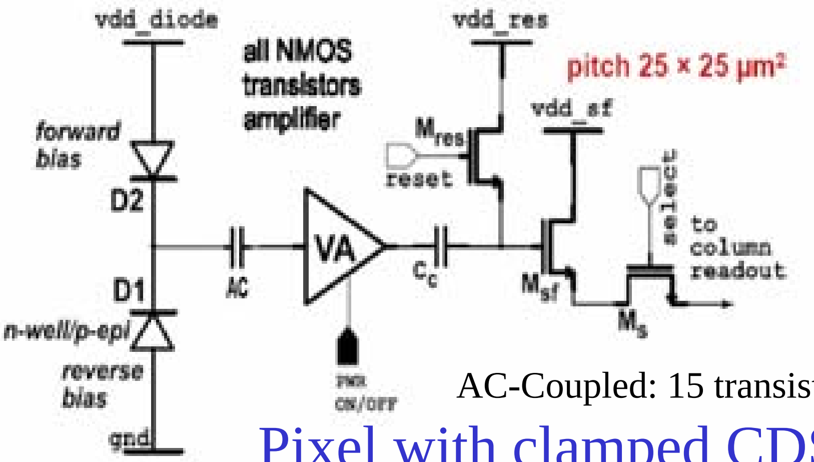


Goal: A readout time of ③ 25µs for the ILC


Pixel
Pixel
Pixel
Pixel: To be implemented:
• Leakage current suppression
• Correlated double sampling
• Frame 0, Frame 1 - memory
One discriminator per line:
Demands for good pixel to pixel uniformity!
=> Pedestal correction on pixel
ADC Discriminator
ADC Discriminator
Multiplexer Encoder
Keep in mind:
Small signals (a few 10^2 e^-)
=> CMOS process fabrication tolerances are of relevance.

MIMOSA8, a MAPS with on - pixel CDS





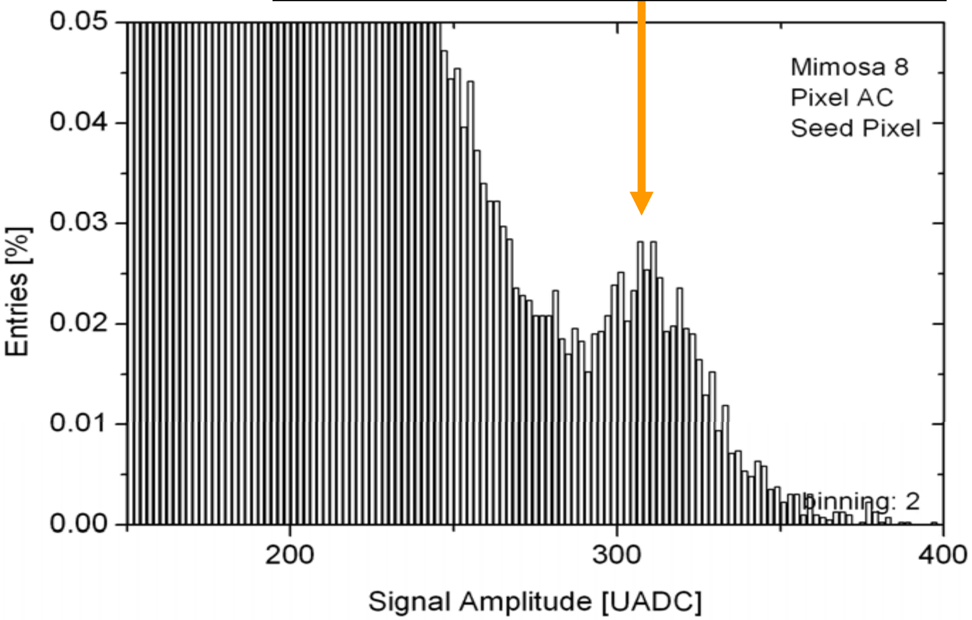
AC-Coupled: 15 transistors

Pixel with clamped CDS

MIMOSA8

- TSMC 0.25µm process (8µm epi)
- 128 x 32 pixel
- On pixel CDS
- On chip discriminators
- fully parallel readout
- **20µs readout time (128 pixels)**

Clear calibration peak
=> Low pixel to pixel dispersion



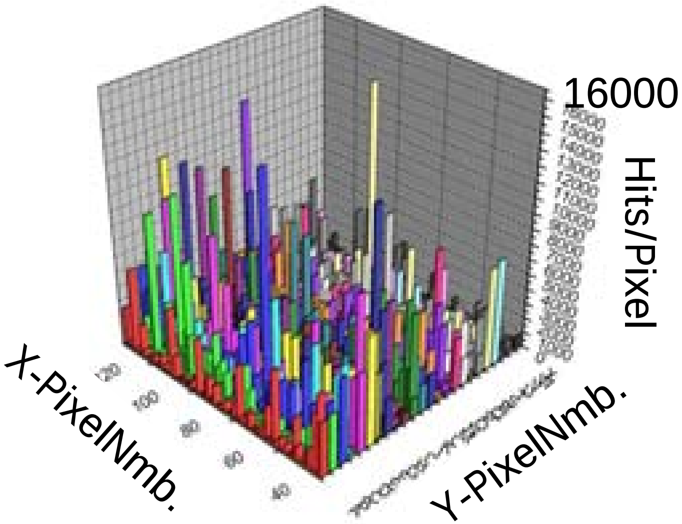
Preliminary results

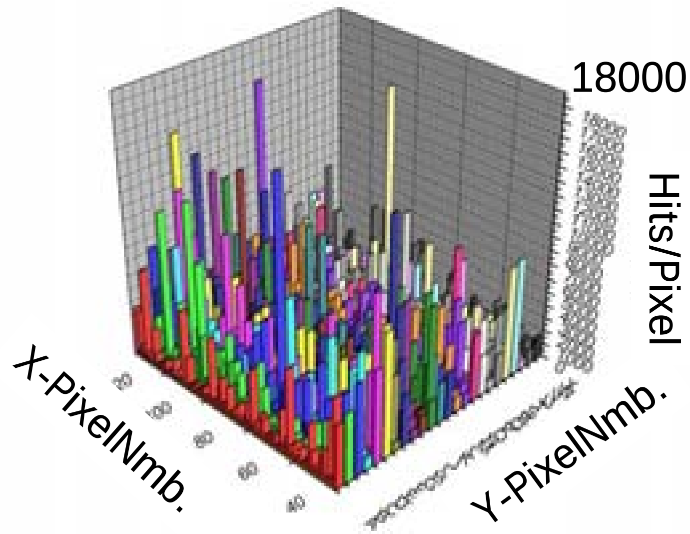
- Signal: ~50-110 µV/e^-
- Noise: ~ 13-18 e^- (Pixel)
  ~ 3- 8 e^- (Dispersion)
- CDS: OK
- Pedestal Correction: OK

MIMOSA8: Discriminator tests

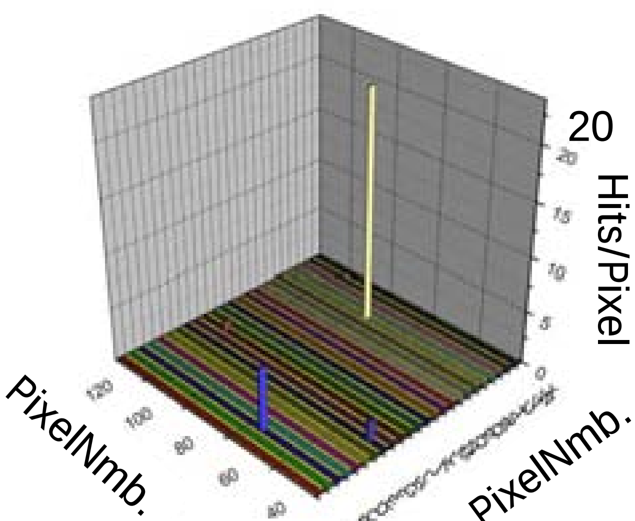
100kEvents

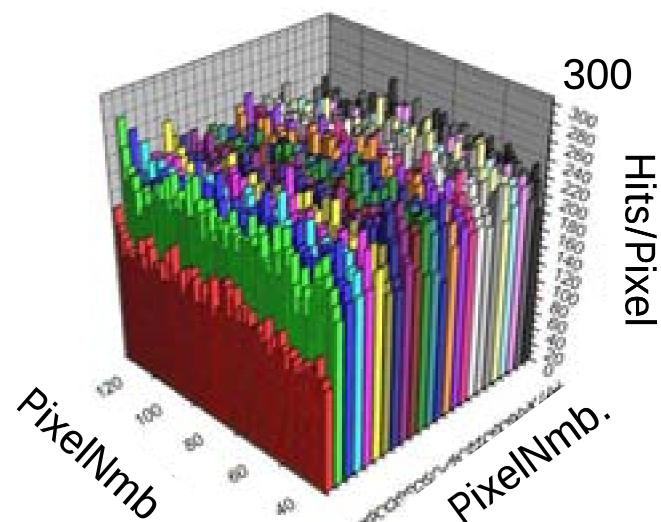
Without ^{55}Fe source | With ^{55}Fe source





V_{th}=5mV





V_{th}=10mV

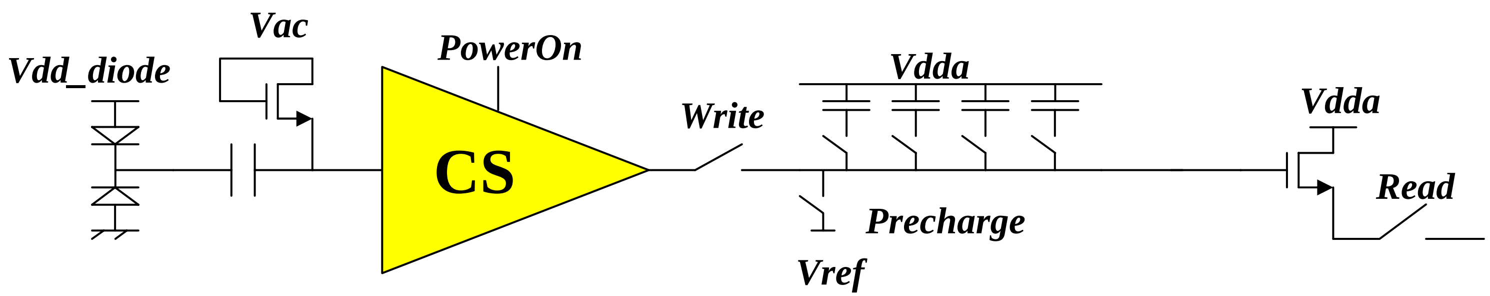
MIMOSA8: Integrated CDS + Discriminator

Next steps: Production of ADCs

- 4 – bit seem most adapted for the MAPS on chip ADCs
- Several dedicated designs are under study:
  2 ramp Wilkinson ADC, flash ADC, semi flash ADC, etc.
- Institutes involved in this development:
  IReS (Strasbourg), LPCC (Clermont-Ferrand), LPSC (Grenoble), Dapnia (Saclay)

Status: First submissions are planned for September

Moderate readout speed: The outer layers



Basing on the FAPS-approach proposed by R. Turchetta:

Within a bunch train:

- Integrate charge with short integration time
- Save charge in analogue memory cells in the pixel (capacitors)

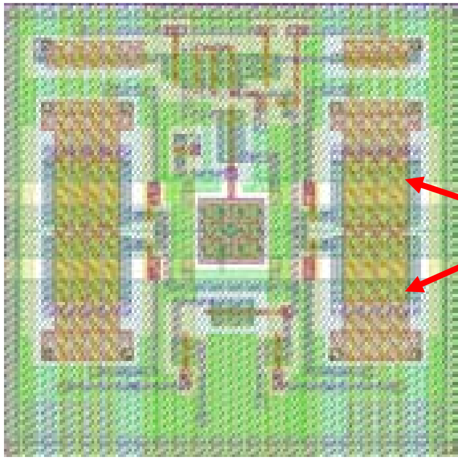
Readout memory cells slowly between the bunch trains.

+ Simpler readout due to reduced data flux
+ Low complexity with respect to previous approach

- Number of memory cells is limited by the size of the capacitor
- This limits the readout speed (frames per buch-train)

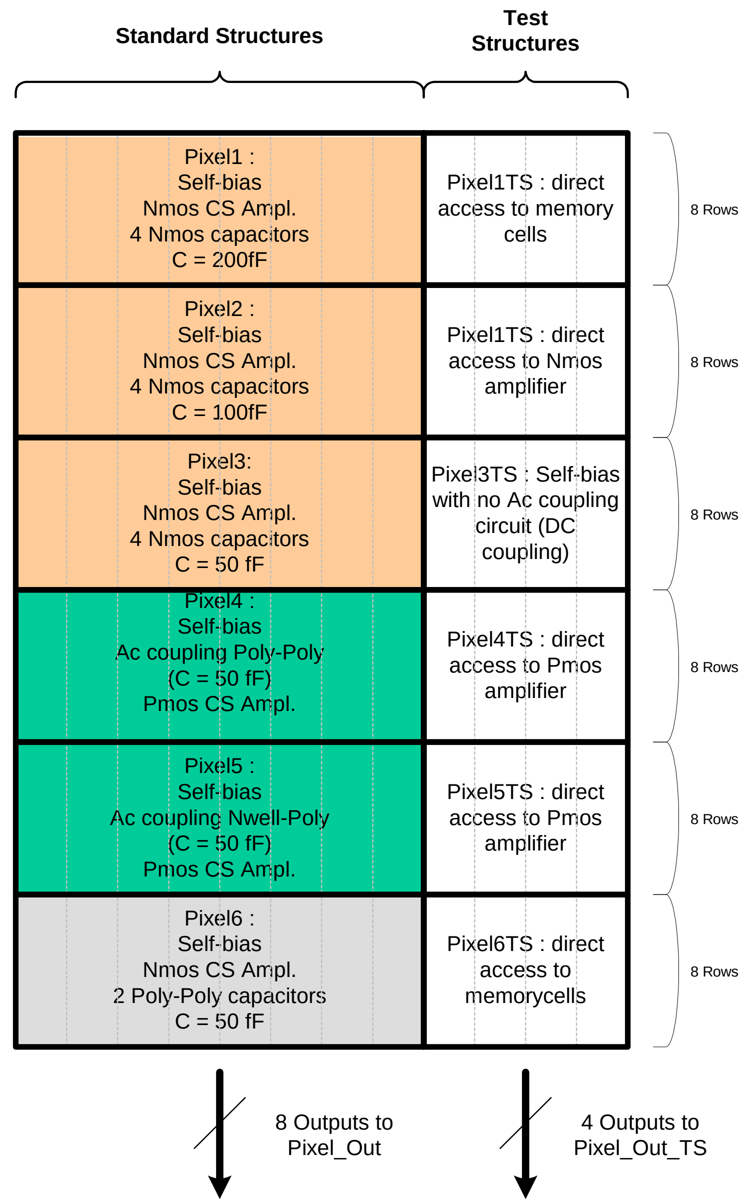
Most probably too slow for the inner layers but ok for the outer ones

MIMOSA-12: Multi memory cell pixels



100 fF capacitor
(memory cell)

Mimosa-12 pixel

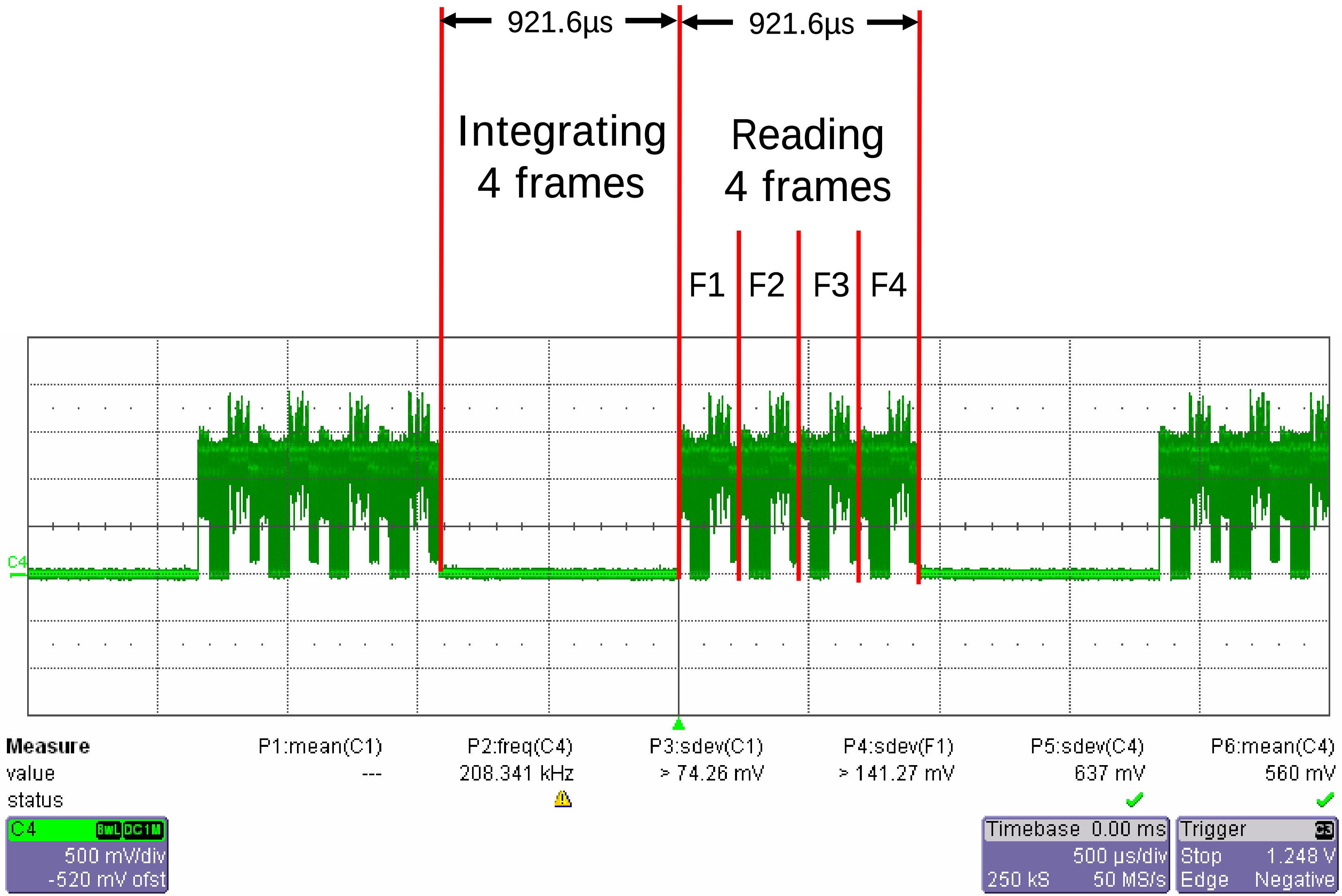


MIMOSA-12:

- AMS - 0.35 µm high resistivity
- 4 capacitors / pixel (35 µm pitch)
- 6 sub-arrays pixels with
  50, 100, 200 fF capacitors
  2 different amplifiers
  1 clamping architecture
- 6 test structures (incomplete pixels to test components)

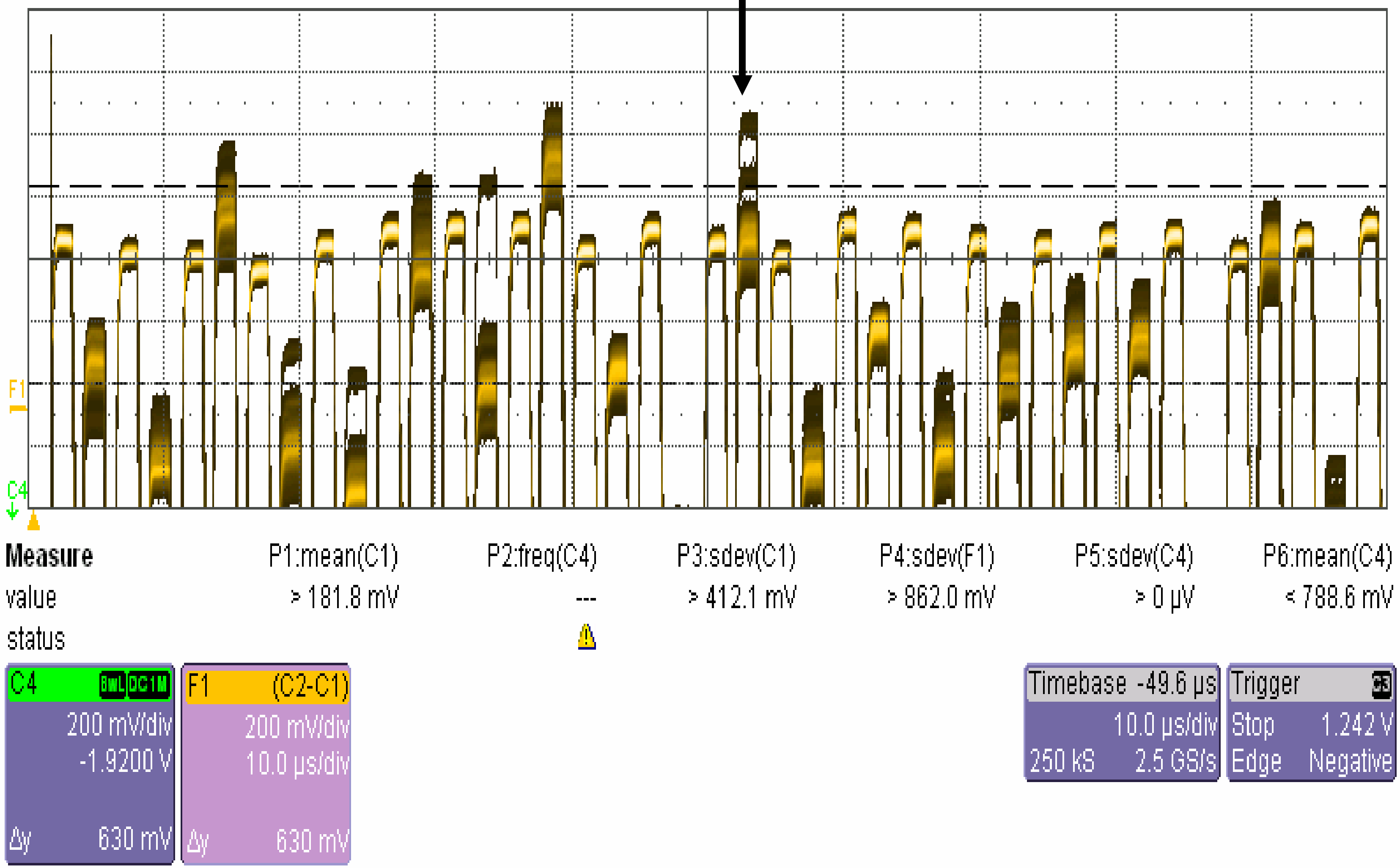
MIMOSA-12: Multi memory cell pixels

Very first tests with an oscilloscope:

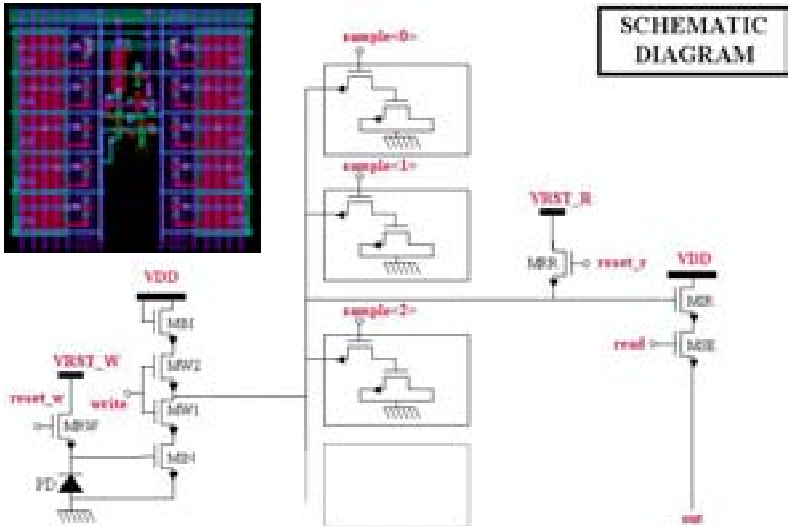


MIMOSA-12: Multi memory cell pixels

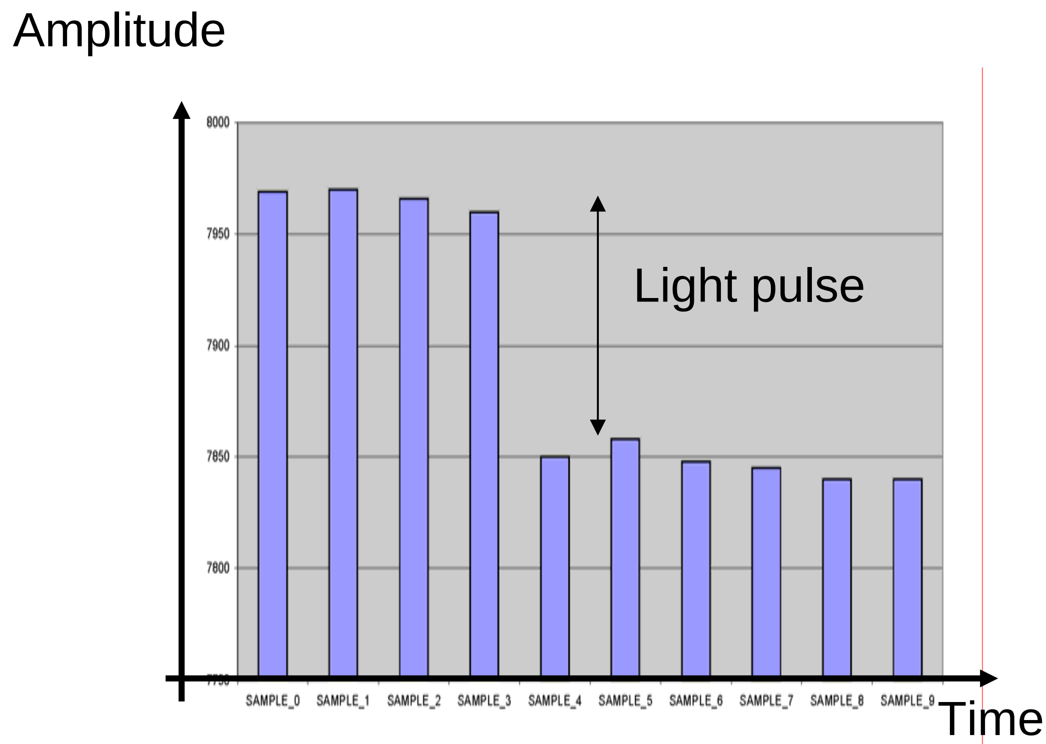
Hit from a ^{55}Fe source on pixel with internal gain 10x and 100fF



Flexible Active Pixel Sensor



Pulses LED test



10 memory cell per pixel

28 transistors per pixel

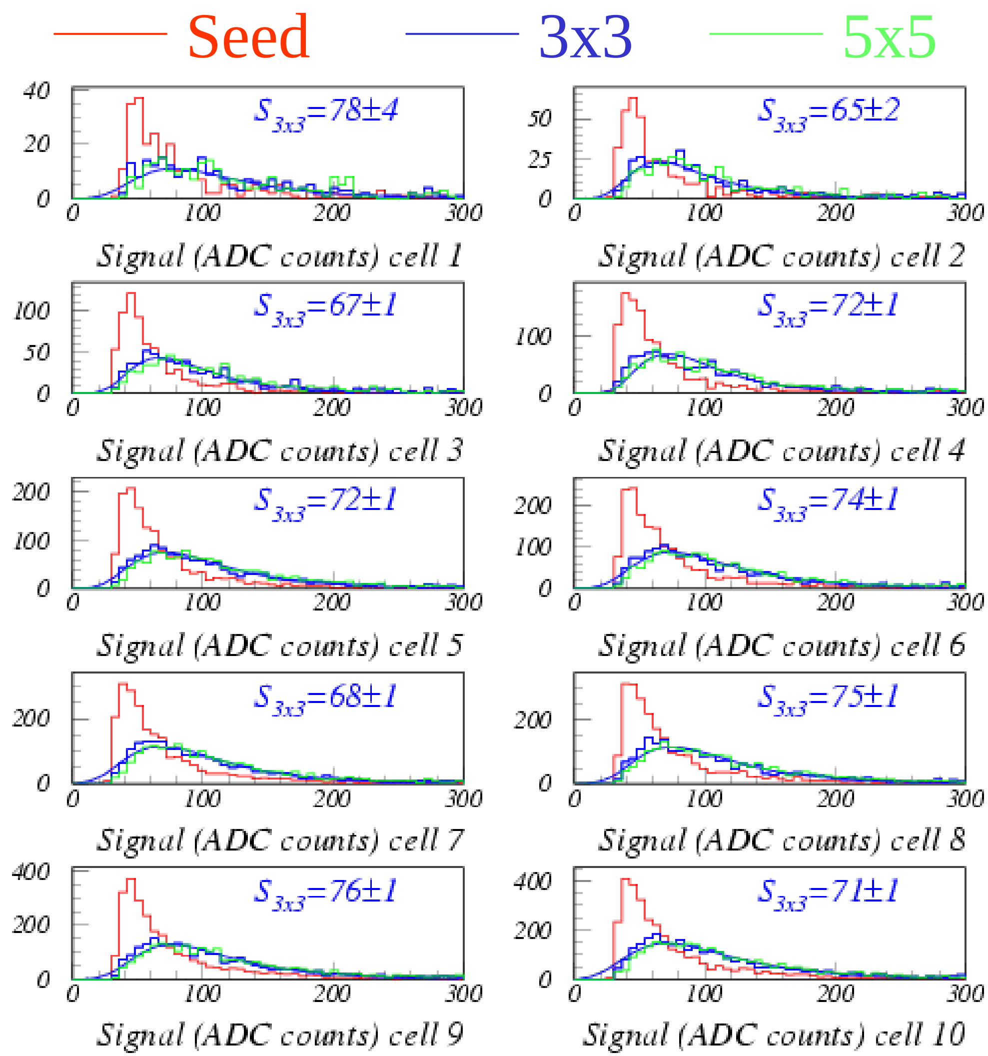
20 µm pitch

40x40 arrays

Design for the Vertex detector at the International Linear Collider

FAPS source test

- Source test
- Correlated Double Sampling readout (subtract $S_{cell\ 1}$)
- Correct remaining common mode and pedestal
- Calculate random noise
  - Sigma of pedestal and common mode corrected output
- Cluster definition
  - Signal $>8\sigma$ seed
  - Signal $>2\sigma$ next
- Note hit in cell *i* also present in cell *i+1*.
- S/N_{cell} between 14.7 ± 0.4 and 17.0 ± 0.3



J. Velthuis (Liv)

Other development lines

MIMOStar2:

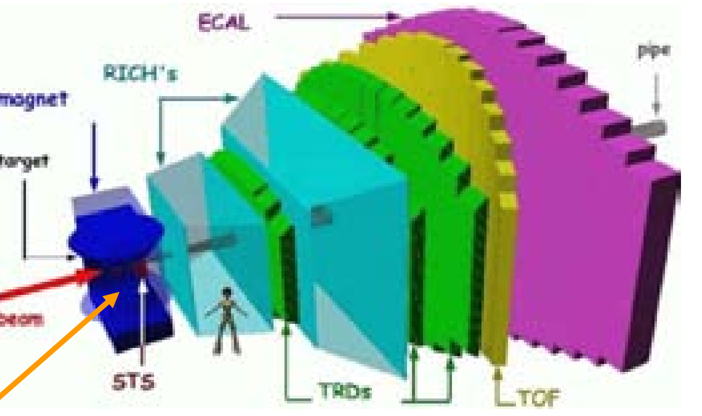
- 128x128 pixels, 30µm pitch,
- 4ms readout time (serial readout).
- Optimized for Star running conditions (+40°C)

Status: To be tested

MIMOSA11:

- 4x42x42 pixels, 30µm pitch, serial readout.
- Driven by requirements of FAIR/CBM
- Optimized for radiation tolerance >>1MRad

Status: Promising beamtest has been done.
Radiation tolerance under study



CBM @ GSI / Darmstadt
Exploration of the nuclear phase space diagram.
www.gsi.de/fair/experiments/CBM

MIMOSA15:

- Even more radiation tolerant pixels then in MI-11.
- Pixels with optimized clamping.
- Pixels with new sensors in current mode
- Pixels optimized for electron microscopes*

Status: Submitted for production

MIMOSA13:

- Readout in current mode
- Optimized readout speed

Status: To be tested

EUDET telescope:

- Macroscopic prototype
- Digital readout

Status: Planned for 2007

* As proposed by P.Rehak, BNL

UK-MAPS: Conclusion and Plans

Parametric test sensors used to test new designs, noise, rad hardness

- MIP detection with good S/N for 3-4 MOS devices, up to >10^{14} p cm^{-2}
- MIP detection with good S/N for FAPS

Beam test on RAL_HEPAPS2 (3/4MOS, FAPS, irradiated sensors) → under study

RAL_HEPAPS4. Large sensor (~1k * 384), rad-hard, high speed (5 MHz per row) → in production

Future: Working with LCFI to investigate in-pixel storage architecture (FAPS) for the ILC

Summary and Conclusion

Radiation doses on the ILC- VTX – detector (3 years):

- ③ $3x10^{10}$ n_{eq}/cm^2 due to neutron gas
- ③ $6x10^{12}$ $e^{\pm}$ $/cm^2$ due to beamstrahlung ($2x10^{11}$ n_{eq}/cm^2)
- ③ Ionising damage: ③ 150 kRad

Radiation hardness of CMOS-Sensors:

- > 10^{12} n_{eq}/cm^2 against neutrons
- > 10^{13} e/cm^2 against 10 MeV electrons
- > 1 MRad against soft X - Rays

CMOS sensors stand ILC radiation doses, even if they happen to be much above the MC-predictions*.

* So far with moderate cooling, R&D under way to operate safely at room temperature.
Performances with intelligent pixels (CDS => more noise) still to be assessed

Summary and Conclusion

Readout speed requirements:

- ~ 25 µs for the inner layer, ~ 50 µs in the second one
- < 200 µs for the outer layers

Readout speed of CMOS-Sensors:

Detectors with integrated data sparsification:

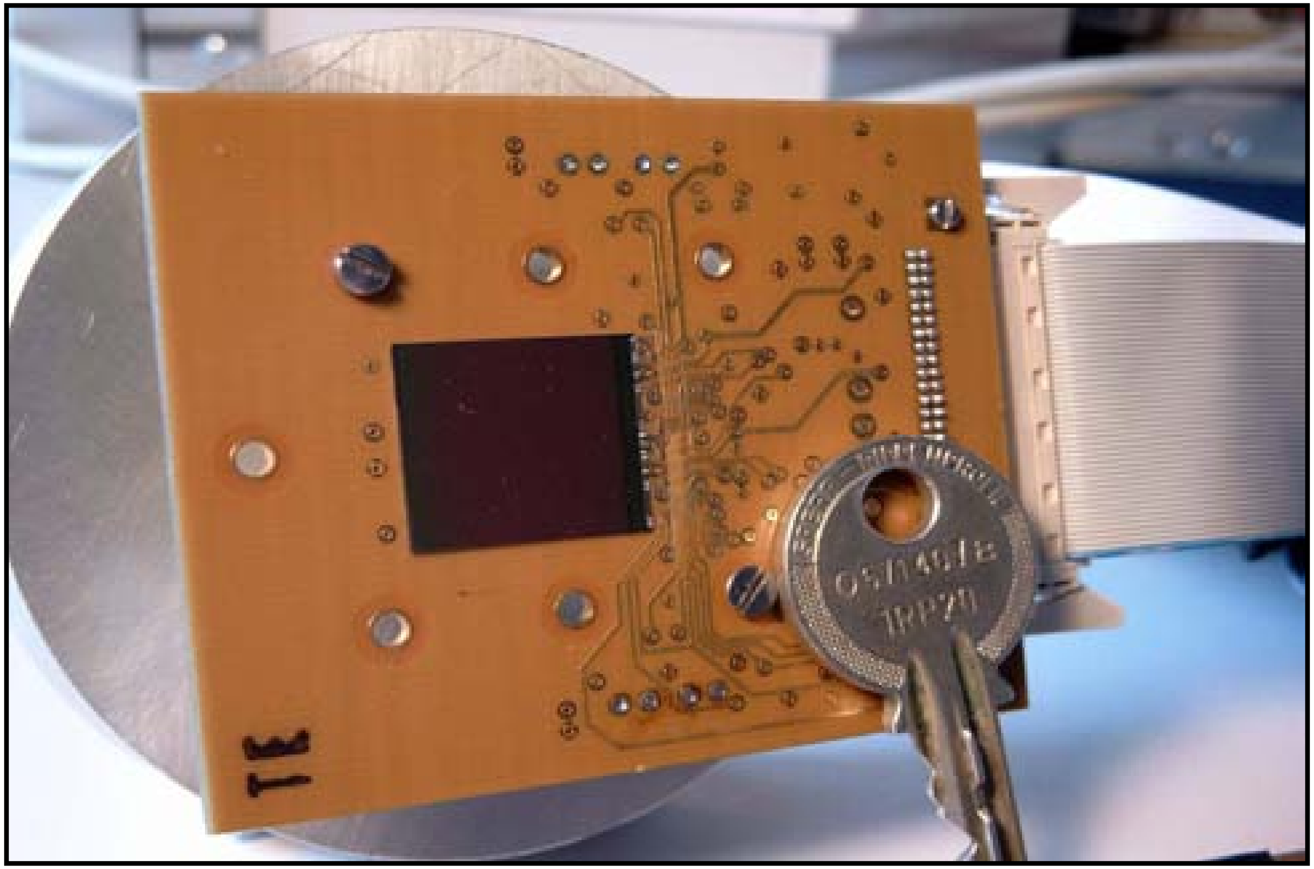
- ~ 20 µs reached with Mi8 (128 pixels/col, On-chip CDS and discri.)
- Very promising results for S/N and discriminator function
- Beam test foreseen in September
- ADC-designs now under study (first submissions planned in Sept.)

Detectors relying on FAPS approach (On-pixel memory cells):

- A first detector has been built.
- Analogue and digital structures work.
- First hits were seen (prove of principle) on oscilloscope.
- Refined tests are under preparation

Design of a fast architecture is on a good way (=> EUDet 2007).

Thank you



MIMOSA V

1 MegaPixel, resolution < 2µm

MIMOSA8 (fck = 7.5MHz, Vth = +6mV)

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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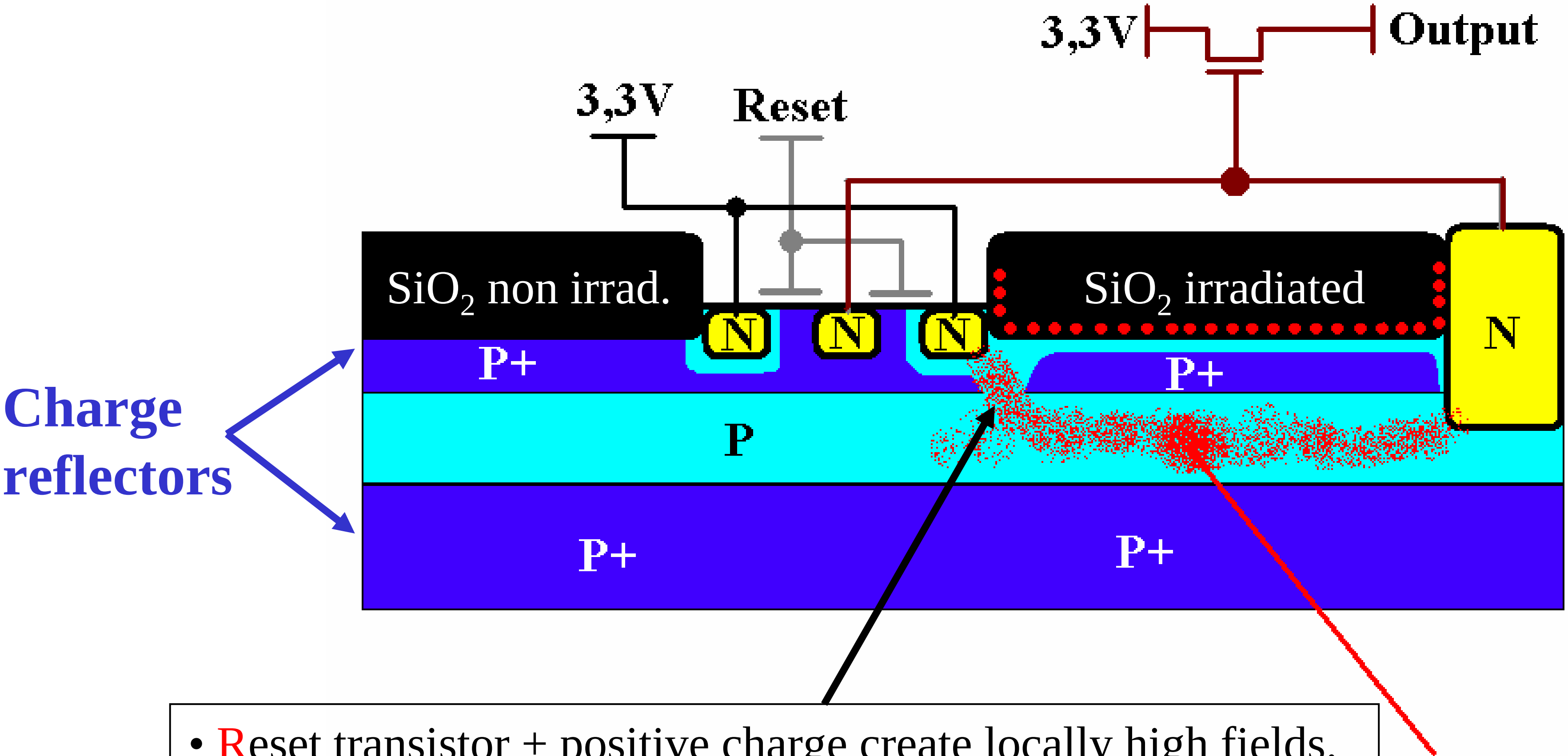
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

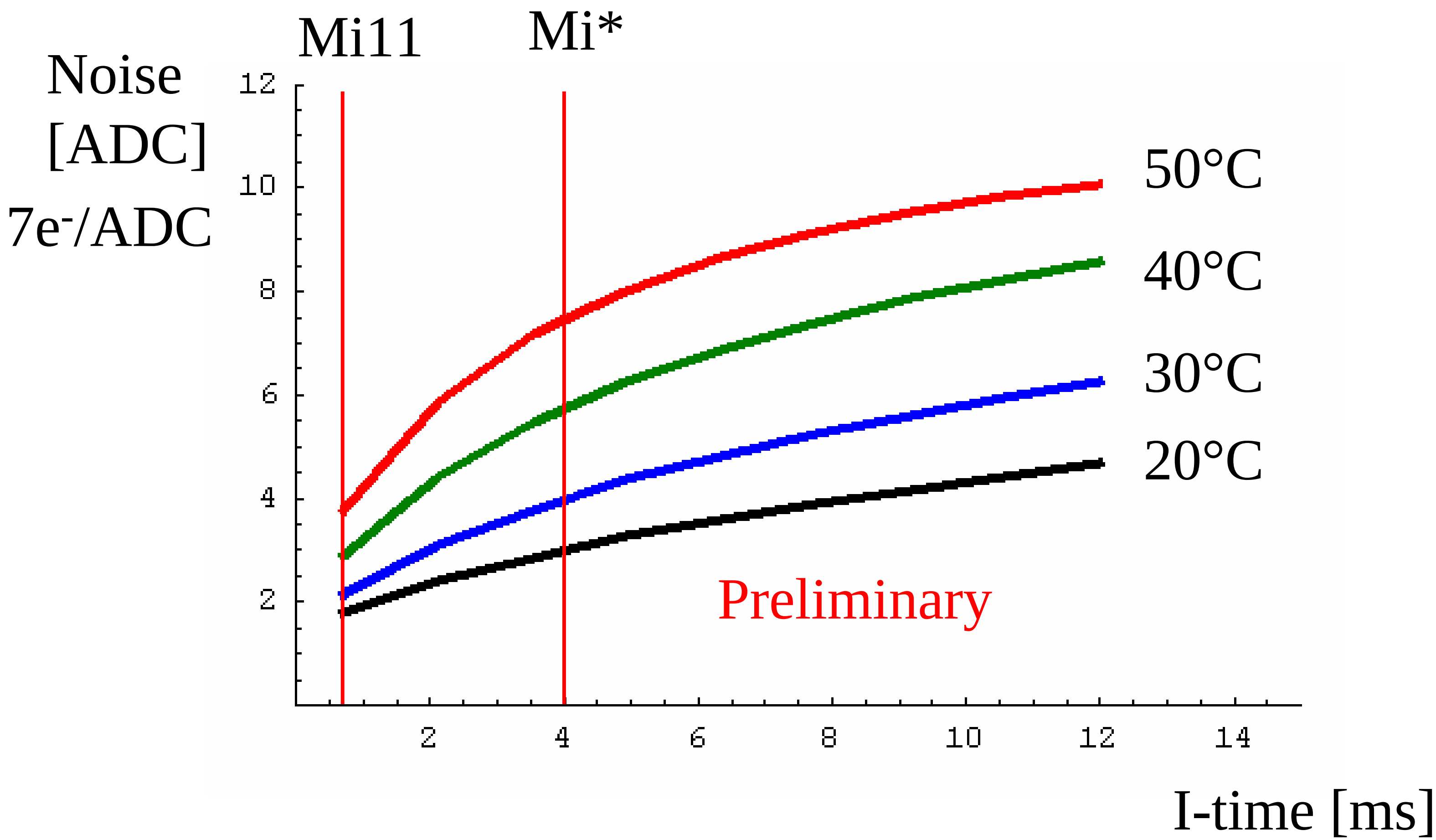
A working hypothesis:

!!Pixel without RESET-Transistor stays OK!!



- Reset transistor + positive charge create locally high fields.
- P-Well barrier gets depleted.
- Parasitic charge collection by the Reset-Transistor.

Result on A0, Sub1 after 23kRad



What stands MAPS for?

CMOS – Monolithic Active Pixel Sensors

Monolithic:

Read-out electronics and sensors are integrated on the same substrate.

Active Pixel :

An amplifier is integrated into each pixel

Sensor

MAPS were developed for visible light applications by industry.

MAPS are produced with cheap standard CMOS-processes.

The operation principle of MAPS

Sensor design:

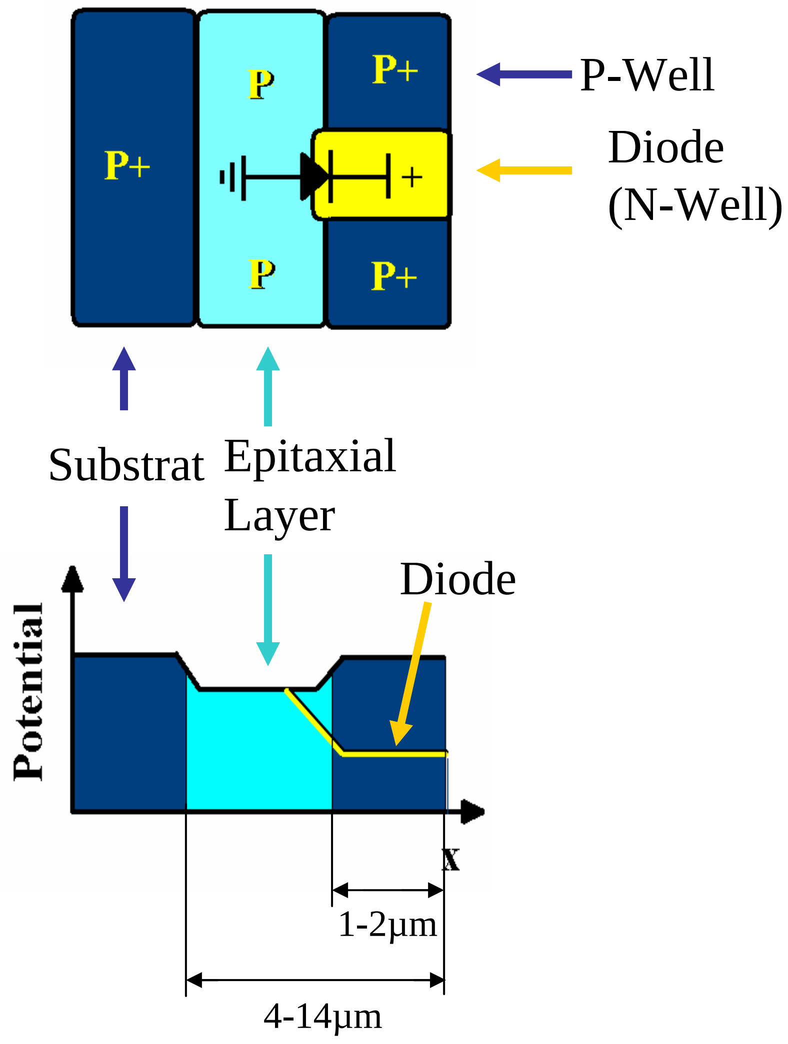
A

Minimum

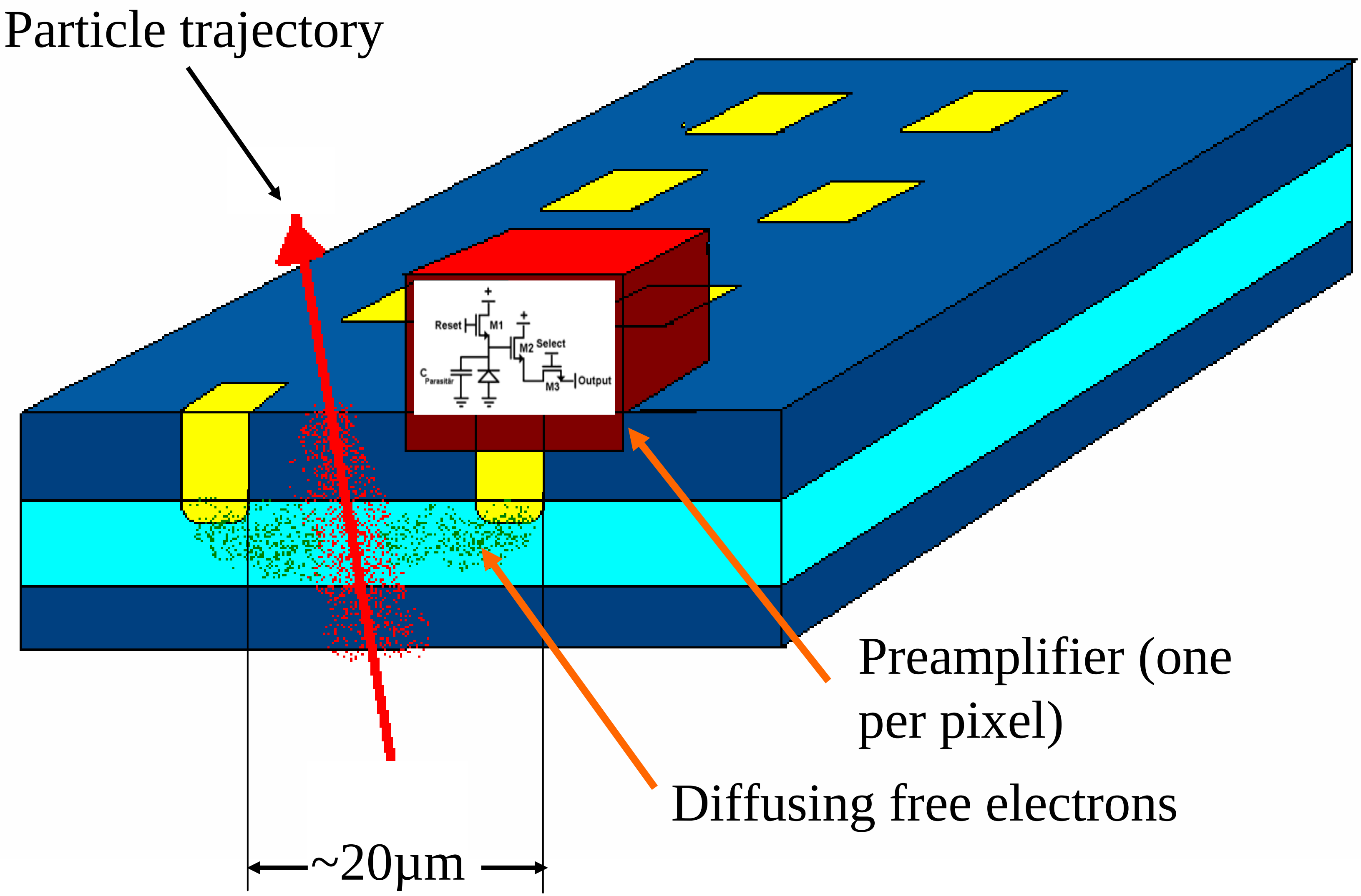
Ionising

Particle creates

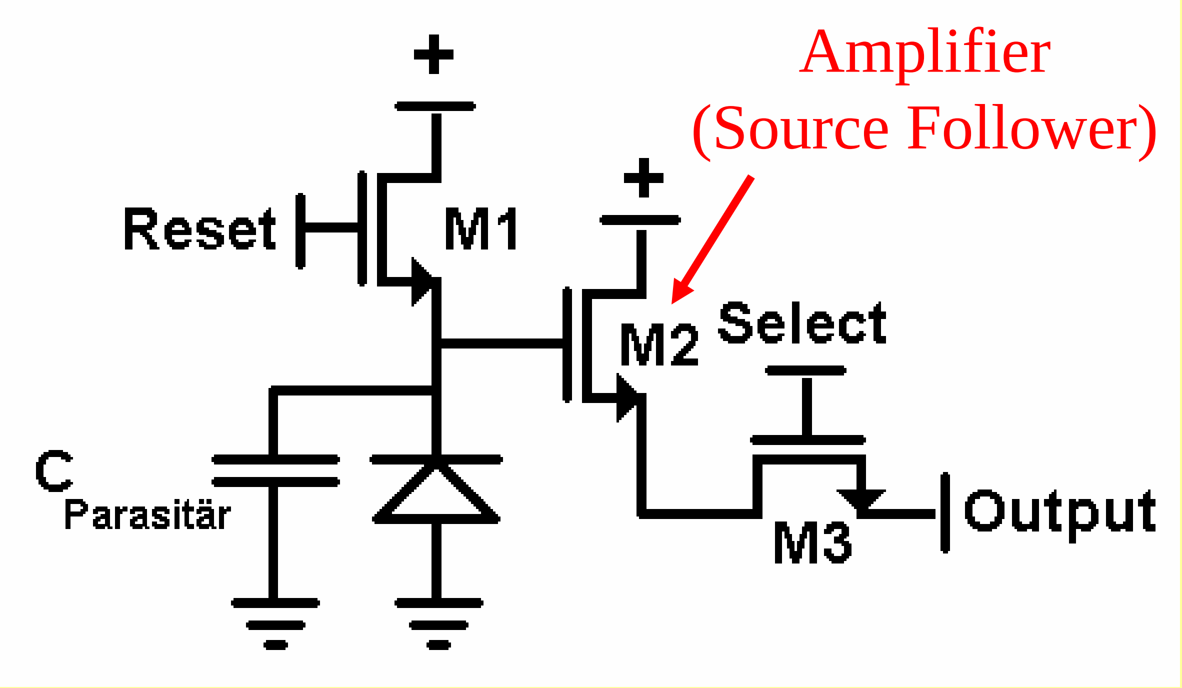
~80 e^-/h-pairs per µm in Si



The operation principle of MAPS

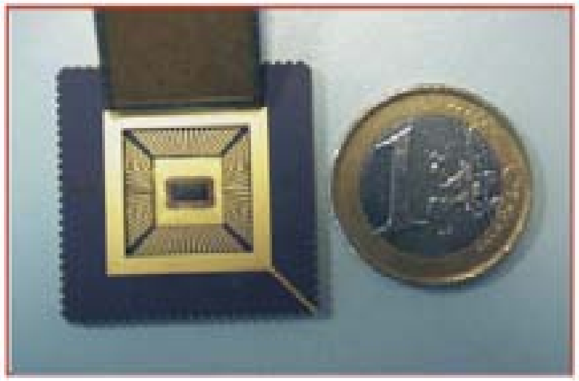


The operation principle of MAPS



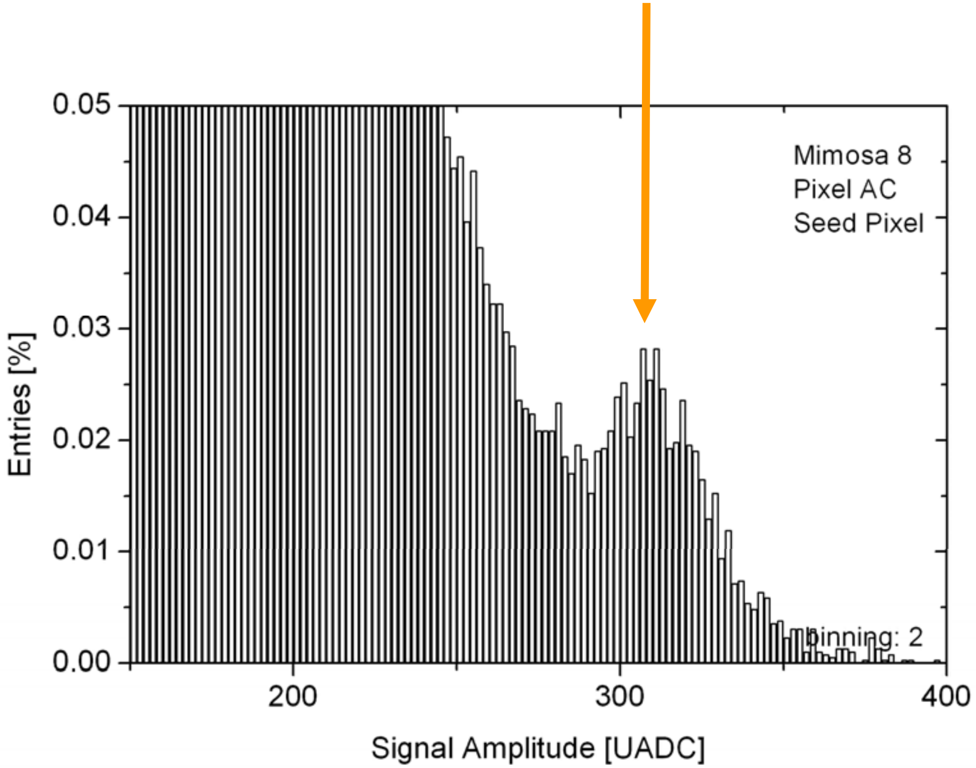
Layout of a classical Active Pixel (simplified)

MIMOSA8: Analogue tests with ^{55}Fe source



In collaboration with CEA/DAPNIA

Clear calibration peak
=> Low pixel to pixel dispersion



Preliminary results

- Signal: ~50-110 µV/e^-
- Noise: ~ 13-18 e^- (Pixel)
  ~ 3-10 e^- (Dispersion)
- CDS: OK
- Pedestal Correction: OK

See also: Y. Degerli et al, Proc. of the 2004 IEEE NSS conference, Roma

Outline

33 million pixels in a box

•Which performances are reached?

The vertex detector concept

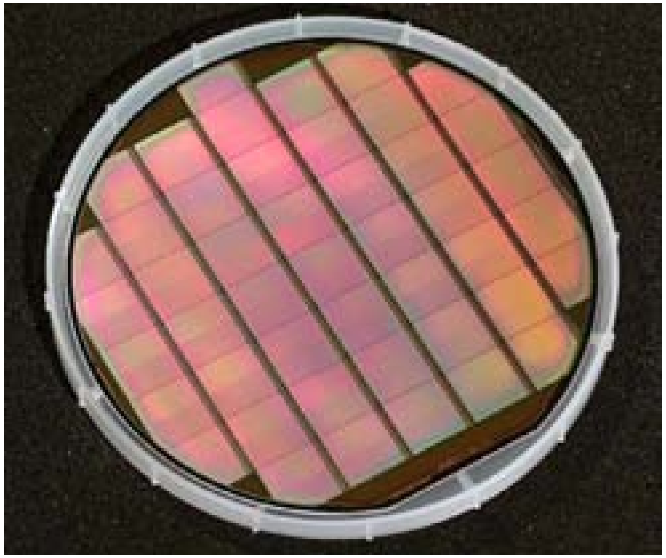
• A short reminder
• Requirements on readout speed
• Requirements on radiation hardness

Radiation hardness

• State of the art
• Recent results

Readout speed

• The problem
• A concept for fast MAPS
• Achievements and milestones



A MIMOSA5 Wafer
33 x 1MPixel
120µm thickness