LCFI Detector Studies

Snowmass 2005, VTX WG

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CCLRC Rutherford Appleton Laboratory

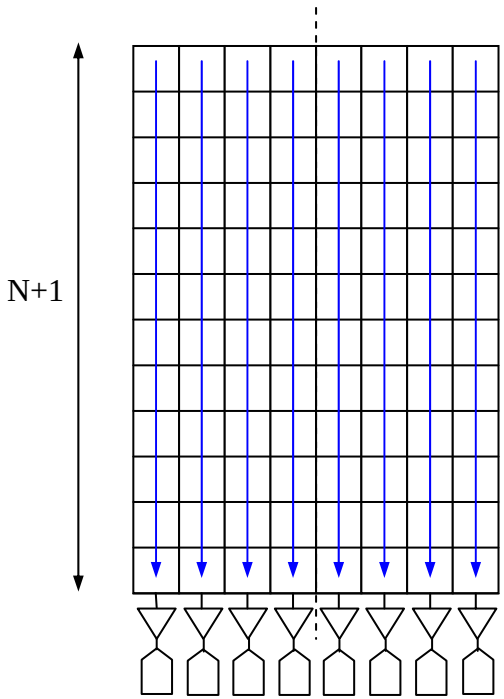
For the LCFI Collaboration

Sensor Research

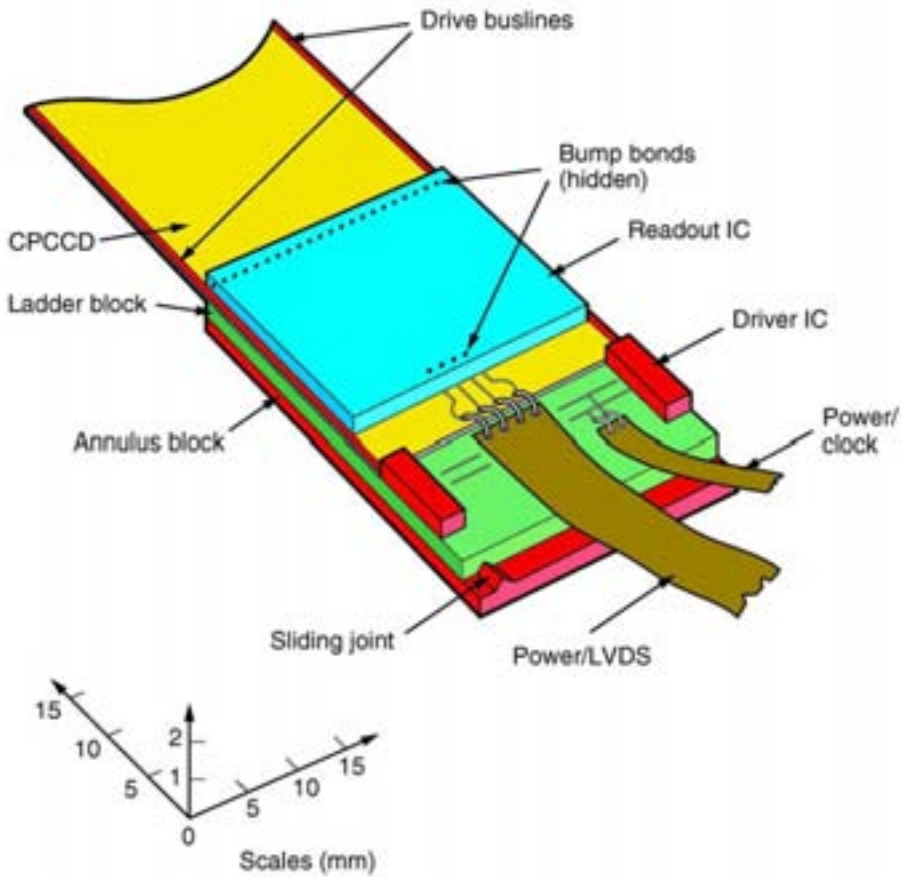
1. **Column Parallel CCDs**
   - Focus so far - building on past experience
   - Readout during bunch train
   - Clock drive major challenge
2. **Storage Sensors**
   - Increased robustness
   - Reduced driver requirements
   - ISIS and FAPS technologies

Column Parallel CCD

- **Separate amplifier and readout for each column**
- **50 MHz clock rate**



Column Parallel CCD
Readout time = $(N+1)/F_{out}$



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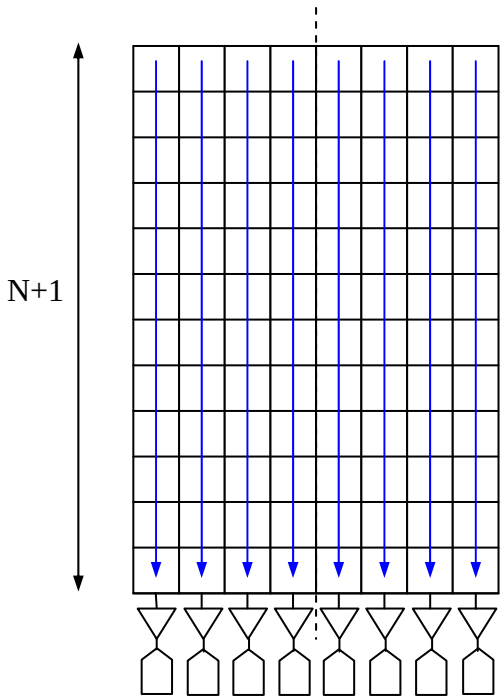

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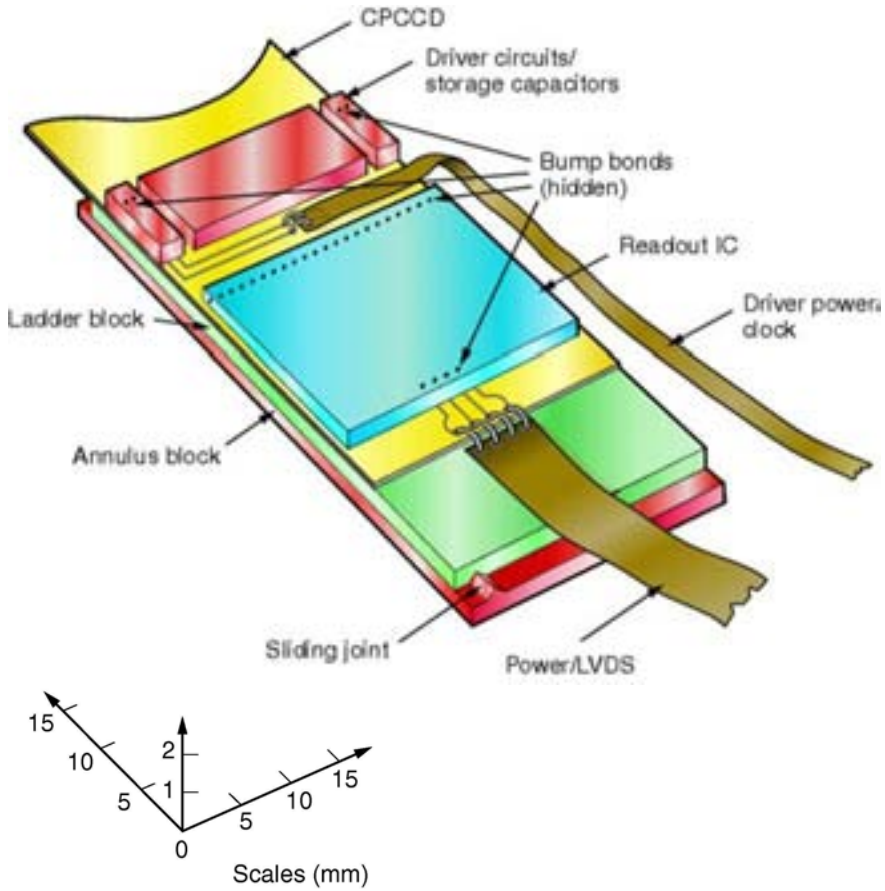
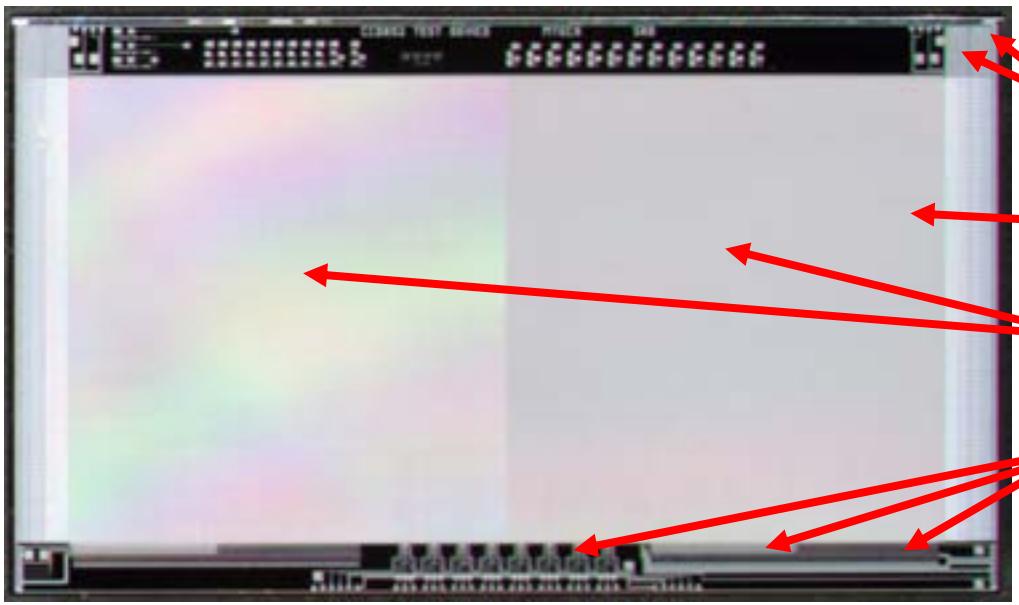


- **Clock drive is real challenge**

Prototype CP CCD



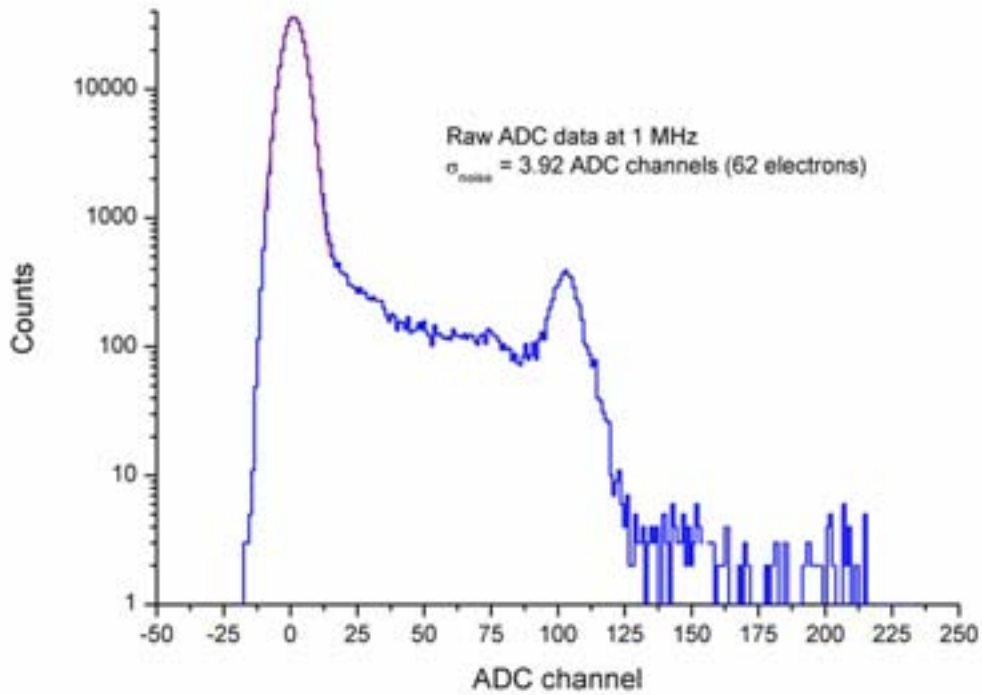
CPC1 produced by E2V

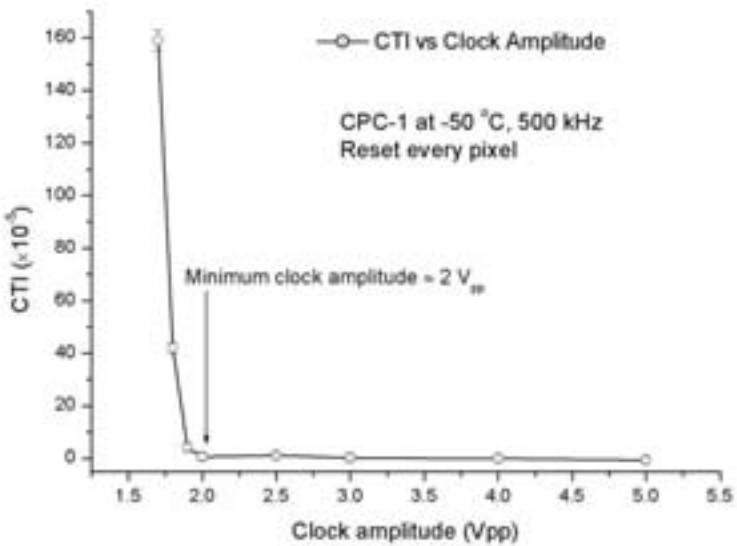
- Two phase operation
- Metal strapping for clock
- 2 different gate shapes
- 3 different types of output
- 2 different implant levels

➢ *Clock with highest frequency at lowest voltage*

CPC1 Results

- **Noise ~ 100 electrons (60 after filter)**
- **Minimum clock ~1.9 V**



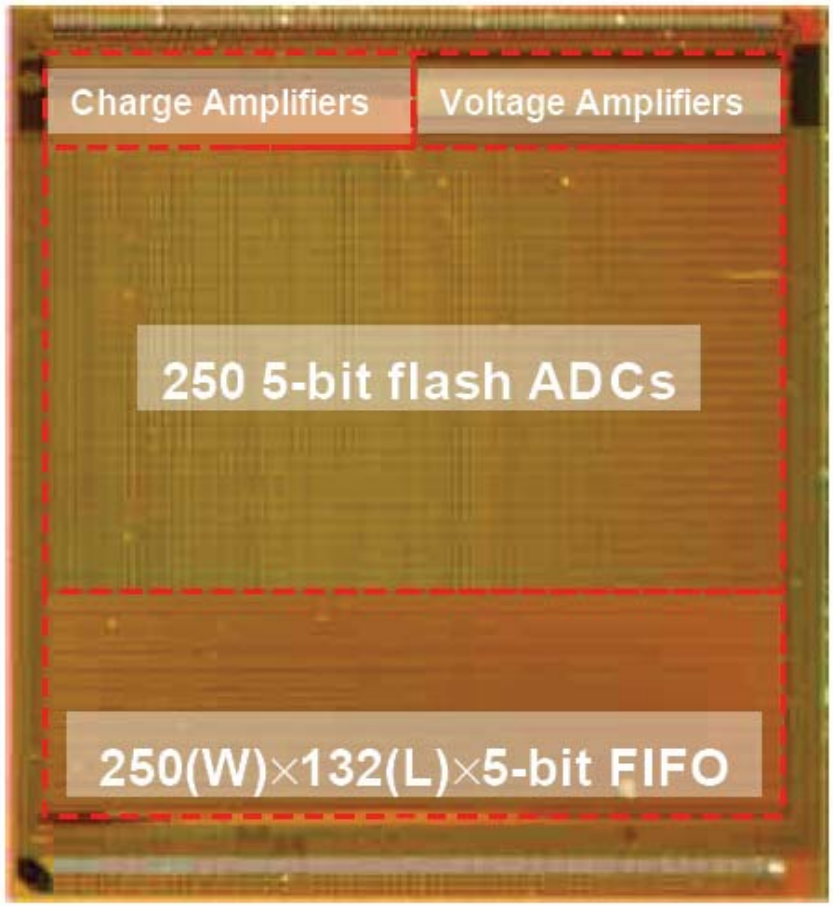


- **Maximum frequency > 25 MHz**
  - **inherent clock asymmetry**

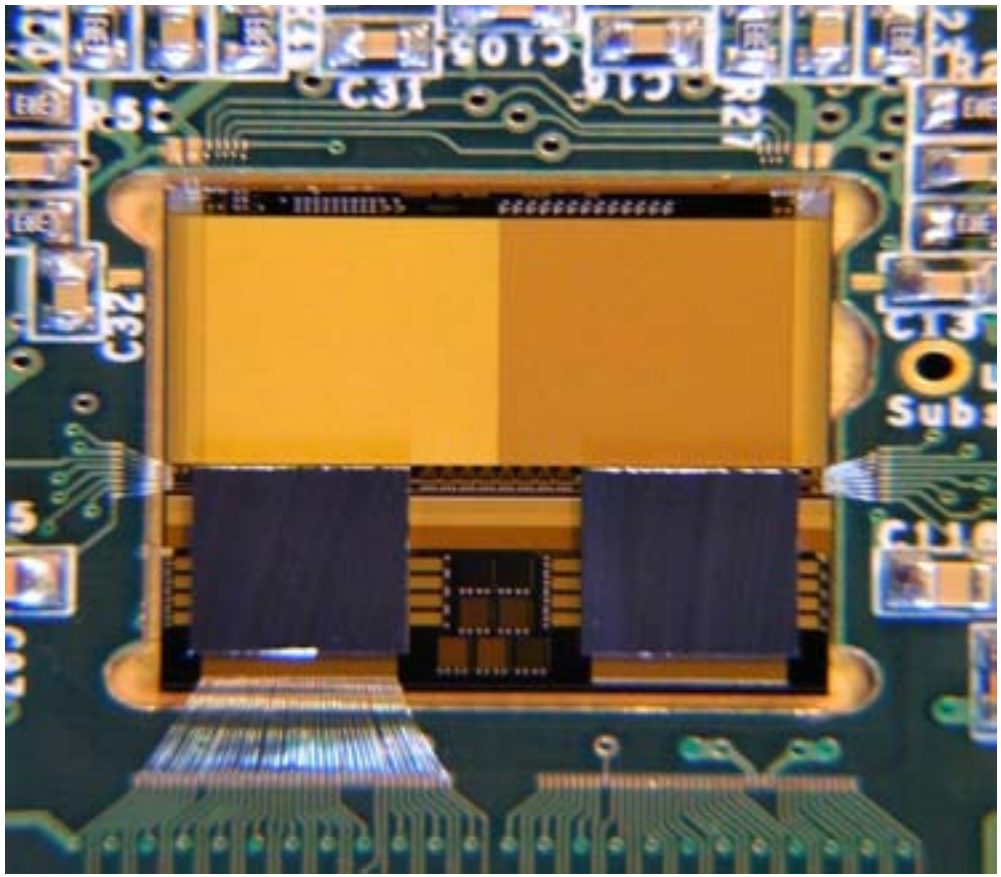
CP Readout ASIC

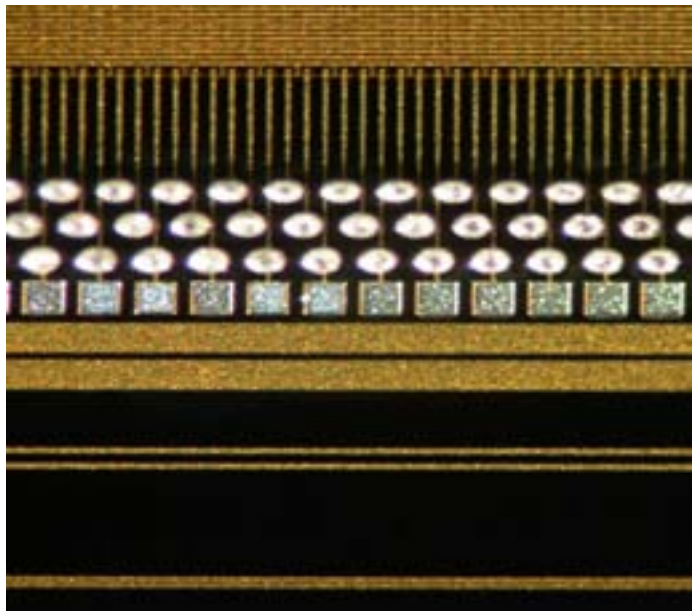
CPR1 designed by RAL ME Group

- IBM 0.25 µm process
- 250 parallel channels with 20 µm pitch
- Designed for 50 MHz
- Data multiplexed out through 2 pads



Bumped Assemblies



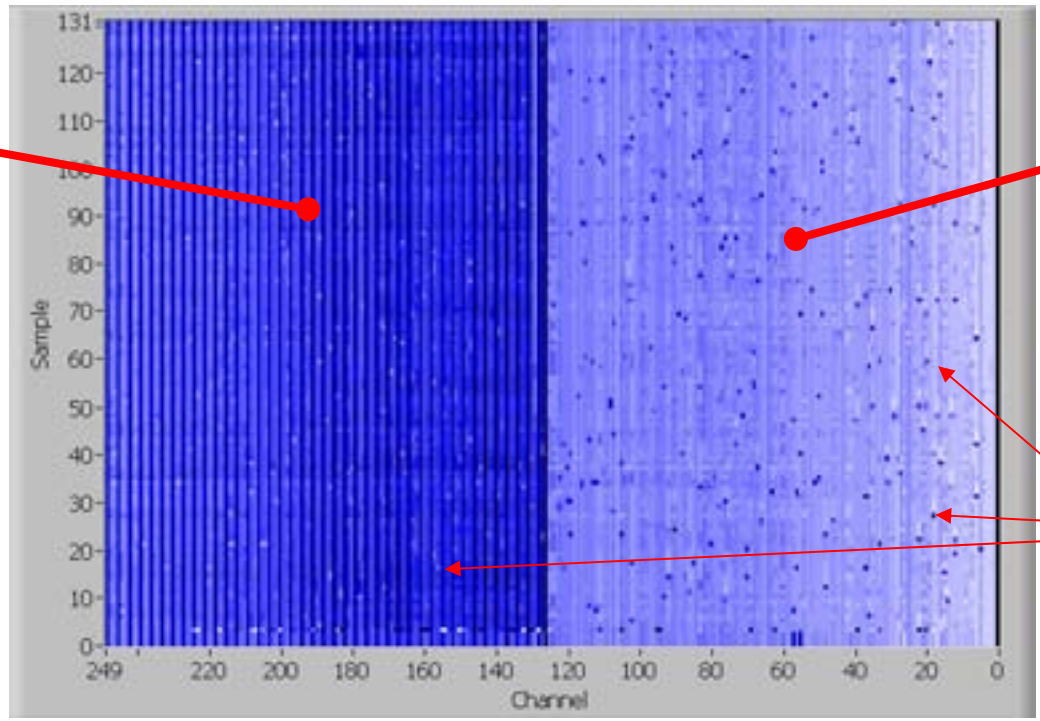


- **Bonding by VTT, Finland**
- **Bump yield very high**
- **Some whole chip failures**
  - ***Not fully understood***

Testing Results

Charge Amplifiers
(inverting)

Voltage Amplifiers
(non-inverting)



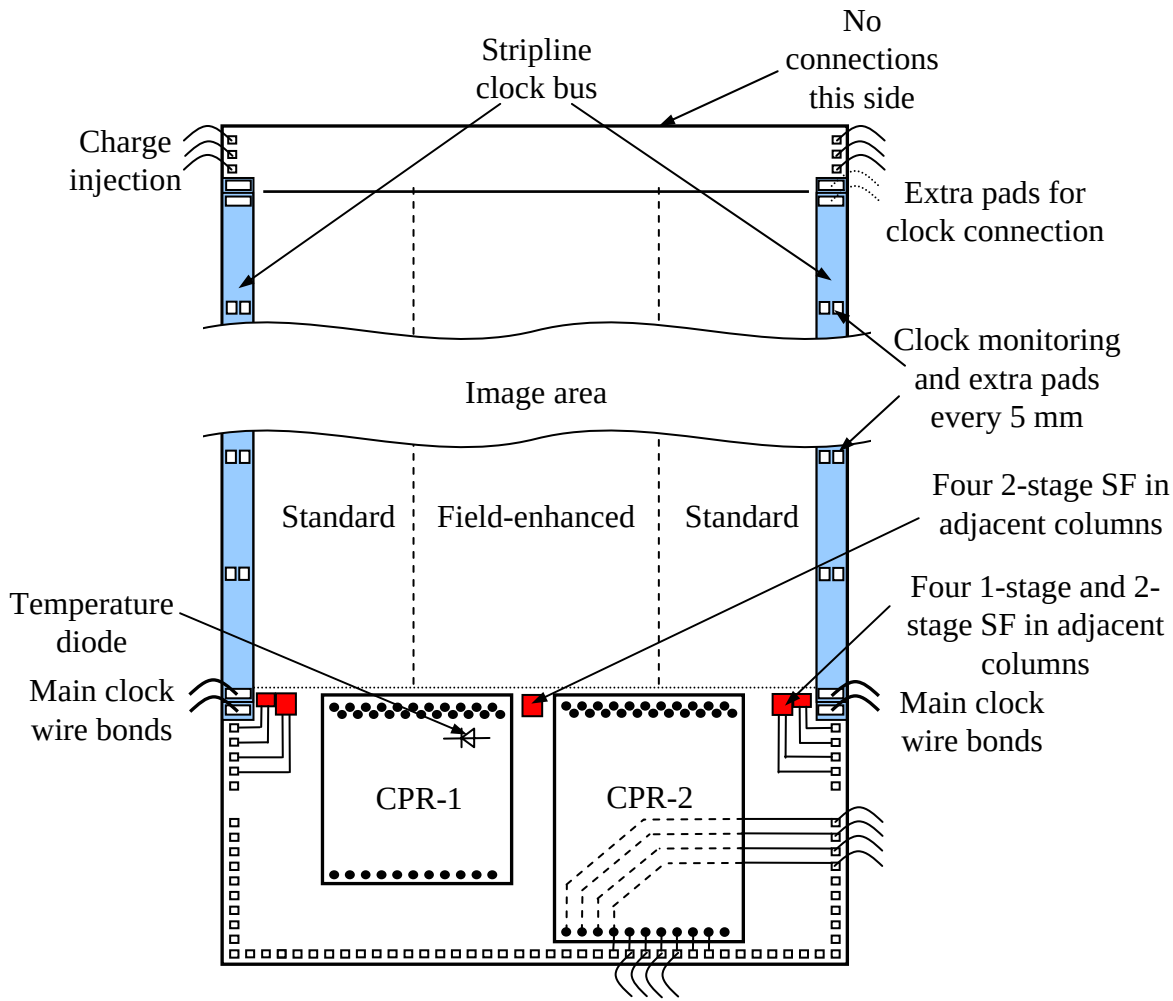
6 keV X-rays

- **Charge amplifiers work**
- **Negligible noise from CPR**
- ***Column parallel operation demonstrated***

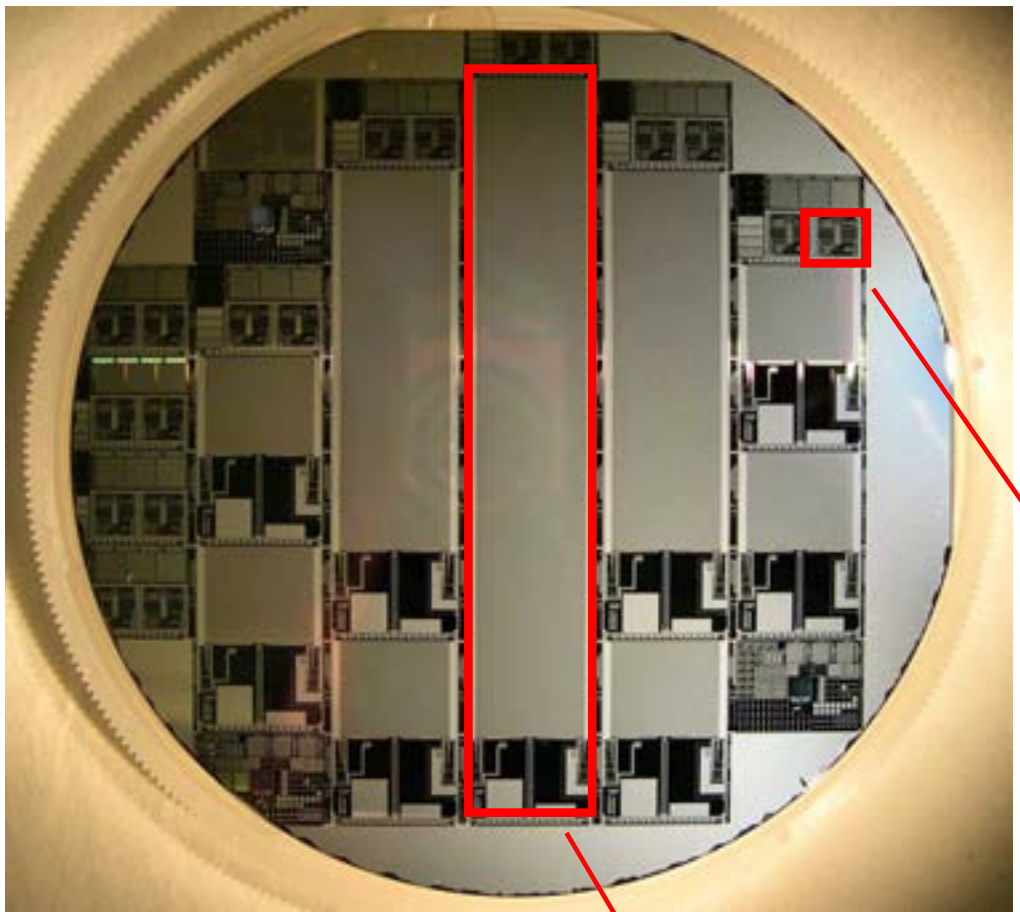
- **No signal in ~20% of voltage channels**
- **Readout chip very sensitive to timing and bias issues**
- **Gain decrease towards centre of chip**

Next Generation: CPC2

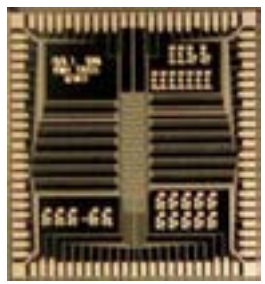
- **Double metal now available from E2V**
- **Symmetric clock design**
- **"Busline-free" option**
- **Compatible with old and new readout chips**



CPC2 Production



- **Dedicated batch at e2v**
- **3 sizes of CPCCD**
  - ***up to 92 mm active length***
- **First wafers in DC probing**
- **Wafers include 16×16 ISIS**



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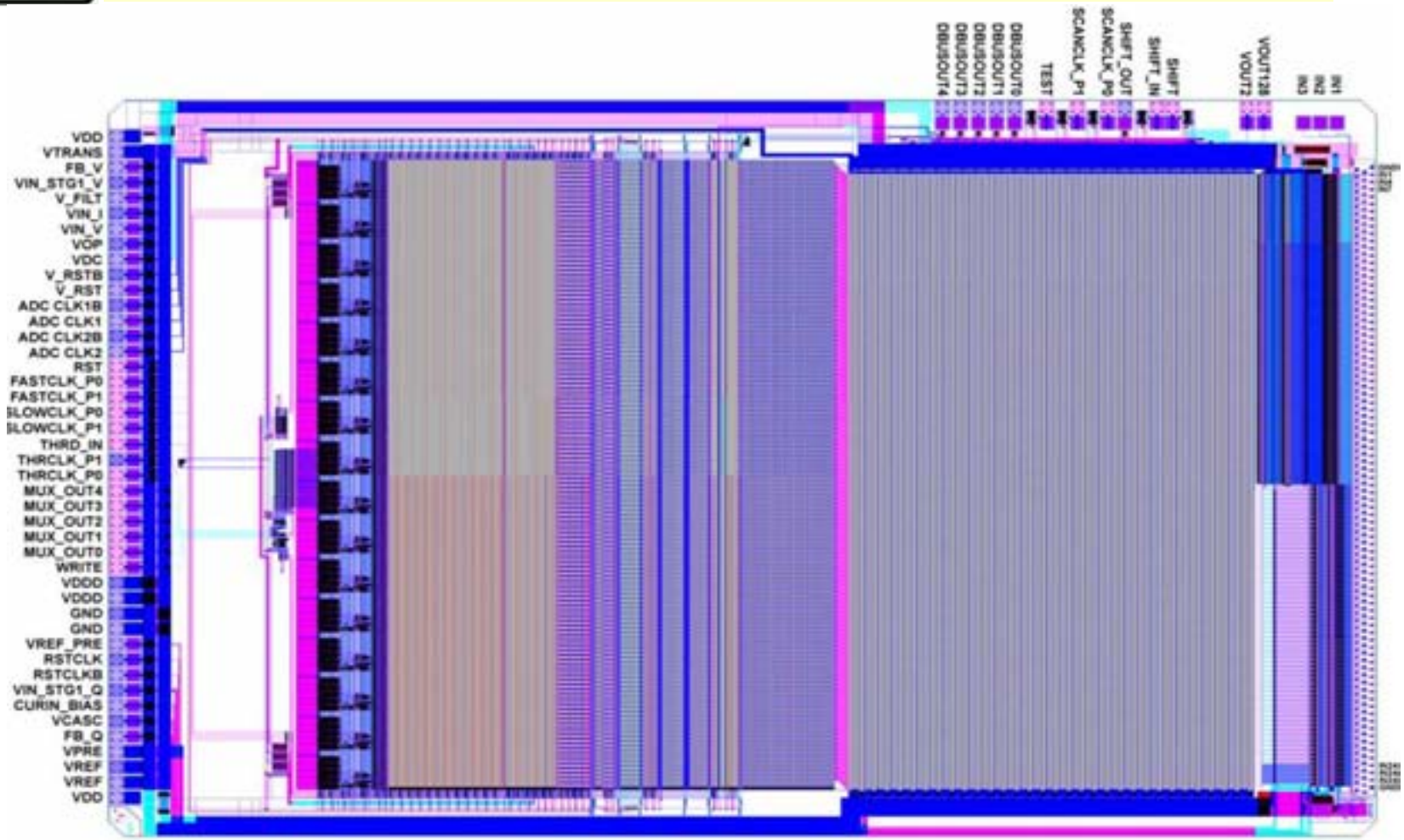
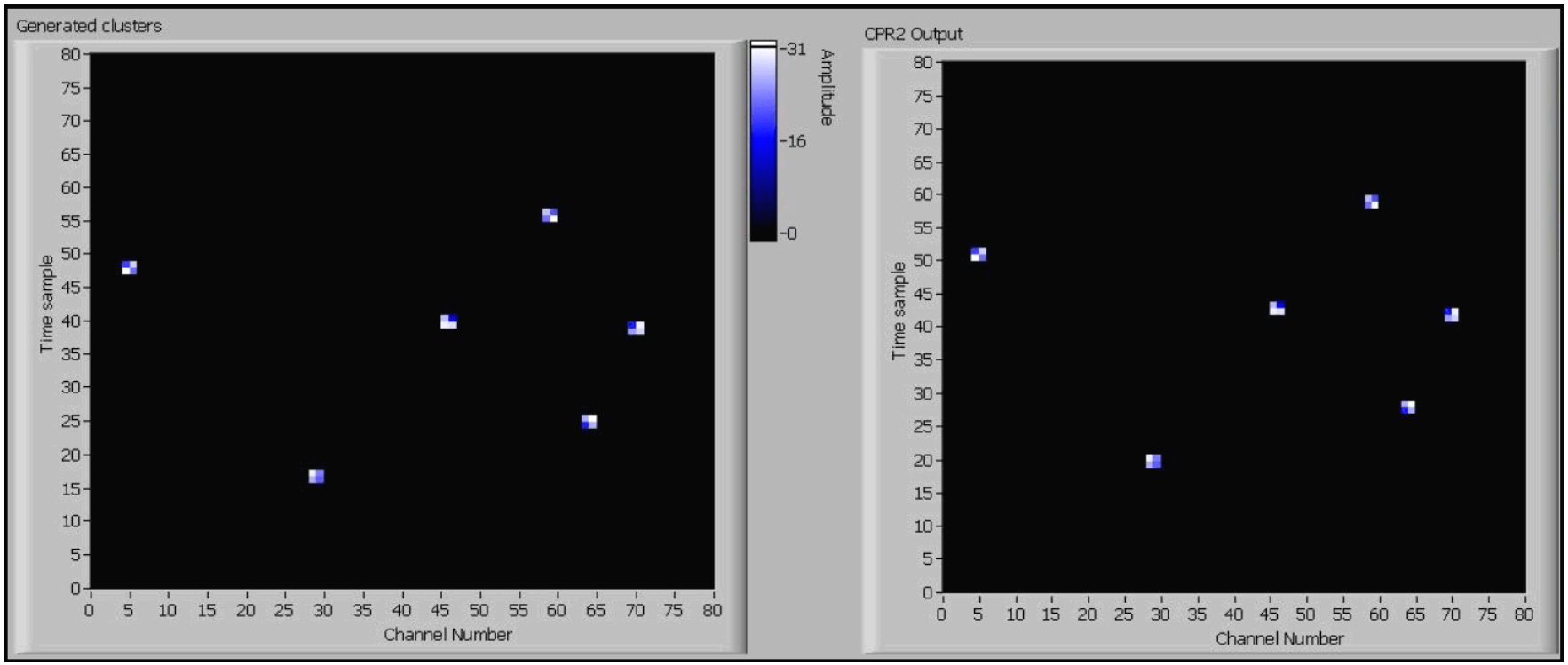


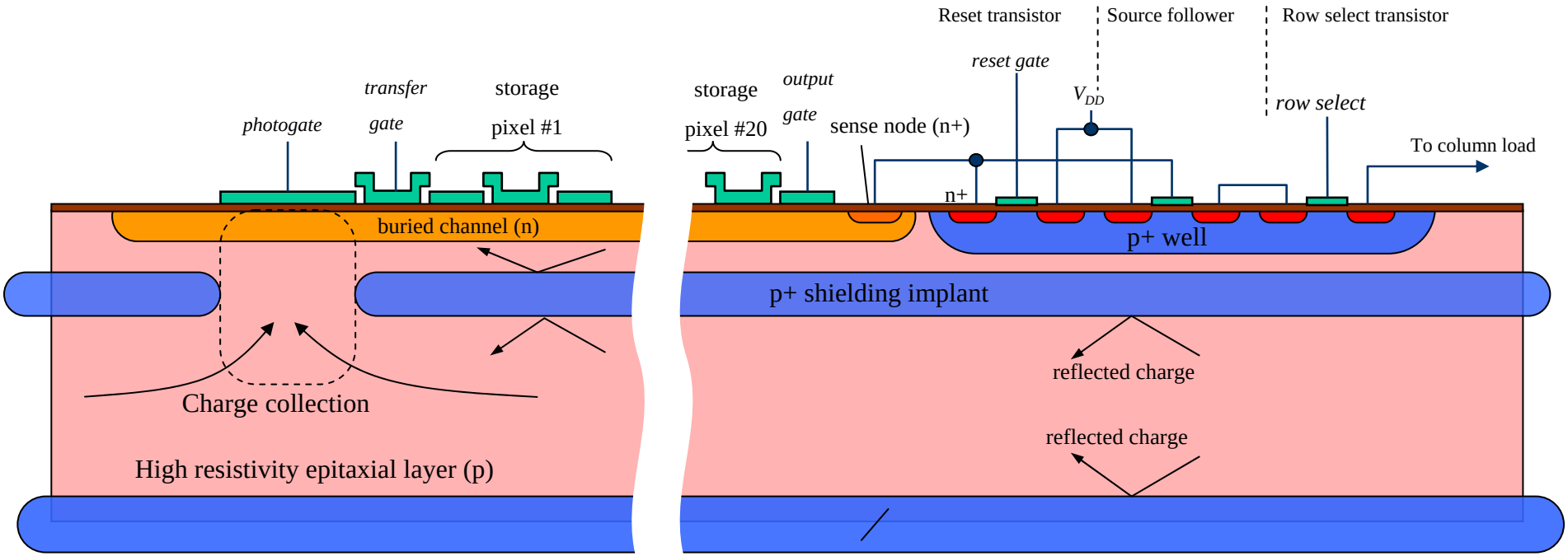
Output | **Sparsification & Multiplexing** | **Cluster Finding** | **Binary Conversion** | **5-bit ADC** | **Preamp Input**

CPR2 Testing



- **Cluster finding logic and sparse readout**
- **Improved amplifiers and ADCs**
- **Increased robustness**

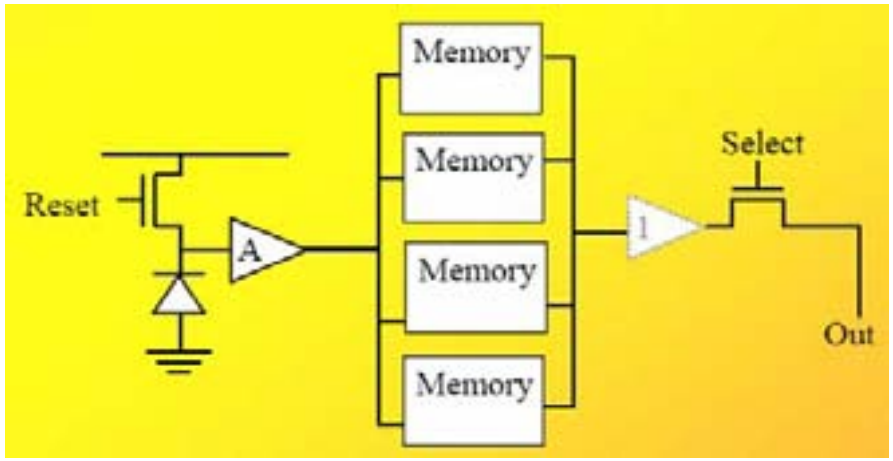
In-situ Storage Imaging Sensor

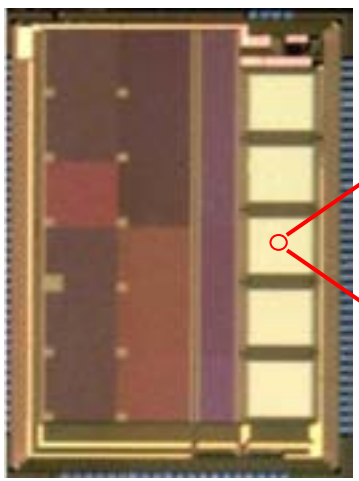


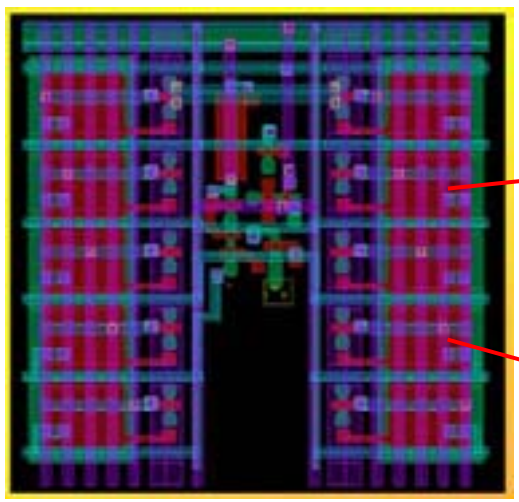
- **Orders of magnitude increased resistance to RF**
- **Much reduced clocking requirements *(readout ~1MHz)***
- **Combination of CCD and CMOS technology on small pitch**

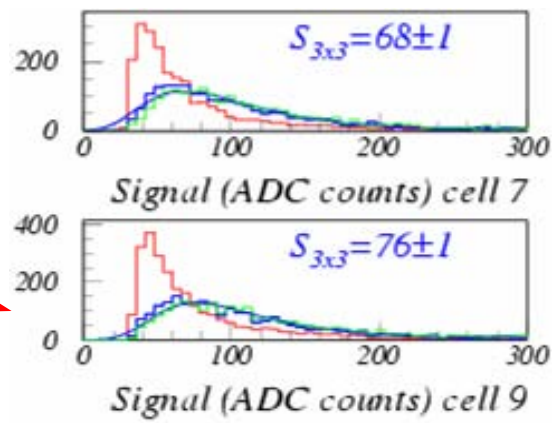
Flexible Active Pixel Sensors

- **FAPS architecture**
  - **First prototypes in 2004**
  - **Pixels 20x20 μm²**
  - **3 metal layers**
  - **10 storage cells per pixel**







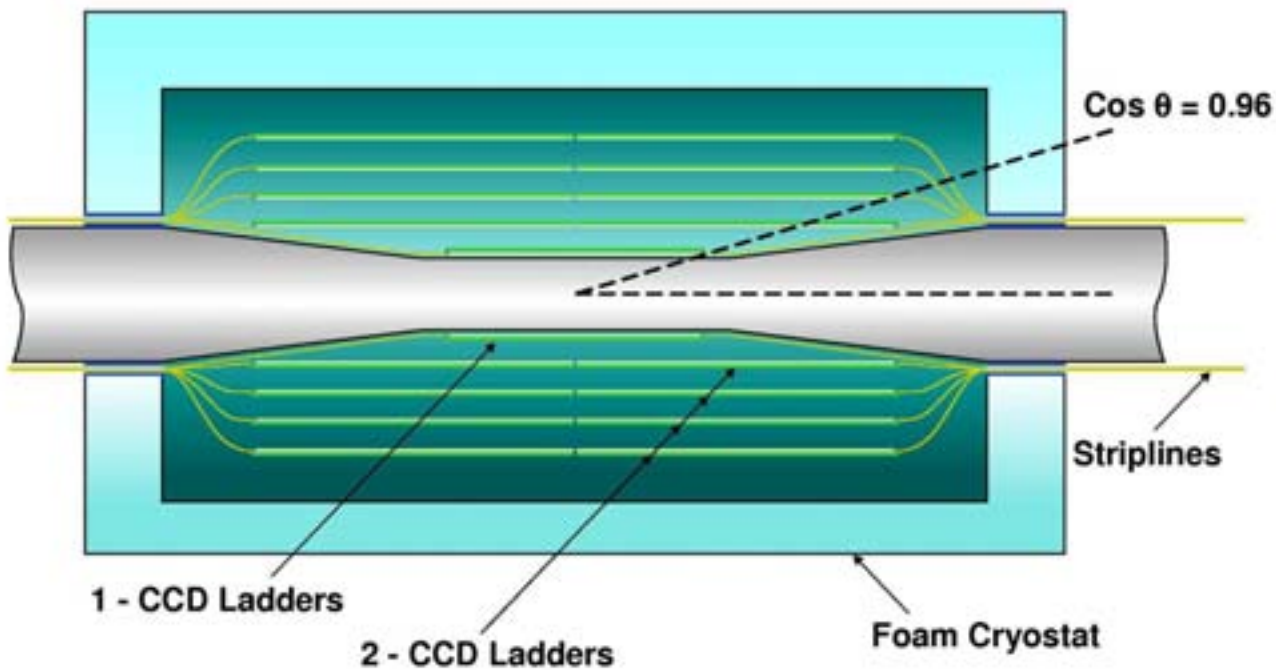


Plans

- **Test and evaluate 2nd generation CPCCD & readout**
- **Test first ISIS prototypes**
- **Design 3rd generation CPCCDs and drivers**
- **Develop ISIS and FAPS test structures**

Backup Slides

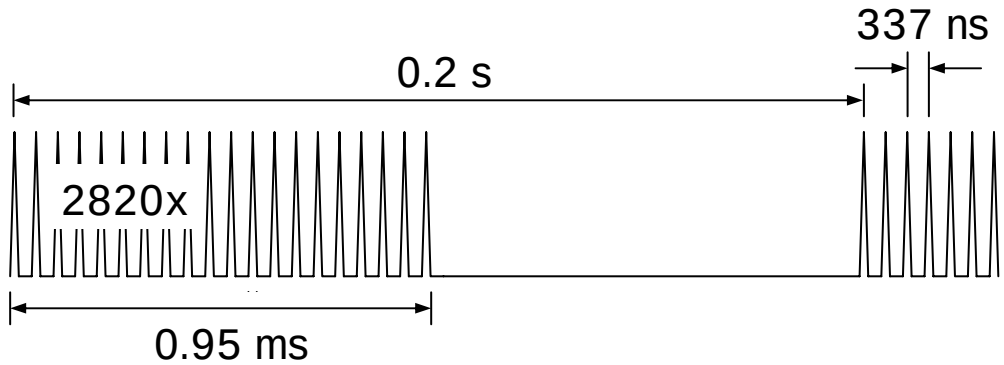
Baseline Vertex Detector



- 800 Mchannels of 20×20 μm pixels in 5 layers
- Optimisation:
  - Inner radius (1.5 cm?)
  - Readout time (50 μs?)
  - Ladder thickness (0.1% X_0?)

Sensors: The Challenge

Beam Time Structure:



What readout speed is needed?

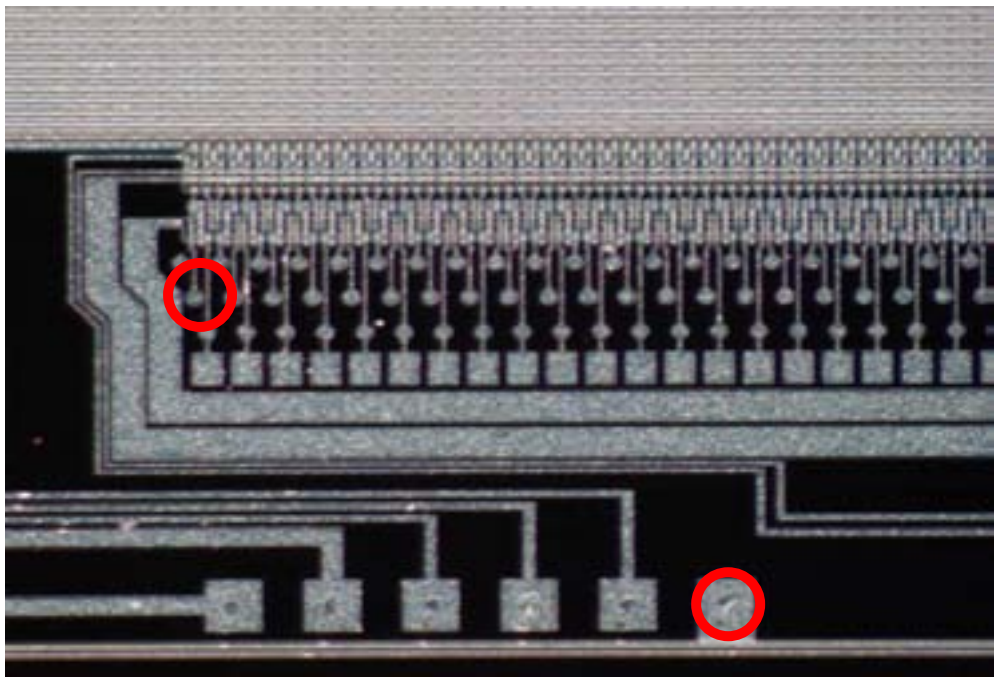
- **Inner layer 1.6 MPixel sensors**
- **Once per bunch = 300ns per frame : *too fast***
- **Once per train ~200 hits/mm^2 : *too slow***
- **10 hits/mm^2 => 50μs per frame: just right**

(Fastest commercial imaging ~ 1 ms/MPixel)

Power dissipation – gas volume cooling

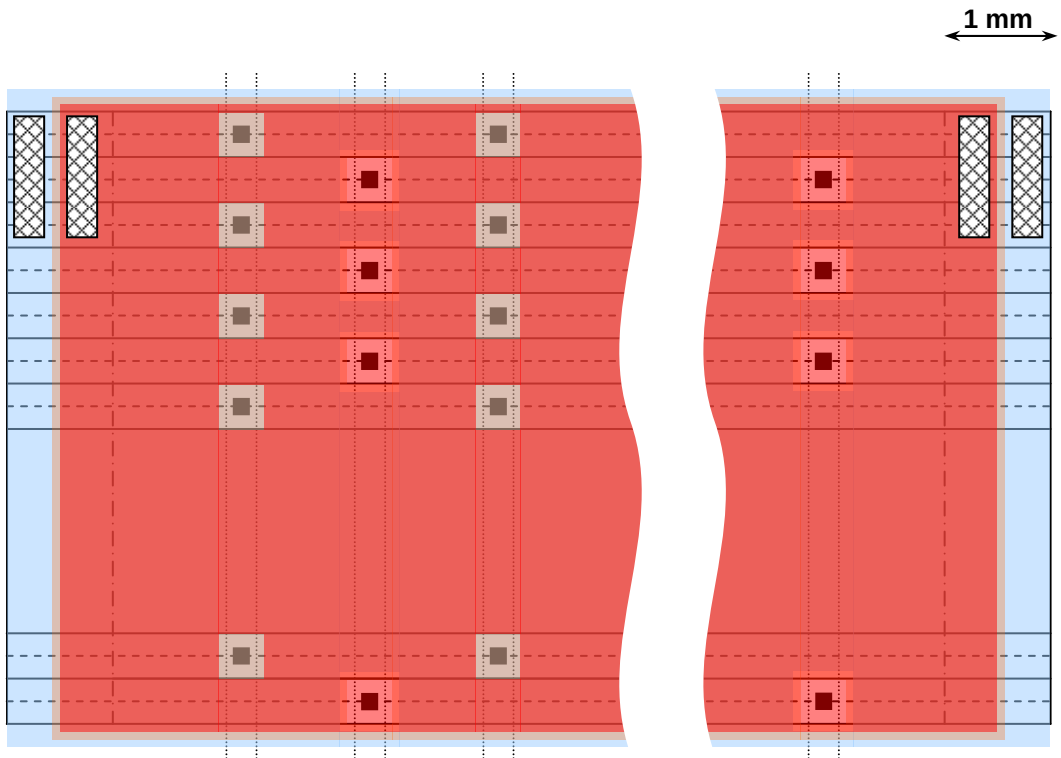
Bumping Failures

- **Short between CCD substrate and chip ground**
- **Possible mechanical damage**



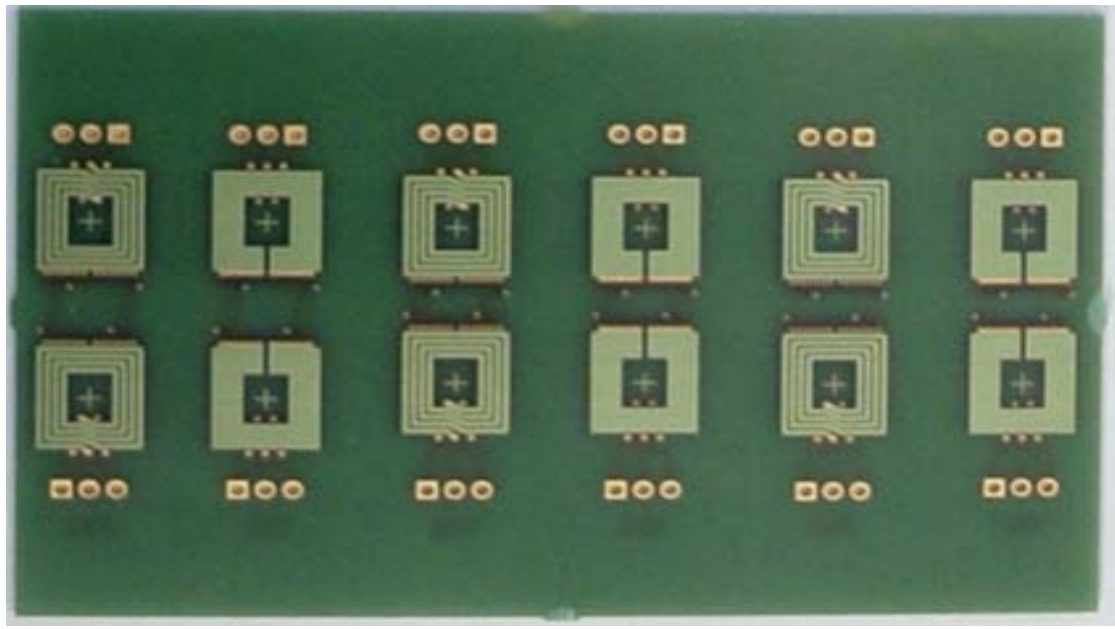
Busline Free CCDs

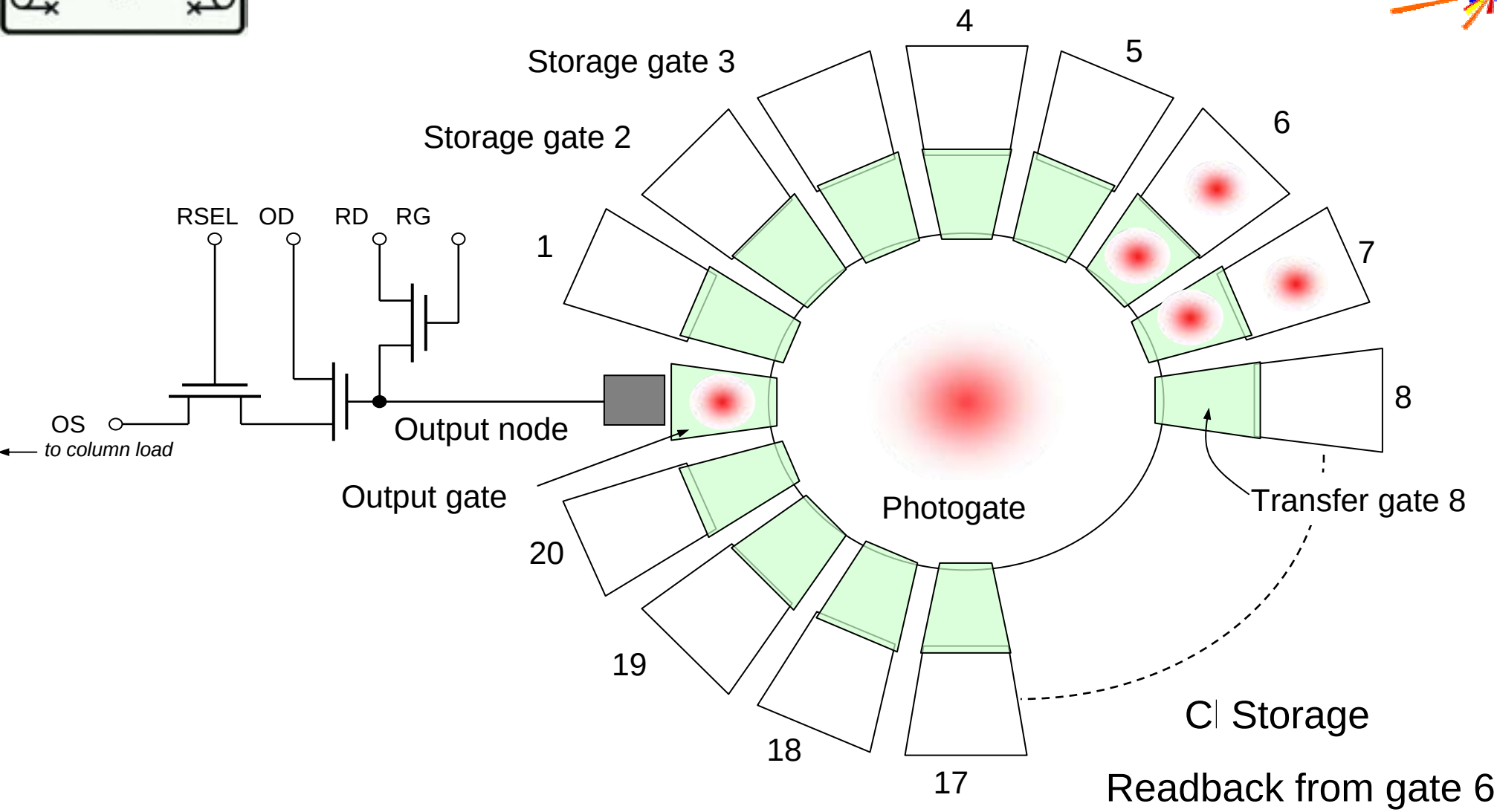
- **Clock signals transmitted via distributed drive planes**
  - **Faster propagation**
  - **More uniform**



CCD Drivers

- **Clock drivers are a big challenge**
  - **Working on air core PCB transformers**
  - **Long-term solution more likely to be IC with local storage**





Idea by D. Burt and R. Bell (e2V)

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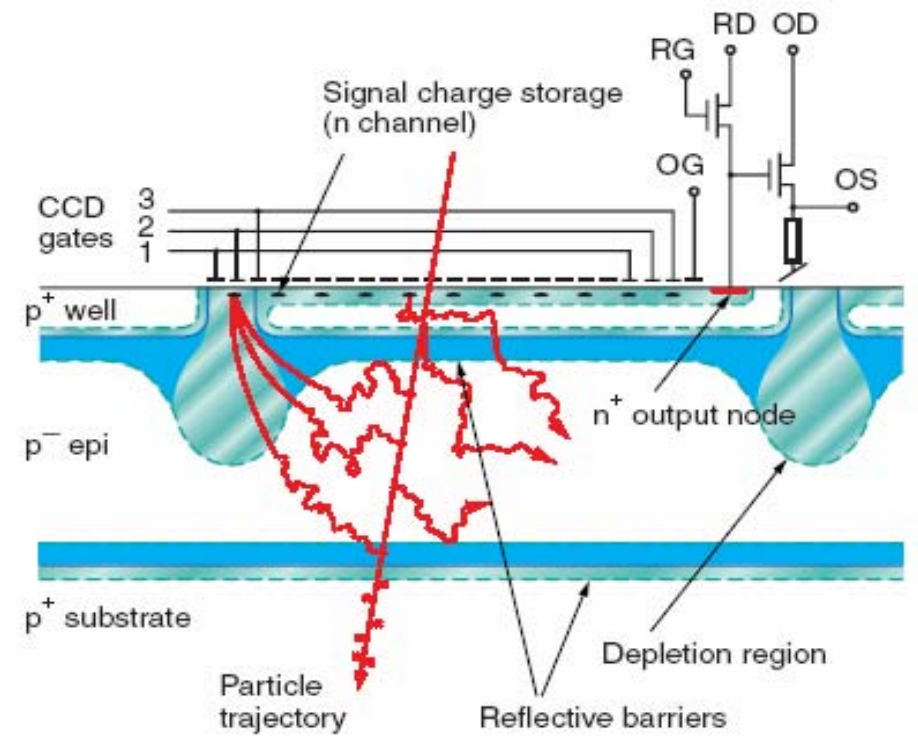

1. **Charge collection similar to CCD or CMOS**
2. **Charge transferred into local CCD array every 50µs**
3. **Local CCD array clocked at 20 kHz**
4. **Source follower for every pixel**
5. **Read out one row at a time**
   - ***Still column parallel***