Detector thinning technology

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[a]MPI fuer Physik, Semiconductor lab, Munich and

- Introduction/Motivation
- Module Concept
- ThinningTechnology
  - Direct Wafer Bonding
  - Anisotropic deep wet etching
- Diodes on thin Silicon
- Summary and Conclusion

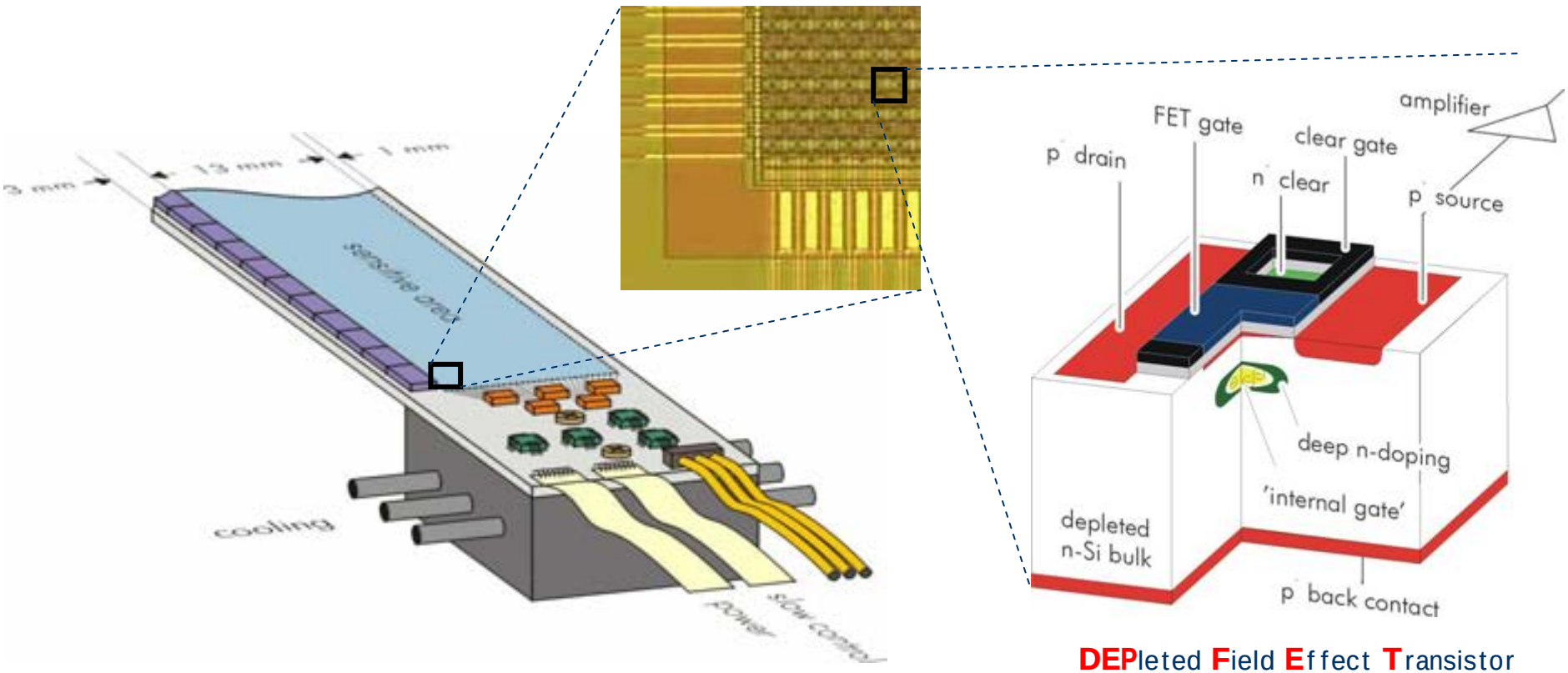
Introduction

- Thinning technology developed for DEPFET option of vertex detector by L.Andricek
- Allows construction of mechanical rigid all silicon modules with thin (50um) active area and thick (300um) frame for mechanical stability
- Relies on wafer bonding technology (MPI für Mikrostrukturphysik, Halle, Germany)
- Processing performed in MPI semiconductor laboratory
- Method has been demonstrated to work very well with thin diodes

Module Concept / Pixel Cell

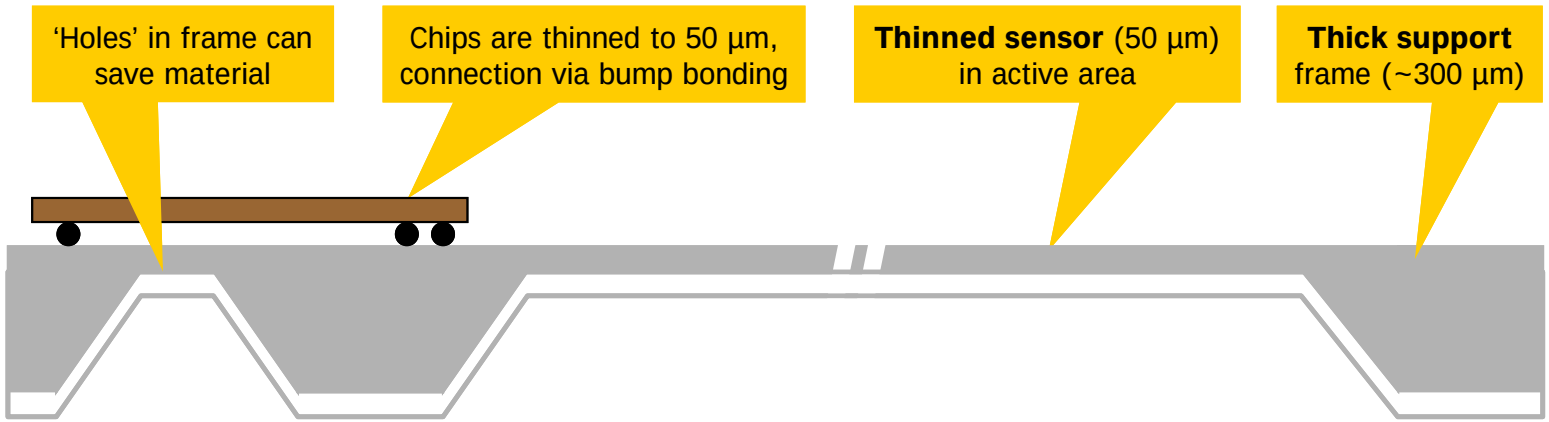
sensitive area 1st layer module: 100x13 mm², 2nd-5th layer : 125x22 mm² ➔ ∑120 modules

sensitive area thinned to 50 μm, supported by a 300 μm thick frame of silicon



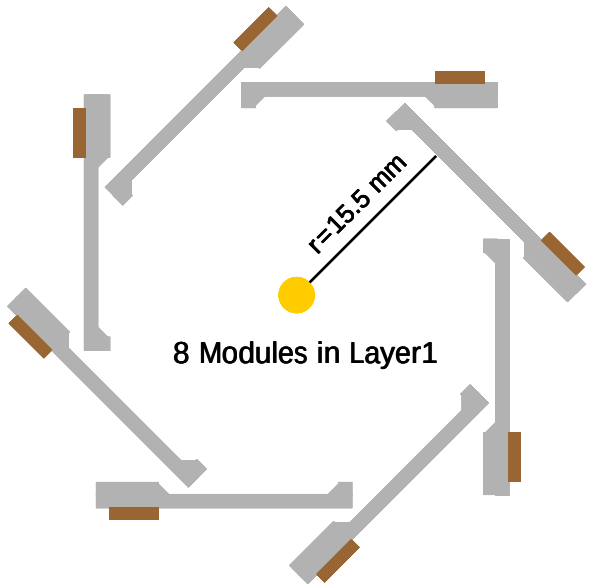
DEPleted **F**ield **E**ffect **T**ransistor

Module cross section



Estimation of material budget:

- pixel area: 13x100 mm^2, 50µm: 0.05% X_0
- steering chips: 2x100 mm^2, 50µm: 0.01% X_0
- frame w. holes: 4x100 mm^2, 50% of 300µm: 0.05% X_0
- total: **0.11% X_0**



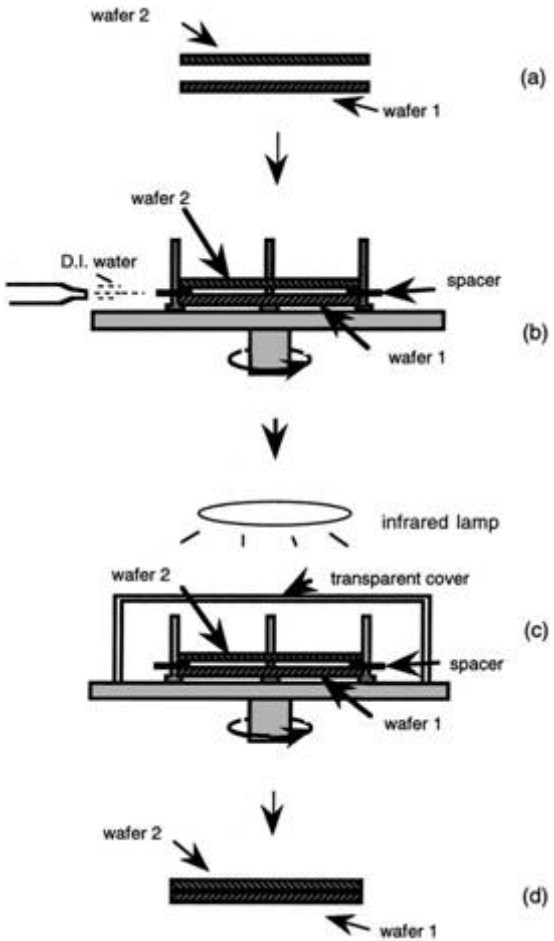
Making thin Sensors

1. implant backside on sensor wafer
2. bond wafers with SiO_2 in between
3. thin sensor side to desired thick.
4. process DEPFETs on top side
5. etch backside up to oxide/implant

Electron micrograph of cut through bonded and thinned wafer

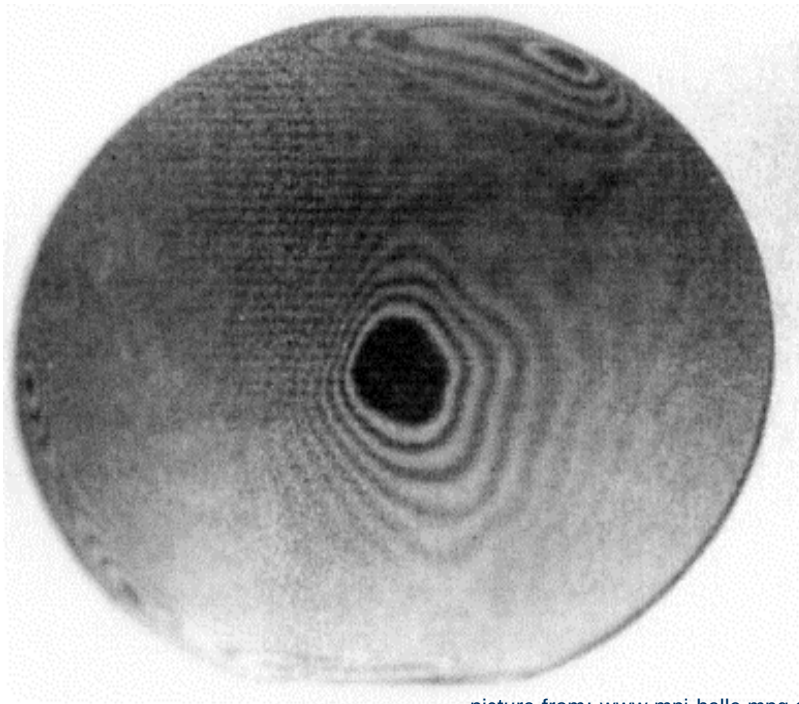
first ‘dummy’ samples:
50µm silicon with 350µm frame

Processing thin detectors
- Direct Wafer Bonding -



Q.-Y. Tong and U. Gösele " Semiconductor Wafer Bonding "
John Wiley & Sons, Inc.

Wafer stacks prepared by
MPI für Microstrukturphysik, Halle



picture from: www.mpi-halle.mpg.de

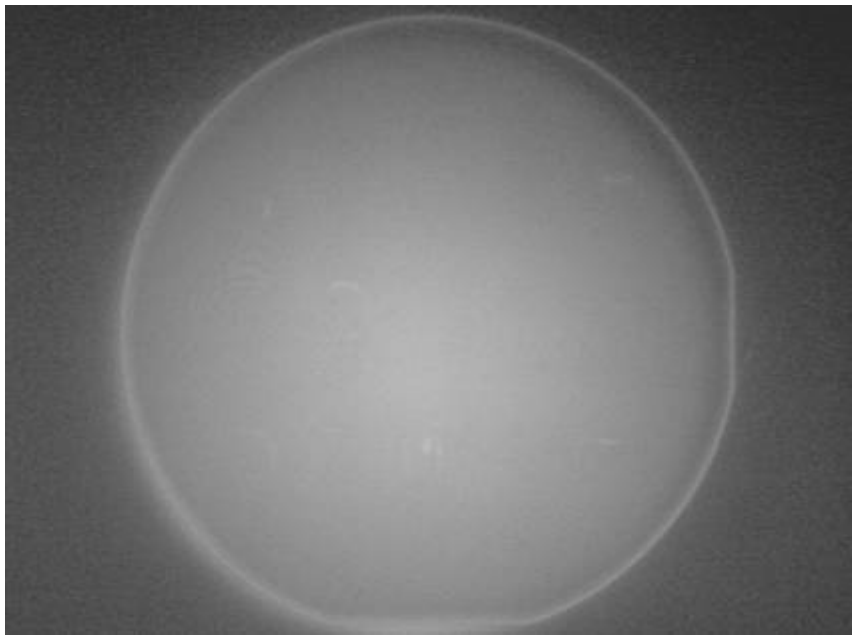
→ annealing at T>1000 ºC → Si-O-Si bonds

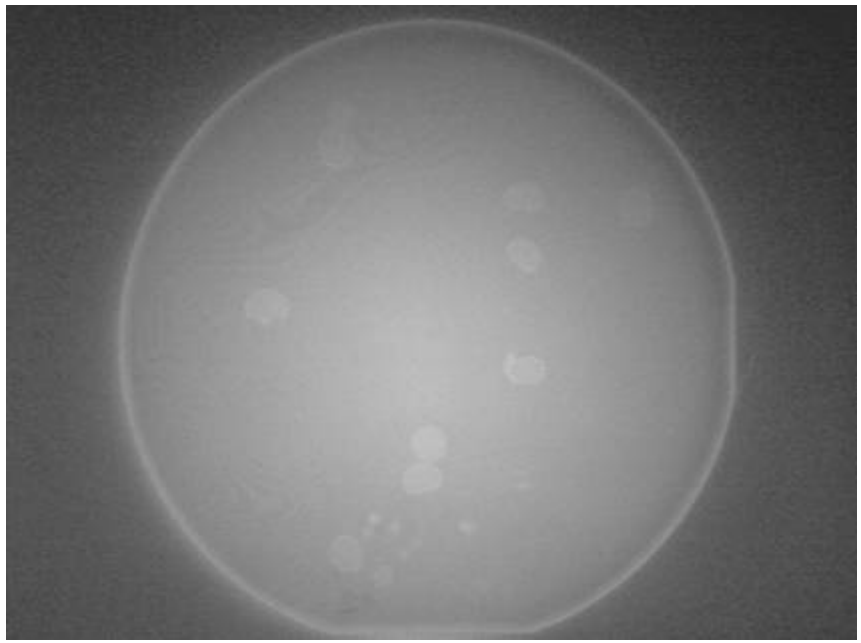
Direct Wafer bonding after Implantation

Bonded wafers (structured implant through BOX):

Direct Wafer Bonding possible, but some voids after annealing!

➔ improve surface condition before bonding





infrared transmission pictures from MPI Halle (M. Reiche)

Anisotropic Wet Etching
- TMAH -

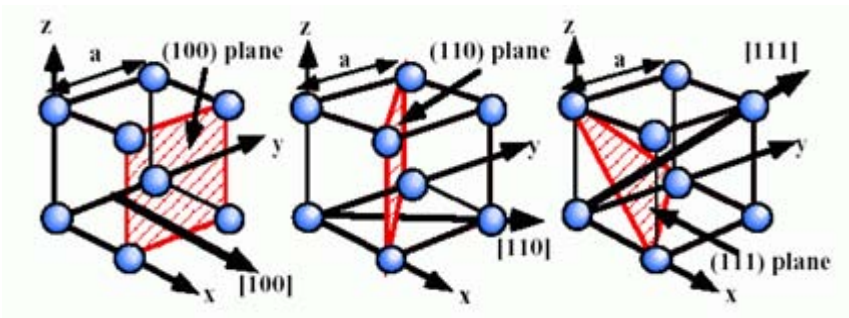
Tetramethyl Ammonium Hydroxide

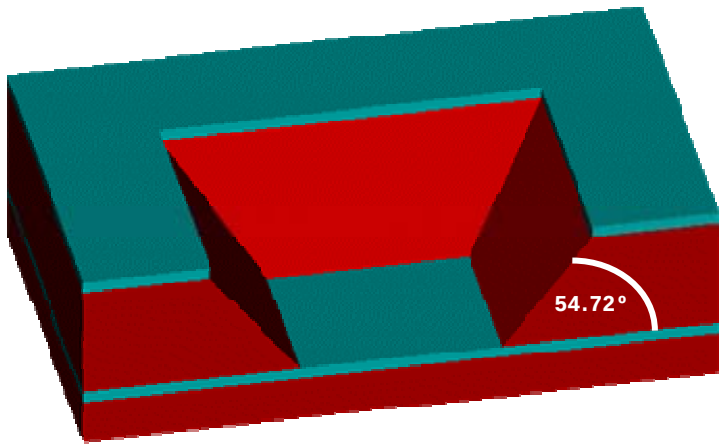
- good selectivity to oxide
- almost perfect selectivity to Al
- no alkali ions

→ 5 wt.% TMAH
1.6 wt.% dissolved silicon
0.4 wt.% $(NH_4)_2S_2O_8$

G.Yan et al., Sensors and Actuators A 89, 2001

- poorer selectivity to (111) (≈30:1)
- rough surface after etching (hillocks)





Mechanical Dummies

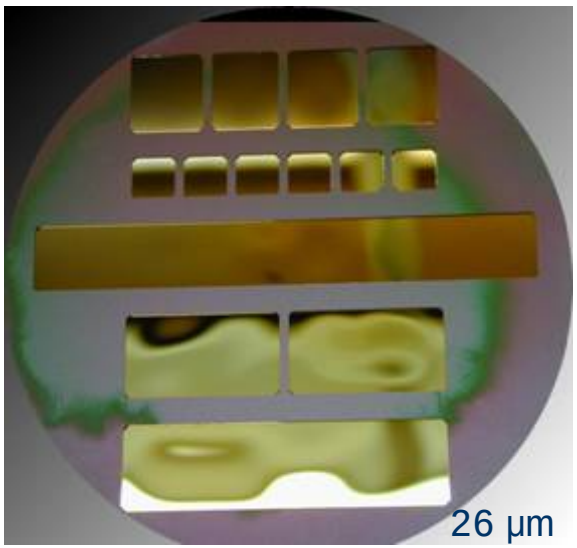
- how thin can we get?? -

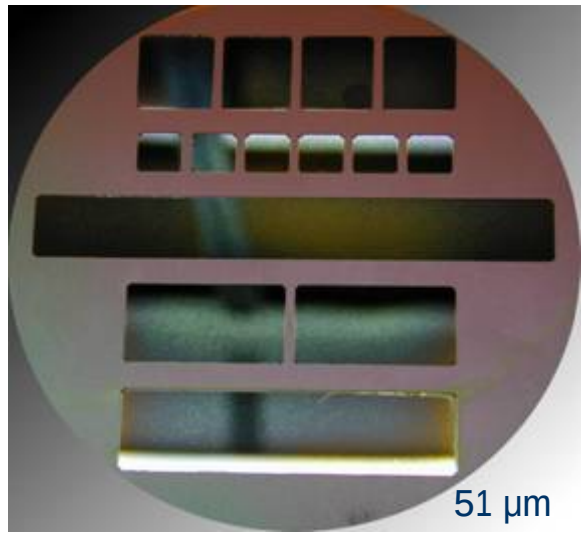
window dimensions:

(50x13)/4 mm^2
6.5x6.5 mm^2
80x10.4 mm^2 (80% of a tesla sensor)
(50x13)/2 mm^2
50x13 mm^2

10 "SOI" wafers with various top layer thicknesses

⇒
24 - 29 micron (3 Wafers)
36 - 38 micron (3 Wafers)
43 - 51 micron (4 Wafers)





Mechanical Dummies

- distortions -

window dimensions:

(50x13)/4 mm^2
6.5x6.5 mm^2
80x10.4 mm^2 (80% of tesla sensor)
(50x13)/2 mm^2
50x13 mm^2

10 "SOI" wafers with top layer different thickness

⇒
24 - 29 micron (3 Wafers)
36 - 38 micron (3 Wafers)
43 - 51 micron (4 Wafers)

➔ principle works!!

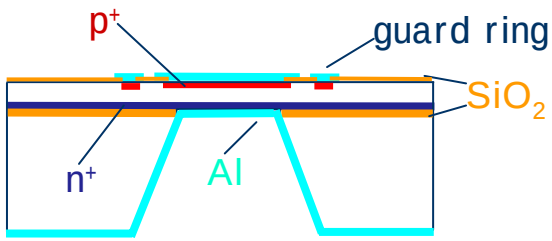
➔ 50 μm seems to be a reasonable thickness

➔ diced samples robust enough for safe handling

PiN Diodes on thin Silicon

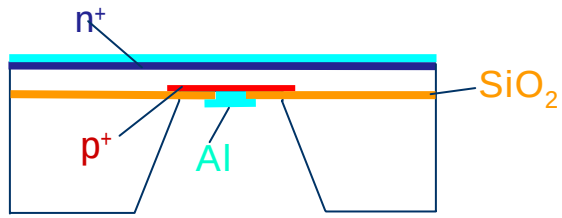
2 types of thinned diodes

Type I: Simplified standard technology



structured p+ on top
unstructured n+ in bond region
3 Wafers

Type II: Implants like DEPFET config.

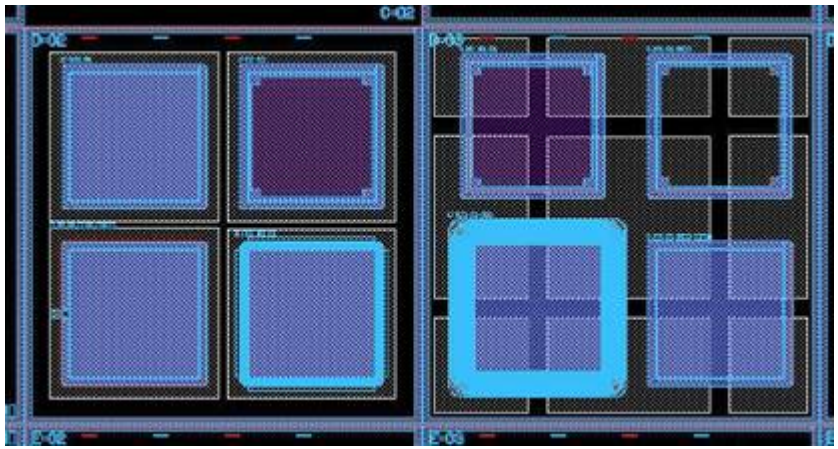


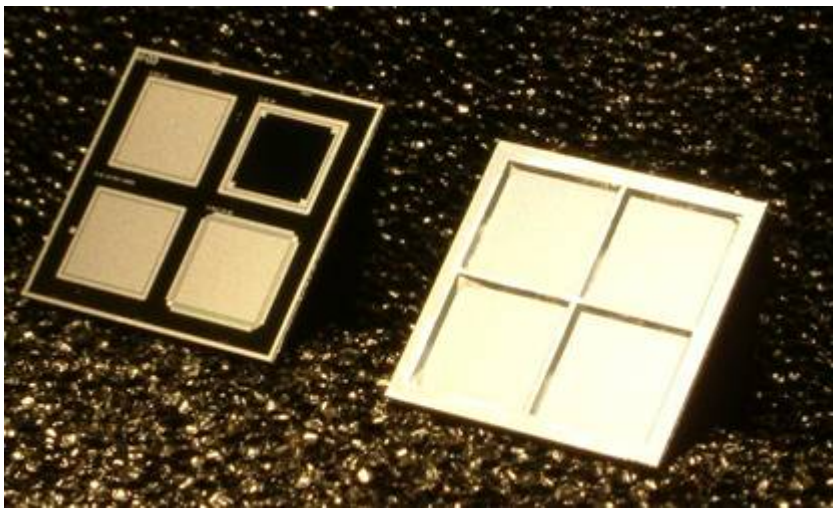
unstructured n+ on top
structured p+ in bond region
3 Wafers

** + 4 Wafers with standard Diodes as a reference **

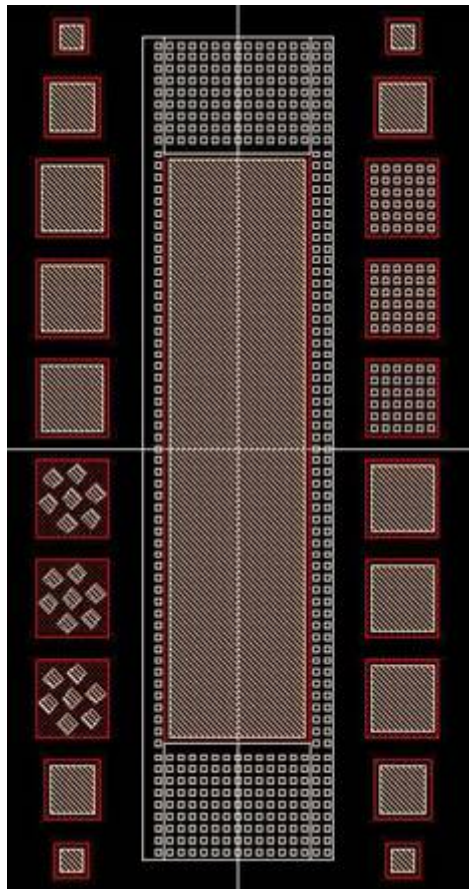
PiN Diodes on thin Silicon

Type I: pn-junction on top wafer surface



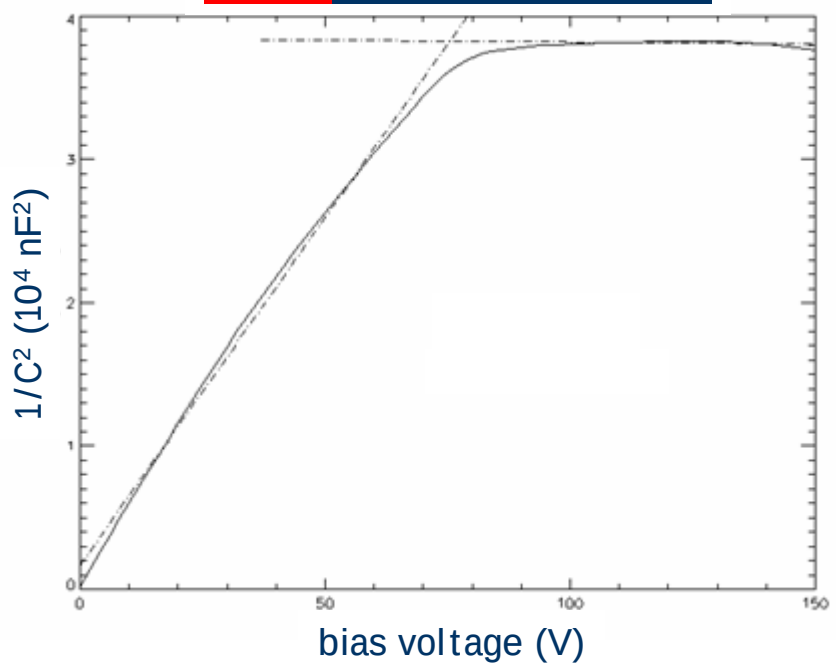


Type II: pn-junction in bond region

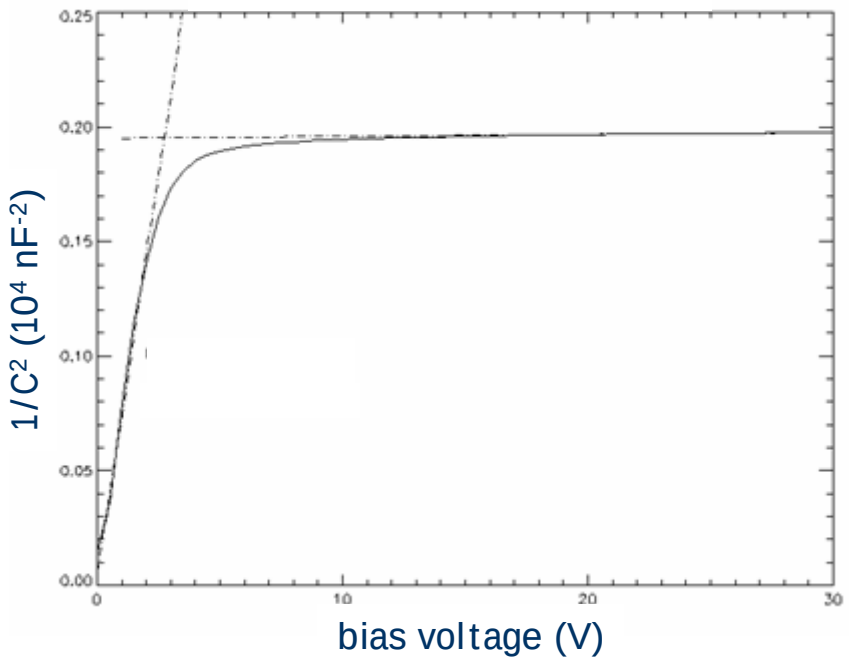


PiN Diodes on thin Silicon
- Type I: CV curves, full depletion voltage -

250 µm, type I diode, 10 mm^2



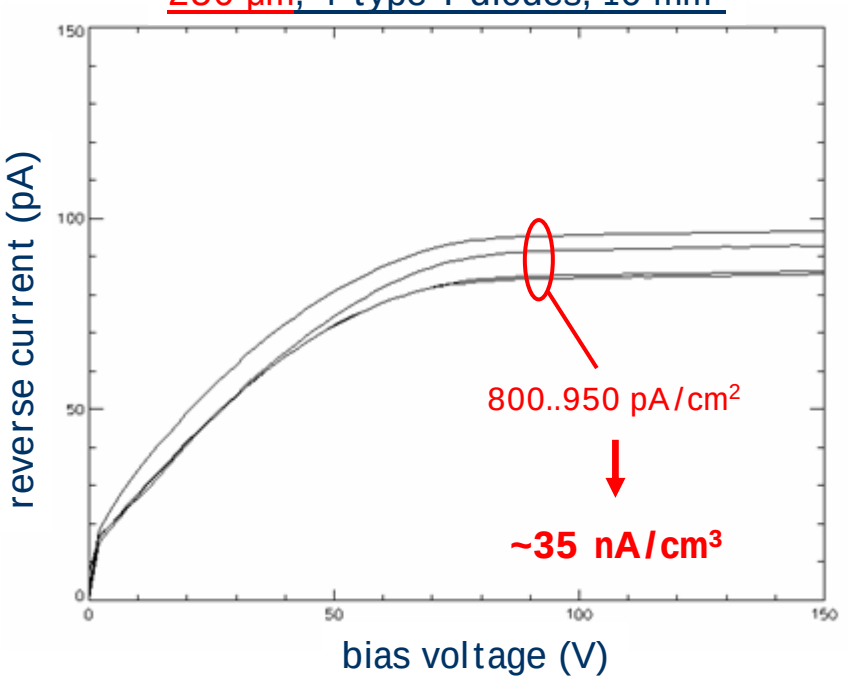
50 µm, type I diode, 10 mm^2



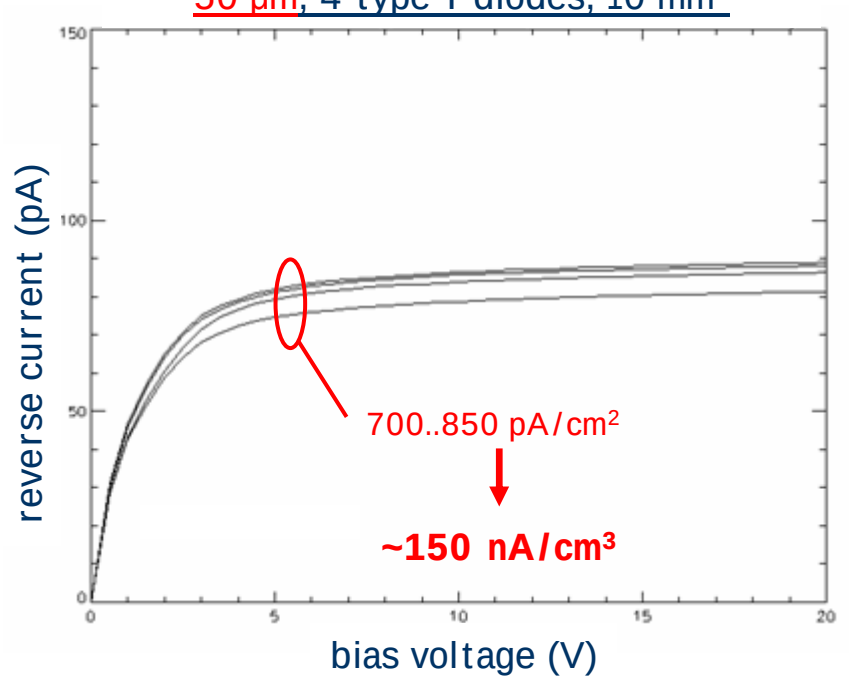
C(30V) ➔ t = 47 µm

PiN Diodes on thin Silicon
- Type I: IV curves -

250 µm, 4 type I diodes, 10 mm²



50 µm, 4 type I diodes, 10 mm²

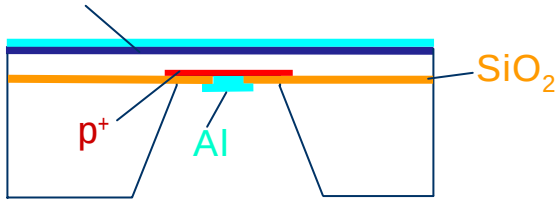


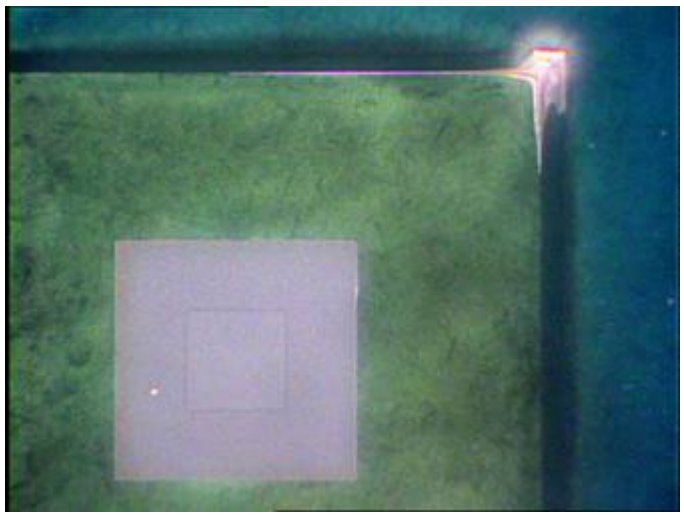
module in the first layer at TESLA: 13 cm²

→ dark current for the entire thin pixel array would be only 11nA!!!

PiN Diodes on thin Silicon
- Type II: IV curves -

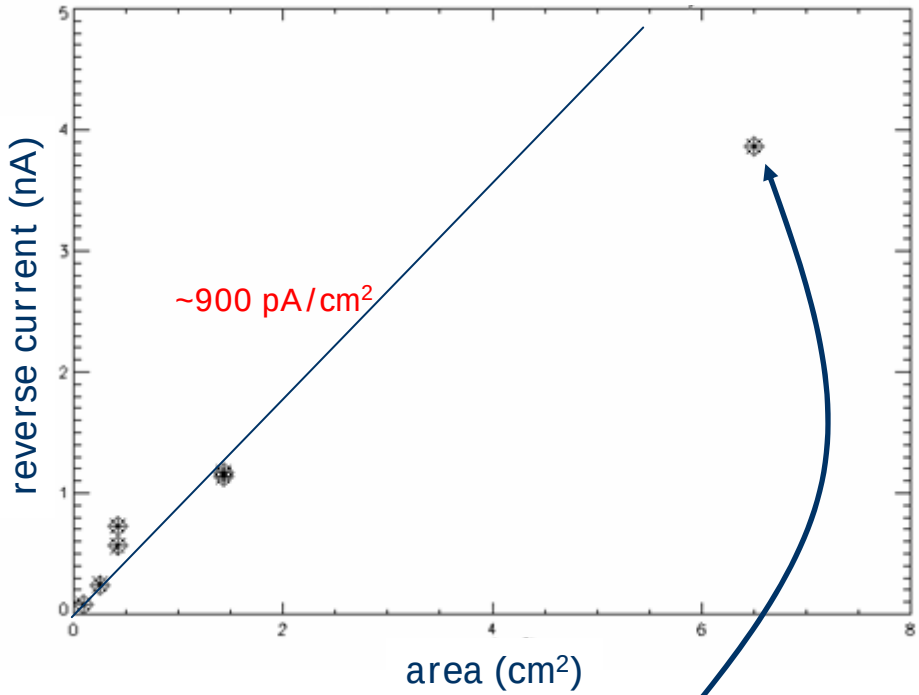
Type II: Implants like DEPFET config.





contact opening and metallization after etching of the handle wafer

Diodes of various sizes: 0.09 cm^2 – 6.5 cm^2
surface generated edge current included
reverse currents at 5 V bias



➔ about 4 nA @ 5V for the 6.5 cm^2 diode, including edge generated current

Further work

- Work done so far on 100mm Si-wafers in „application“ part of our laboratory
- Transferring technology to 150mm wafers in our production line is in progress
- Fabrication of thin DEPFET pixel detectors is planned

Summary and Conclusions

- A thinning technology based on wafer bonding and etch back for radiation sensors with implanted and structured back side was presented.
- The sensitive pixel area is thinned to 50 μm and supported by an integrated silicon frame.
- The feasibility of the thinning technology was shown:
  - Direct wafer bonding after lithography and implantation is possible
  - TMAH (with the appropriate additives) seems to be a good choice for the deep etching
  - Handling of etched wafers and diced thin chips is safe and easy
- IV/CV measurements of diodes on thin silicon are extremely encouraging: reverse current < 1 nA/cm^2 for large area PiN diodes, including edge generated current.