# STAR Heavy Flavor Tracker (HFT)

#### Constraints and Conceptual Mechanical Design

Leo Greiner, LBNL August 18, 2005

# What will be covered

- Requirements
- Conceptual mechanical design
- Some details of the prototypes already constructed.
- Future work and development.

#### A Heavy Flavor Tracker for STAR

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## **Requirements**

The primary motivation for the HFT is to extend STAR's capability to measure heavy flavor production down to very low transverse momenta by the measurement of displaced vertices. These are key measurements for the continuing heavy ion and spin physics programs at RHIC. Heavy quark measurements will facilitate the heavy ion program as it moves from the discovery phase to the systematic study of the dense medium created in heavy ion collisions as well as the nucleon spin structure in polarized p+p collisions. The primary physics topics to be addressed by the HFT include open charm measurements, thermalization, heavy quark energy loss and flow

- Requirements are driven by the physics.
- D<sup>0</sup>, open charm reconstruction.
- Reconstruction of low invariant mass events to 500 MeV/c.

### Mechanical Requirements

- 1. Position resolution of  $\sim 10 \ \mu m$ .
- 2. Low mass / radiation length. MCS is a factor.  $(X_0 \sim 0.3\% / layer)$
- 3. Coverage of -1 < eta < 1
- 4. Radiation hard to ~2K RAD/year

#### Additional Functional Requirements:

•Easy to calibrate.

- •Easy to align.
- •Easy to remove, repair and replace without re-survey.
- •Fit easily into the existing detector and infrastructure at STAR.

#### Conceptual mechanical design



Kinematic mount shown for HFT

### STAR HFT

- Two layers
  - 1.5 cm radius
  - 4.5 cm radius
- 24 ladders
  - 2 cm X 20 cm
    each
  - ~ 100 Mega Pixels





Purpose: Greatly improve D meson capability in STAR

#### Ladder Constituents



There are 3 basic constituents of a sensor ladder as shown below;

- 1. APS + RDO ASIC
- 2. Cable
- 3. Mechanical Carrier



2 prototype designs

End view

#### Sensor / RDO ASIC

#### MIMOSTAR Sensor – under development at IRES

Min I efficiency	98%
Accidental rate	< 100 /cm <sup>2</sup>
Position resolution	< 10 µm
Pixel dimension	$30 \ \mu\text{m}  imes 30 \ \mu\text{m}$
Detector chip active area	19.2 mm× 19.2 mm
Detector chip pixel array	640× 640

#### **RDO ASIC – under development at LBNL**

•ADC – 10 bit ADC for signals from sensor chip

•CDS – Chip will perform correlated double sampling and zero supression.

•High speed LVDS outputs

•Configuration, control, clock, synch functions

Both chips thinned to 50  $\mu$ m thickness. X<sub>0</sub> = 0.053 % each

#### <u>Cable</u>

- •~ 100 traces (2 LVDS pairs / sensor, clk, power, gnd, cntl )
- •4 layer design, 25 µm kapton, 20 µm Al conductor
- •Impedance controlled signal / clock pairs with power and ground geometrically arranged as shielding.

Prototype cable



X<sub>0</sub> =0.090 %

#### **Carrier**

2 carrier candidates





Top layer =  $50 \ \mu m \ CFC$ Middle layer =  $3.2 \ mm \ RVC$ Bottom layer =  $50 \ \mu m \ CFC$  Outer shell = 100  $\mu$ m CFC Fill = RVC

X<sub>0</sub> =0.11 %

### **Carrier**



Plot shows fundamental resonance frequency measured with a capacitance probe.

Measured = 139 Hz

Calculated = 135 Hz





#### Total Radiation Length / Ladder

<u>Component</u>	<u>% radiation</u> <u>length</u>	<u>Si equivalent</u> (µm)
RDO chip	0.0534	50
Adhesive	0.0143	13.39
MIMOSA detector	0.0534	50
Adhesive	0.0143	13.39
Cable assembly	0.090	83.92
Adhesive	0.0143	13.39
Carbon fiber / RVC beam	0.11	103
<u>Total</u>	<u>0.35</u>	<u>327.09</u>

#### Prototype Status

•Prototypes have been constructed and tested for both carrier candidates. Results are encouraging and consistent with calculations.

•A prototype cable has been designed and constructed (Cu conductors)

•These structures have been fashioned into prototype ladders using thinned 50 µm MIMOSA5 detectors. (Single ended output). We are reading multiple detectors into an ADC / DAQ system. This tests many of the mechanical handling and assembly tasks needed.



### **Future Work**

- •Further testing of prototypes
- •Prototype kinematic mount
- •Work on ASIC development
- •Etc.