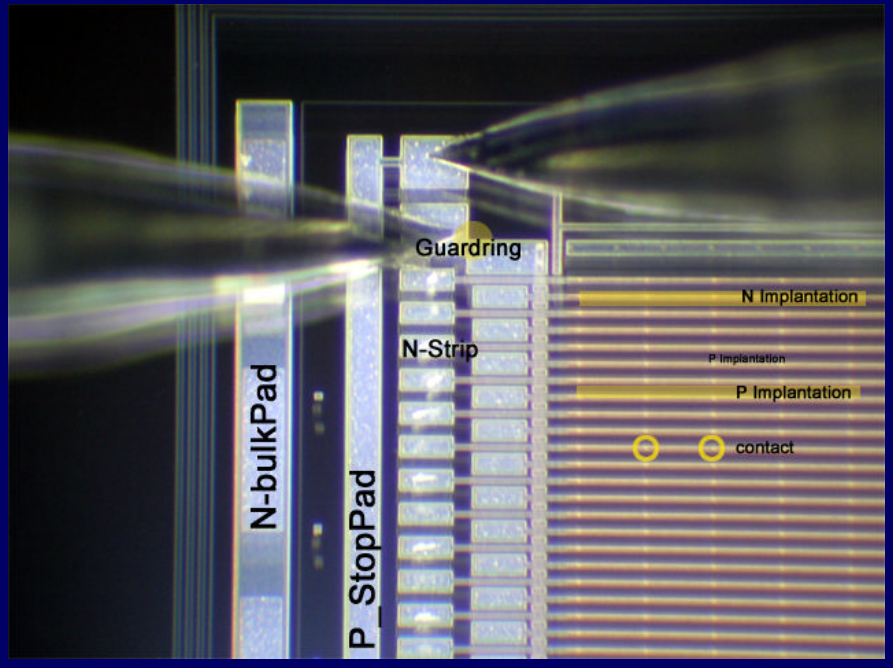
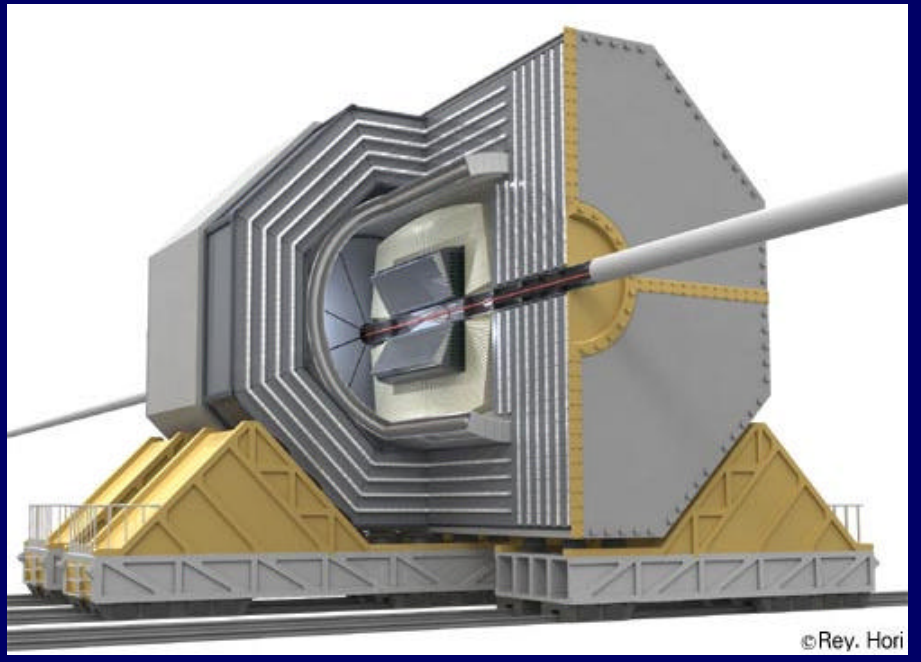
Status of DSSD R&D for Silicon Inner Trackers

Eunil Won
Korea University





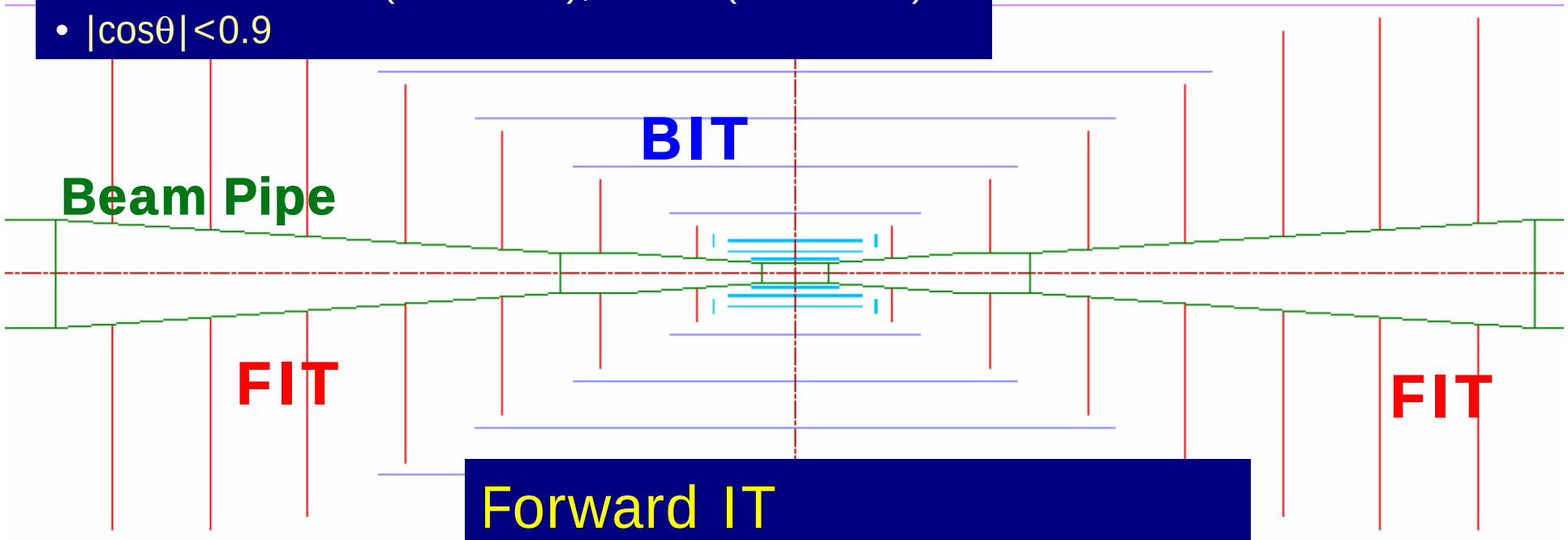
Outline

- Inner trackers in GLD
- DSSD Design and Fabrication
- DSSD Electrical Characteristics
- Radiation Hardness/source test
- Readout Status
- Summary

Barrel/Forward Intermediate Trackers ("snowmass parameters")

Barrel IT

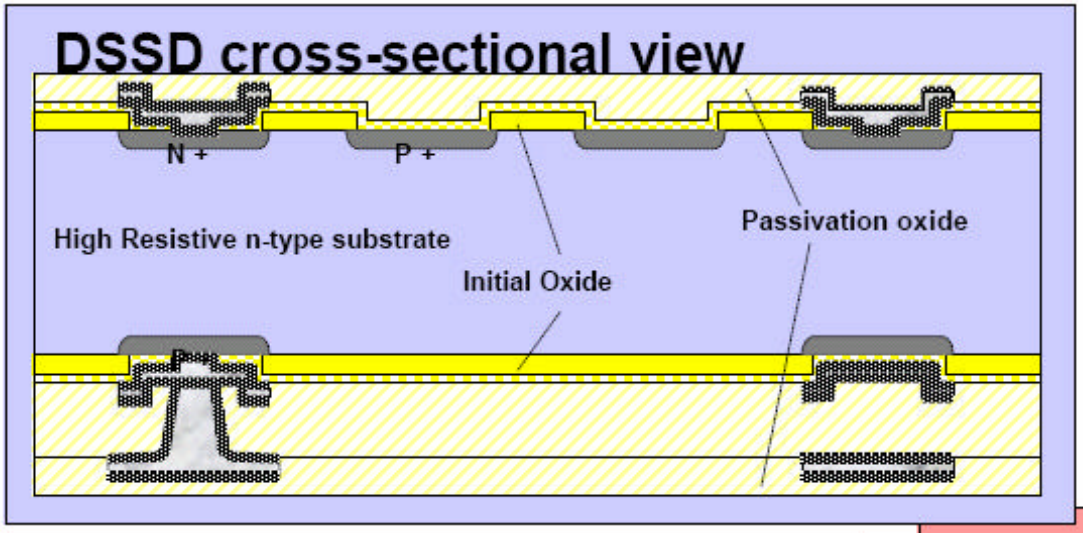
- spatial resolution 10 μm
- 4 layers (thickness 561 μm Silicon strip)
- r=9 cm (innermost), 30 cm (outermost)
- half z = 18.5 cm (innermost), 62 cm (outermost)
- $|\cos\theta|<0.9$



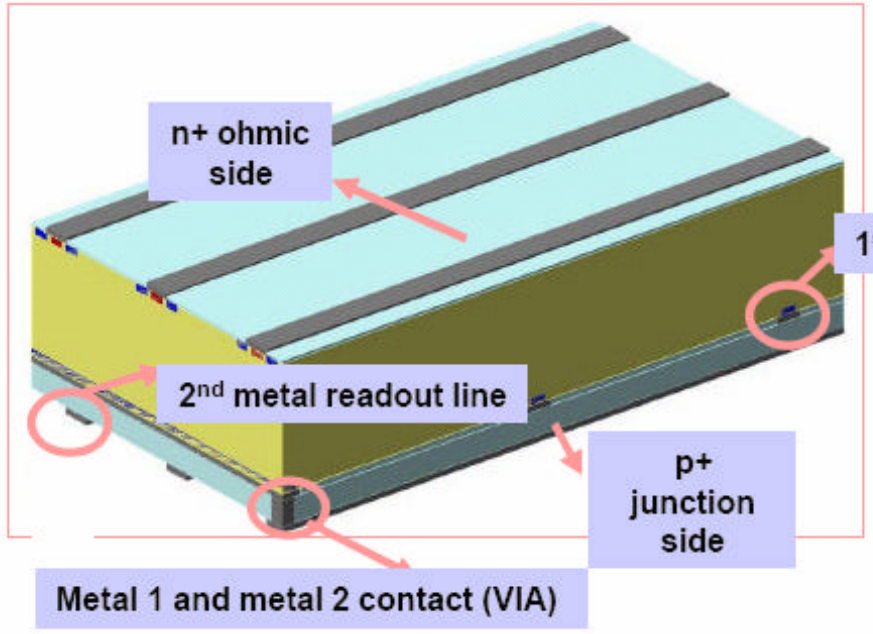
Forward IT

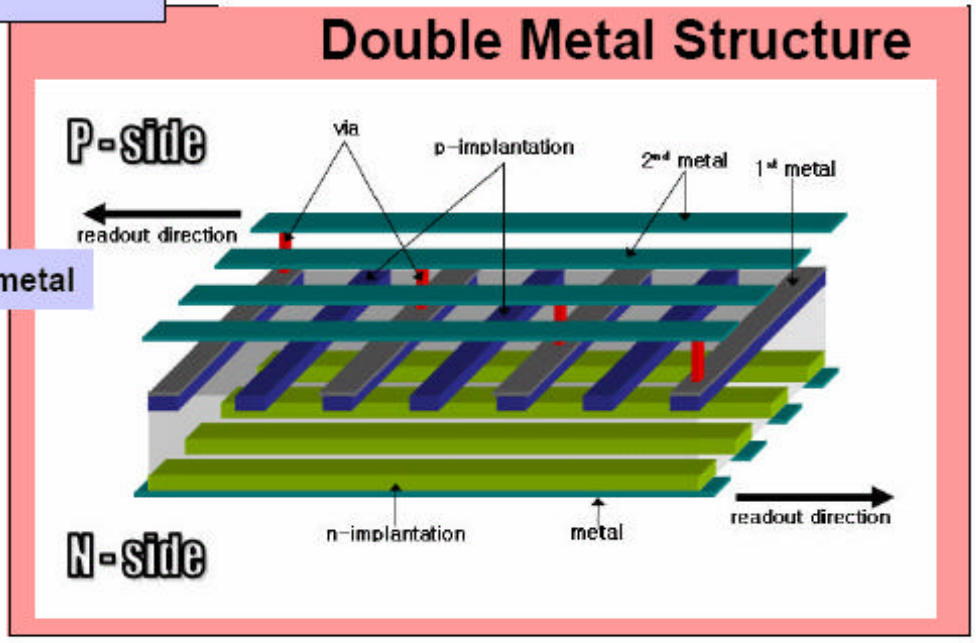
- spatial resolution 10 μm
- 7 layers (thickness 561 μm Silicon strip)

DSSD Schematics



- 5 inch wafer technology
- n-type substrates
- DC type sensors
- p side readout from vias (double metal structure)
- 11 masks in total





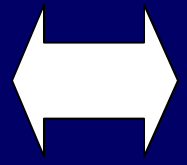
DSSD Parameters

List	DC-type		Unit
	p side	n side	
sensor size	55610 x 29400		μm
wafer thickness	380		μm
pitch	100	50	μm
readout trace pitch	50	50	μm
implant strip #	511	511	-
number of readout	511	511	-
strip length	25600	51072	μm
strip width	9	9	μm
number of masks	6	5	–

DSSD R&D flowchart

Kyungpook/
Seoul Nat. Univ

- mask design
- DSSD simulation
- Sensor characteristics measurements
- Radiation damage tests



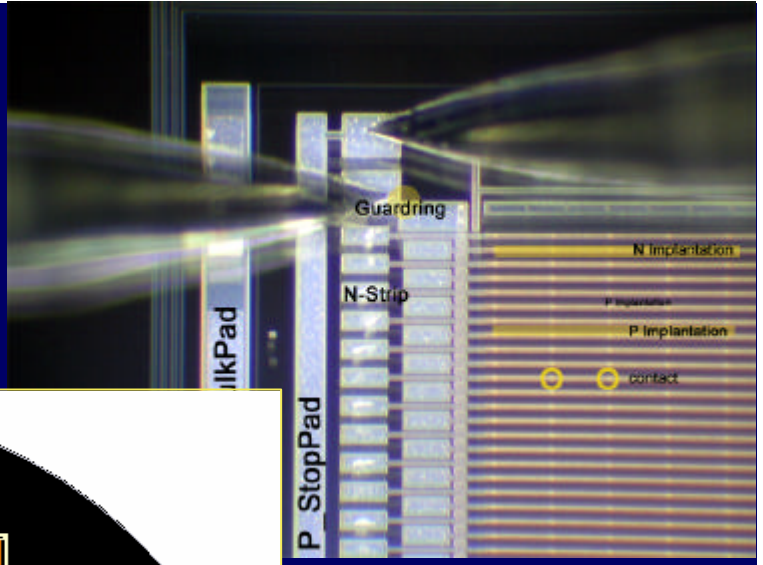
Korea/Chonnam Univ

- hybrid development
- Readout Electronics

Minimum commercial partners involved in the R&D process

: may be able to achieve competitive price/quality over existing choices

N-side Design



64ch 50μm pitch

32ch 50μm pitch

16ch 50μm pitch

Rear-side of SSD

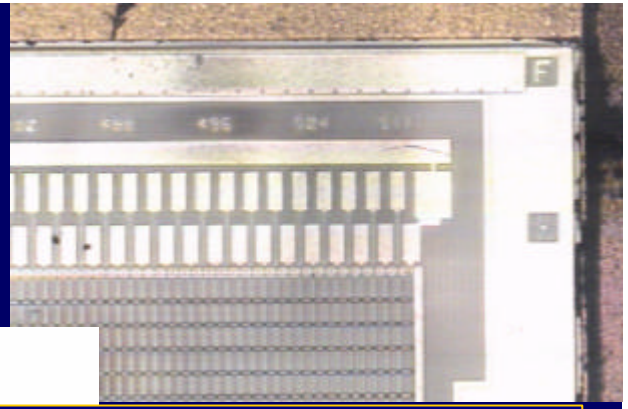
511ch 50μm pitch

1x1cm^2 PIN diode

Pixel Array

For SDD R&D

P-side Design

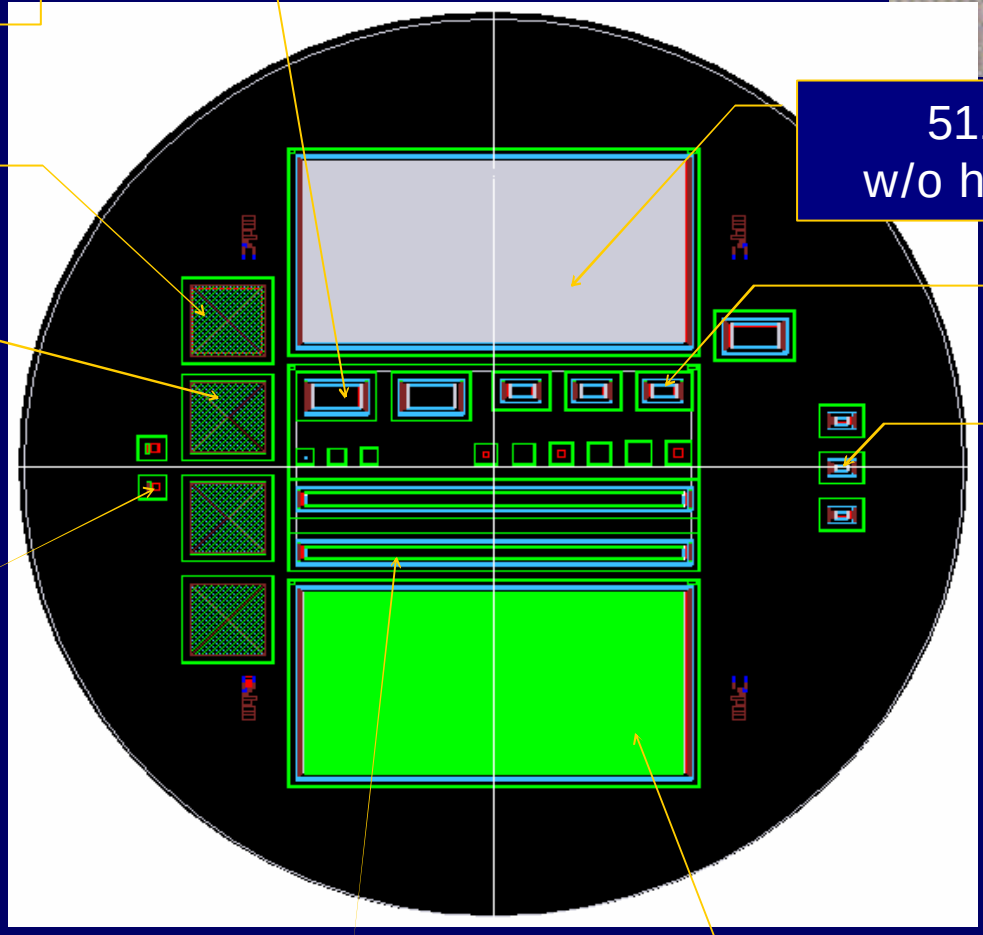


64ch 100μm pitch

1cm PIN diode

For SDD R&D

Pixel array



511ch 100μm pitch
w/o hourglass (sensor-1)

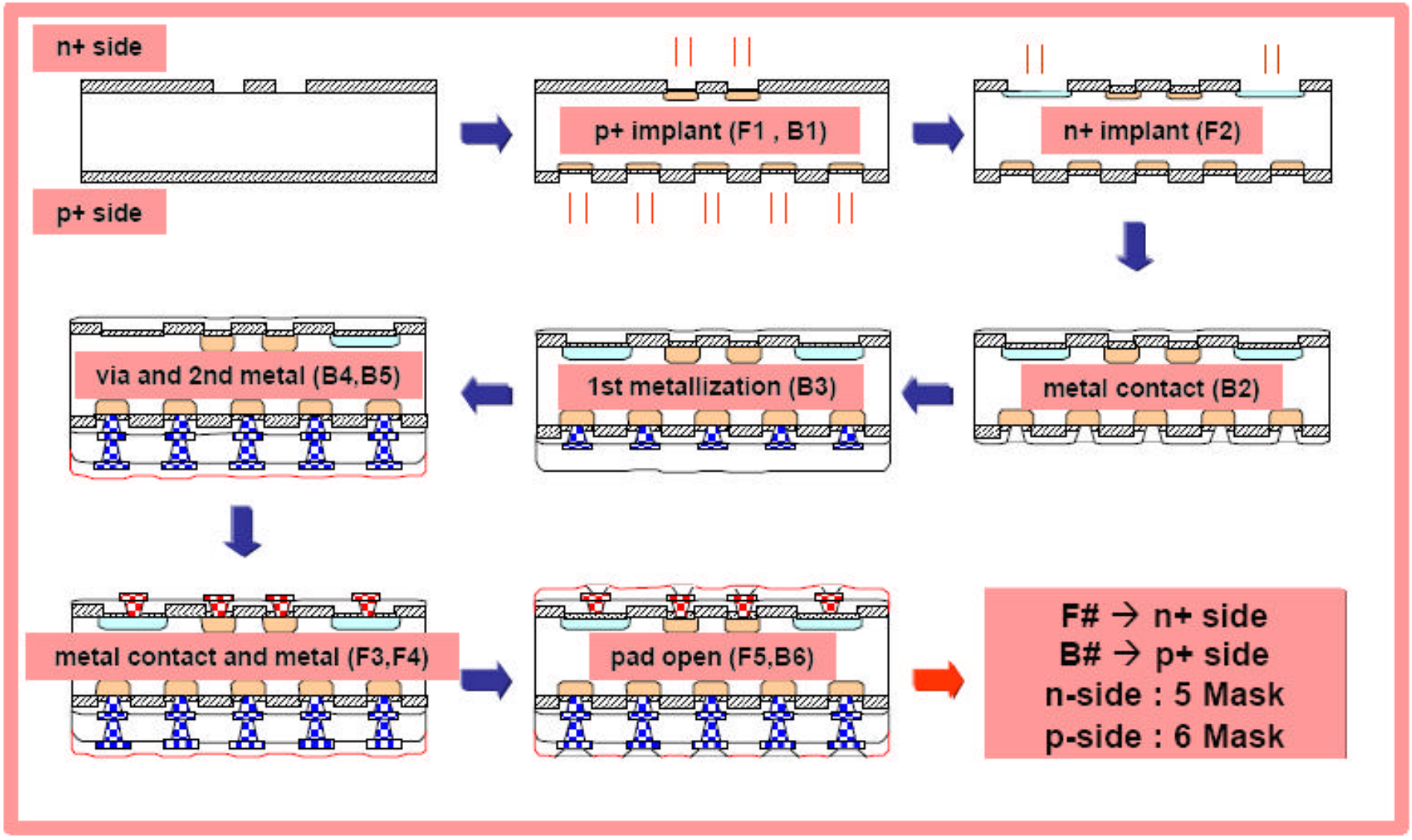
32ch 100μm pitch

16ch 100μm pitch

16ch 100μm pitch SSD

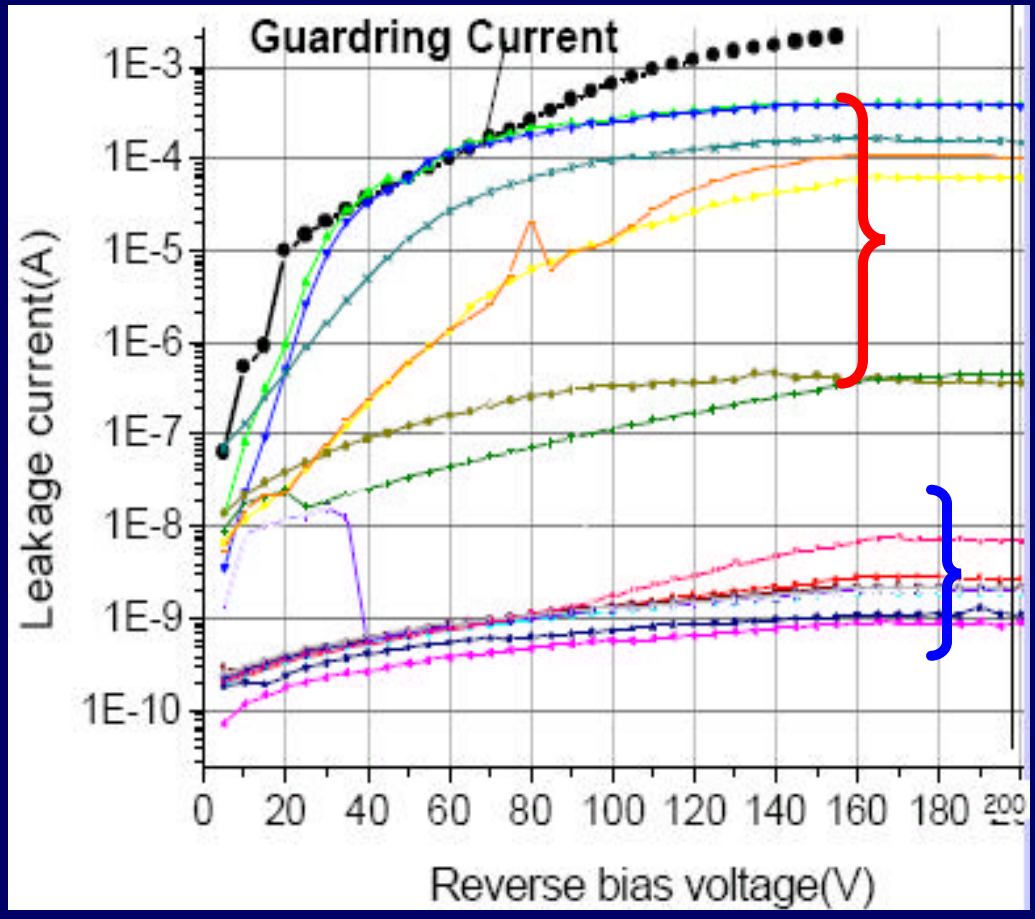
511ch 100μm pitch
w/ hourglass (sensor-2)

DSSD Fabrication



DSSD's from 1st Fab out

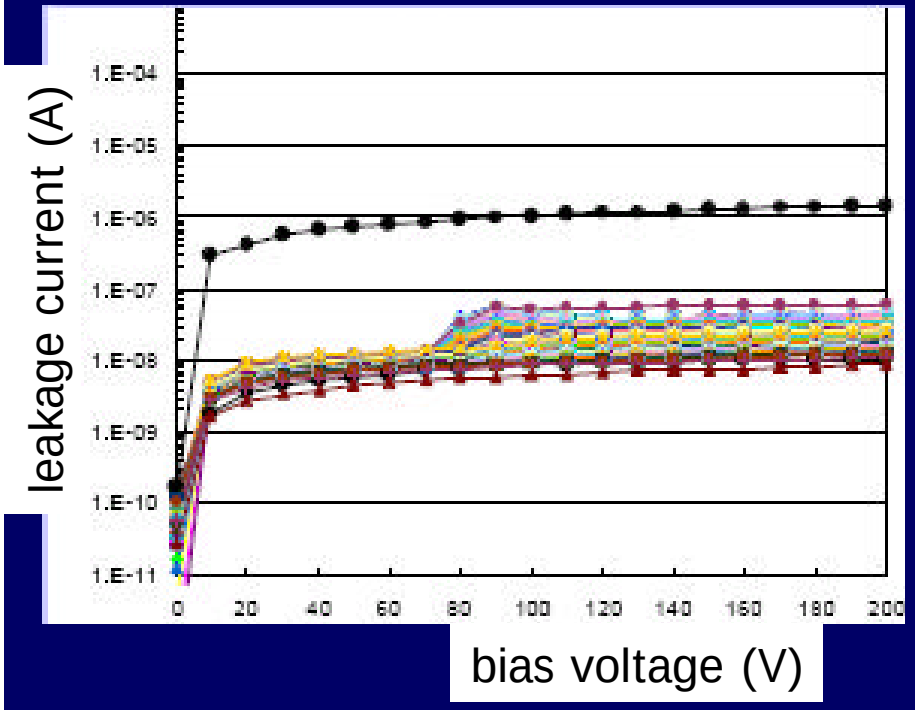
P-side IV



- P-side Guard Ring
  ~ 1mA/sensor @100V
- Lots of extremely leaky P-strips
- Some good P-strips
  ~ <10nA/strip @100V

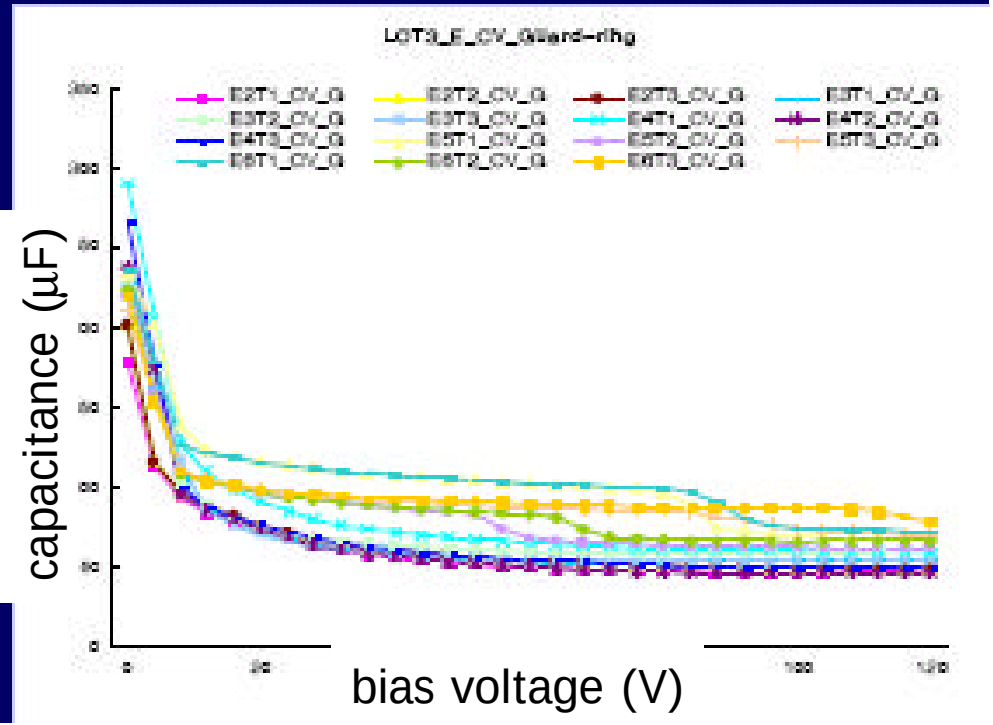
After seeing this, we tried out countless experiments to improve the sensor quality

DSSD's from Latest Fab out



- P-side Guard Ring ~ 1uA/sensor @100V
- All P-strips ~ 8-50nA/strip @100V
- No extremely Leaky P-strips

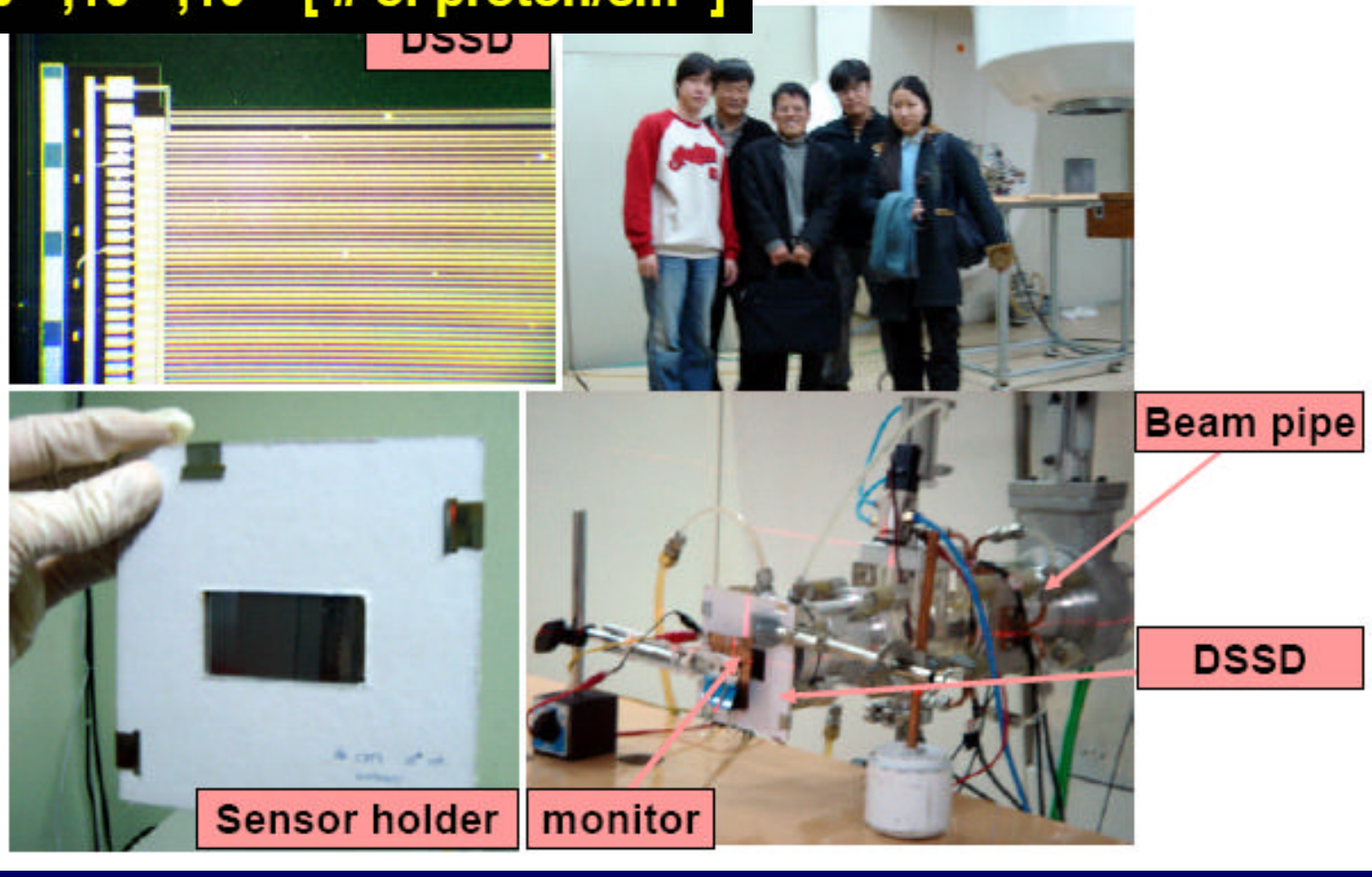
- Full Depletion Voltage ~70V
- Operation Voltage ~100V



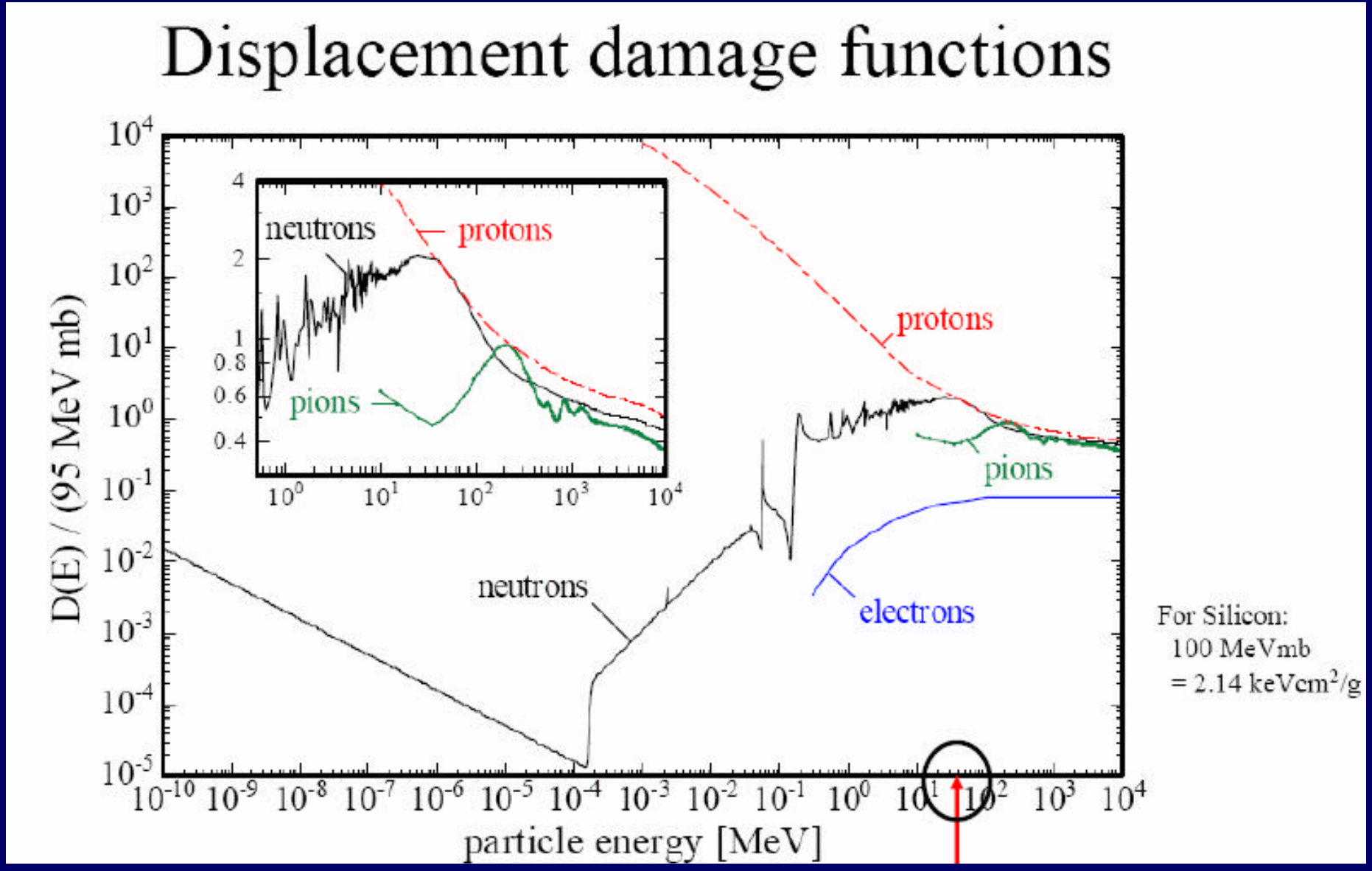
Radiation Hardness Test

cyclotron in Korea Institute of Radiological and Medical Sciences : 35MeV proton cyclotron

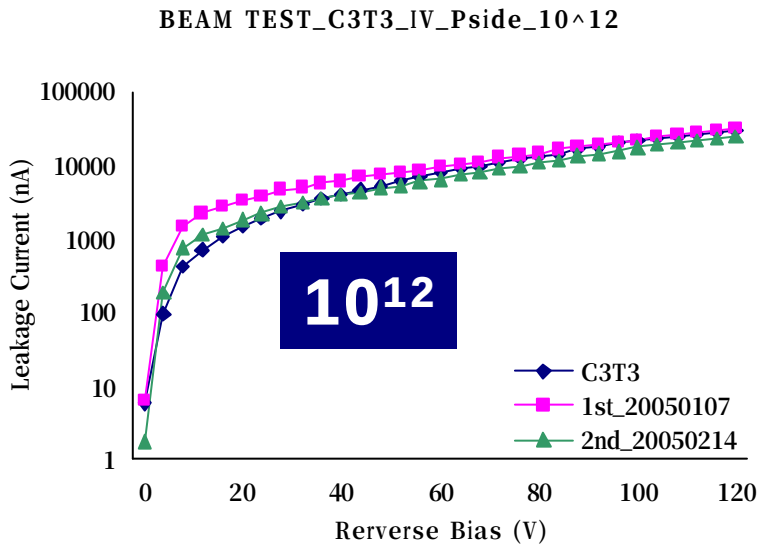
10^{12} ,10^{13} ,10^{14} ,10^{15} [# of proton/cm^2]

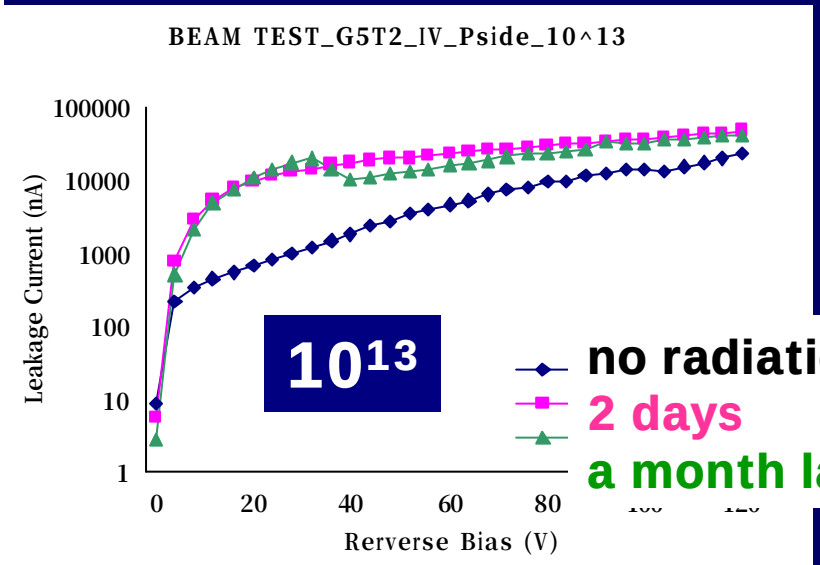


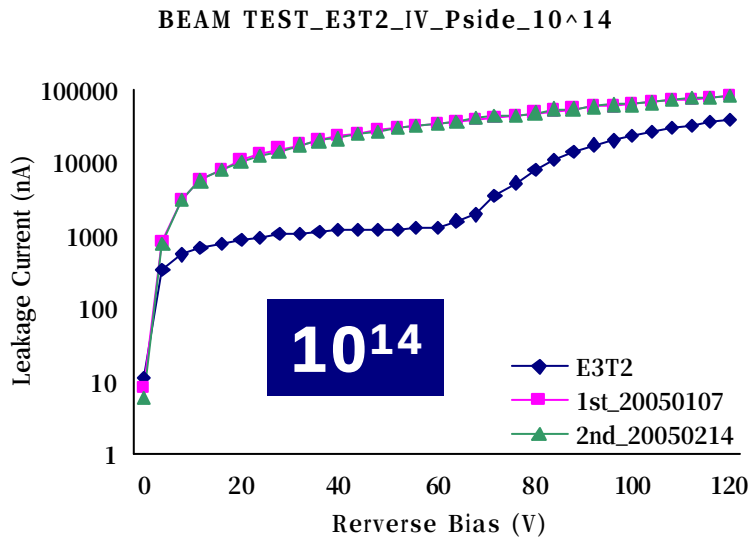
Radiation Damage

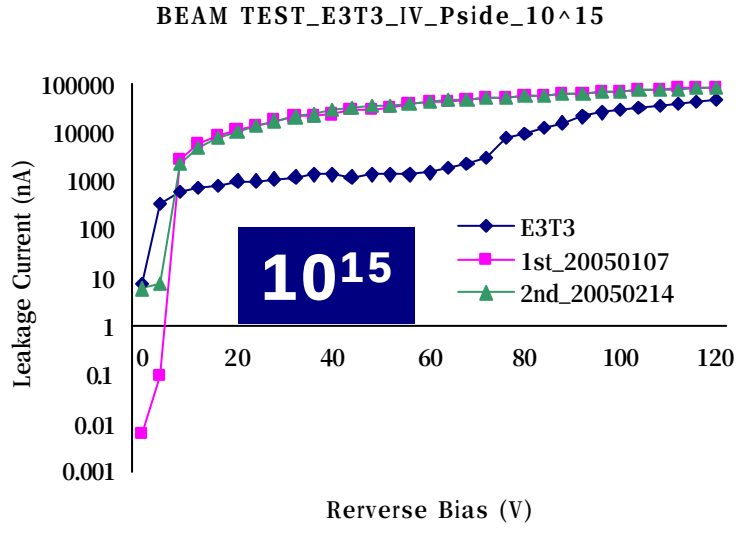


IV before and after irradiation



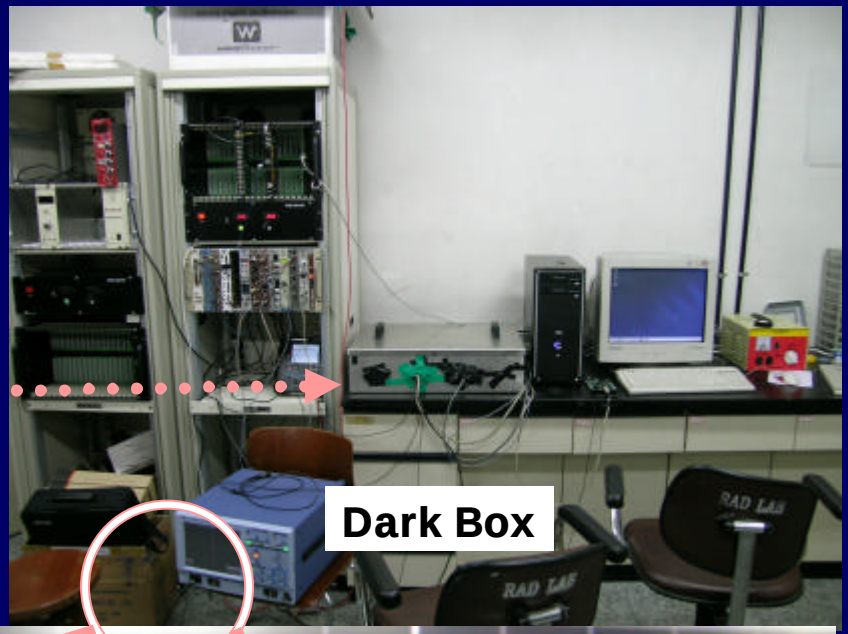


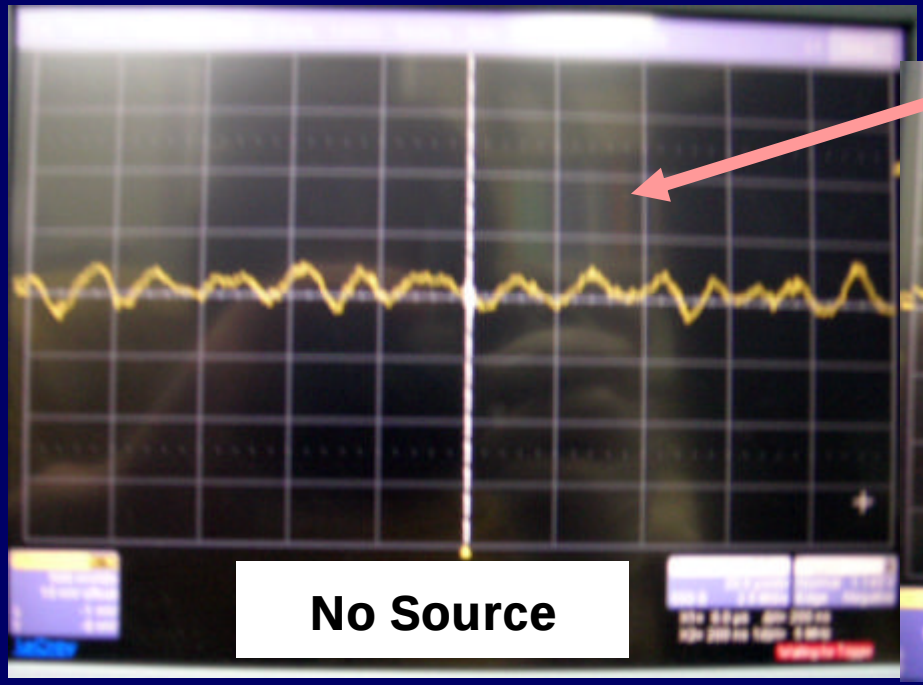


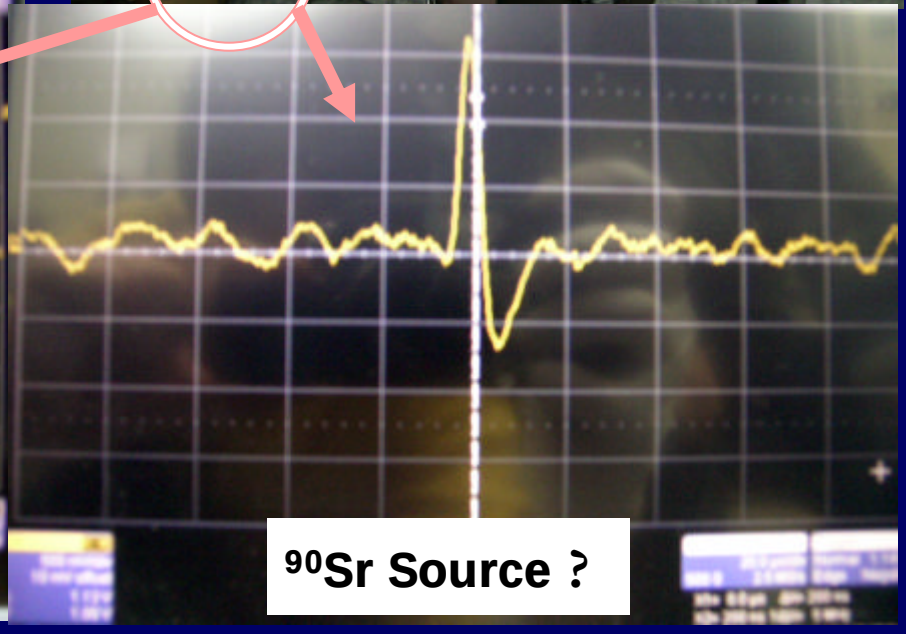


Source Test

- signals from p-side pads (~20) pasted together
- no per-pad signal yet (requires VA-like readout)

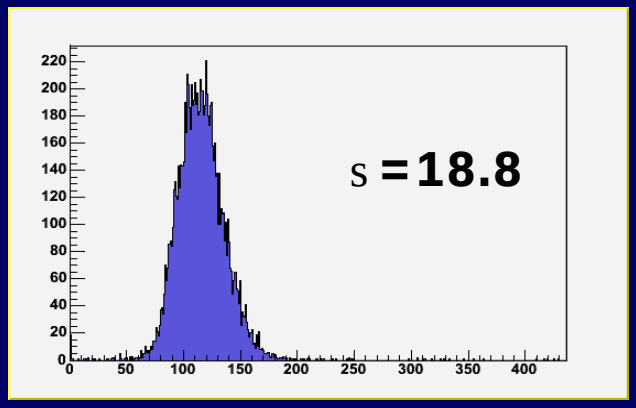




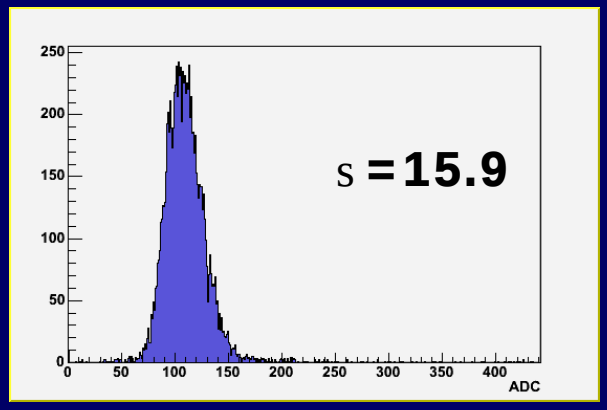


Source Test (cont)

Pedestals

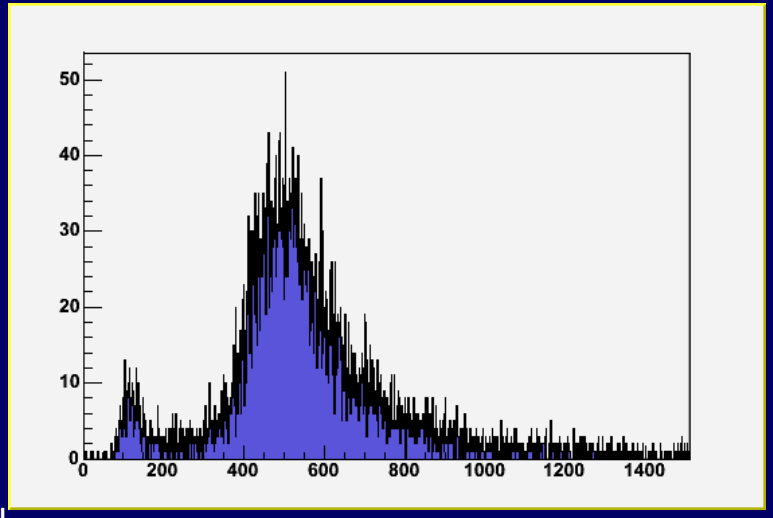


HAMAMATSU SSD



DSSD 32ch pattern

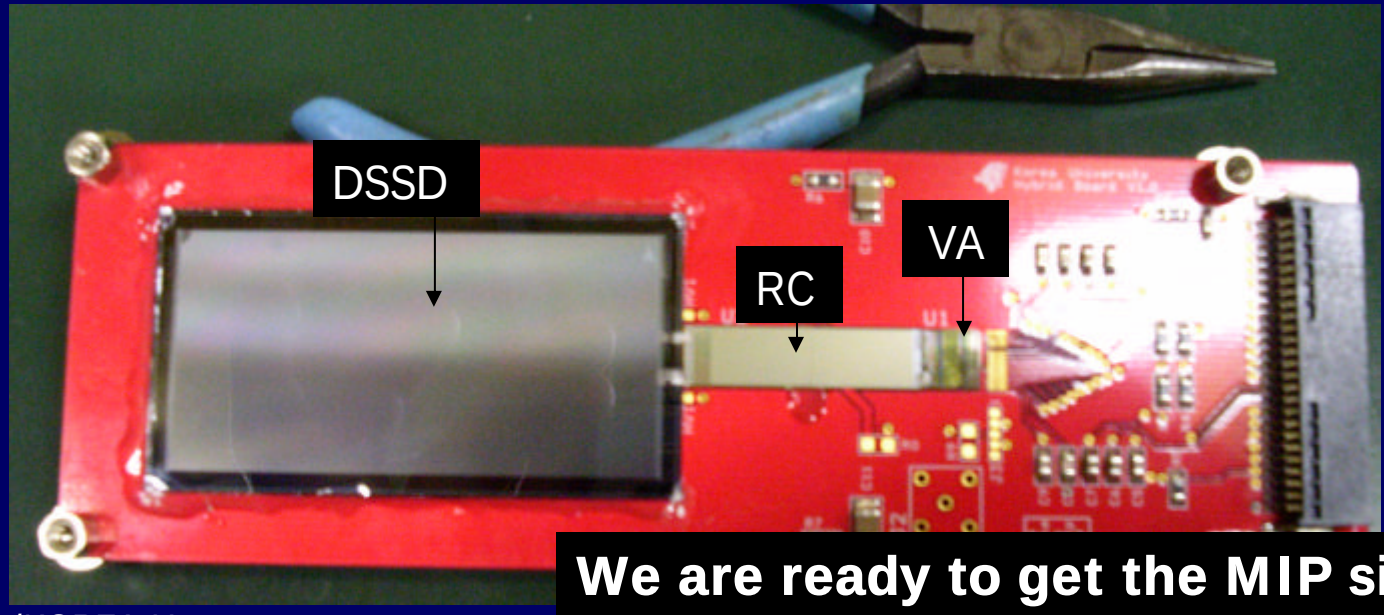
S/N of DSSD 32ch pattern



Signal mean = 504.3
Pedestal mean = 108.6
Pedestal sigma = 15.9
S/N = 25

Status of Hybrid Board

- **We mounted latest fab out DSSDs to the hybrid** (August 9)
  - ✓ VA1 + RC sensor + 511 channel DSSD
- **Wire bonding done** (August 11)
  - ✓ pads – VA : by a company (LP electronics in Korea)
  - ✓ VA – RC, RC – DSSD : done by a KEK expert (T.Tsuboyama)

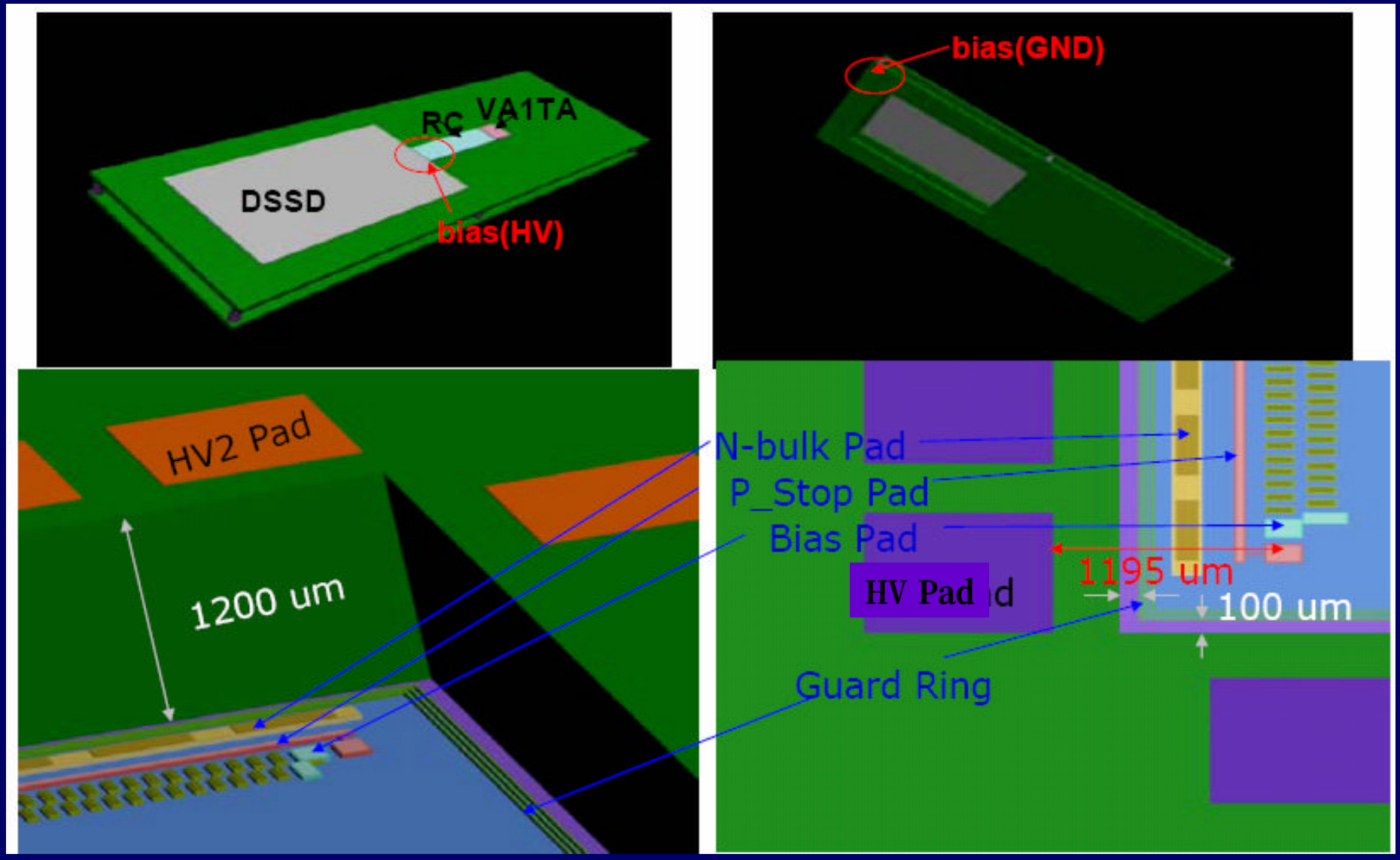


We are ready to get the MIP signal!

Summary

- **DSSD Design and Fabrication :** 1st design sensors all fab out & fab of new design sensors in progress
- **Radiation Hardness Test :** Not seen much effect with 10^{12} p/ cm^2 & more tests coming
- **Source Test :** Seen a reasonable S/N with a 32ch DSSD pattern & more tests coming
- **Readout electronics :** built & reading out in progress

Hybrid Board Design

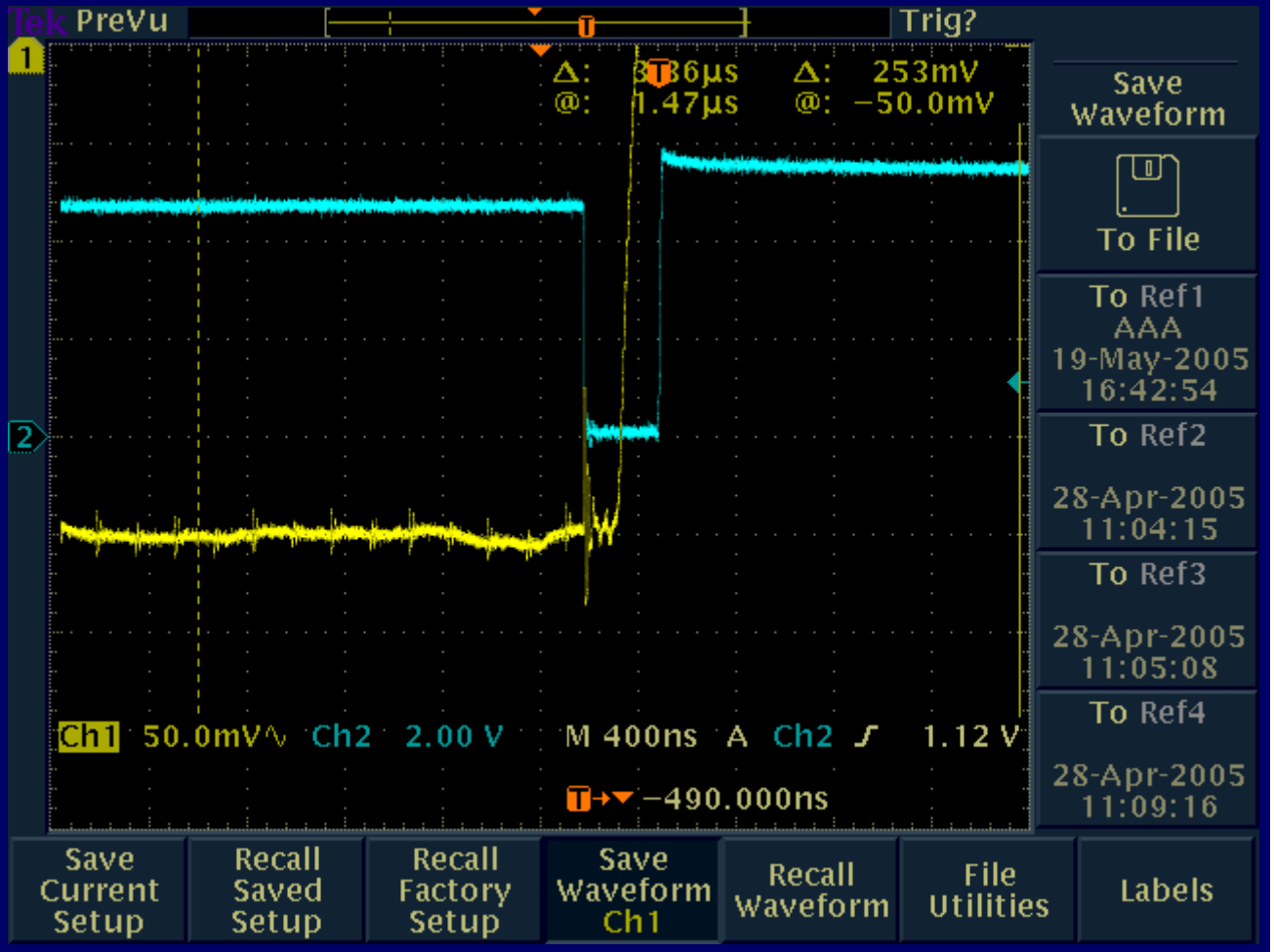


Status of Hybrid Board

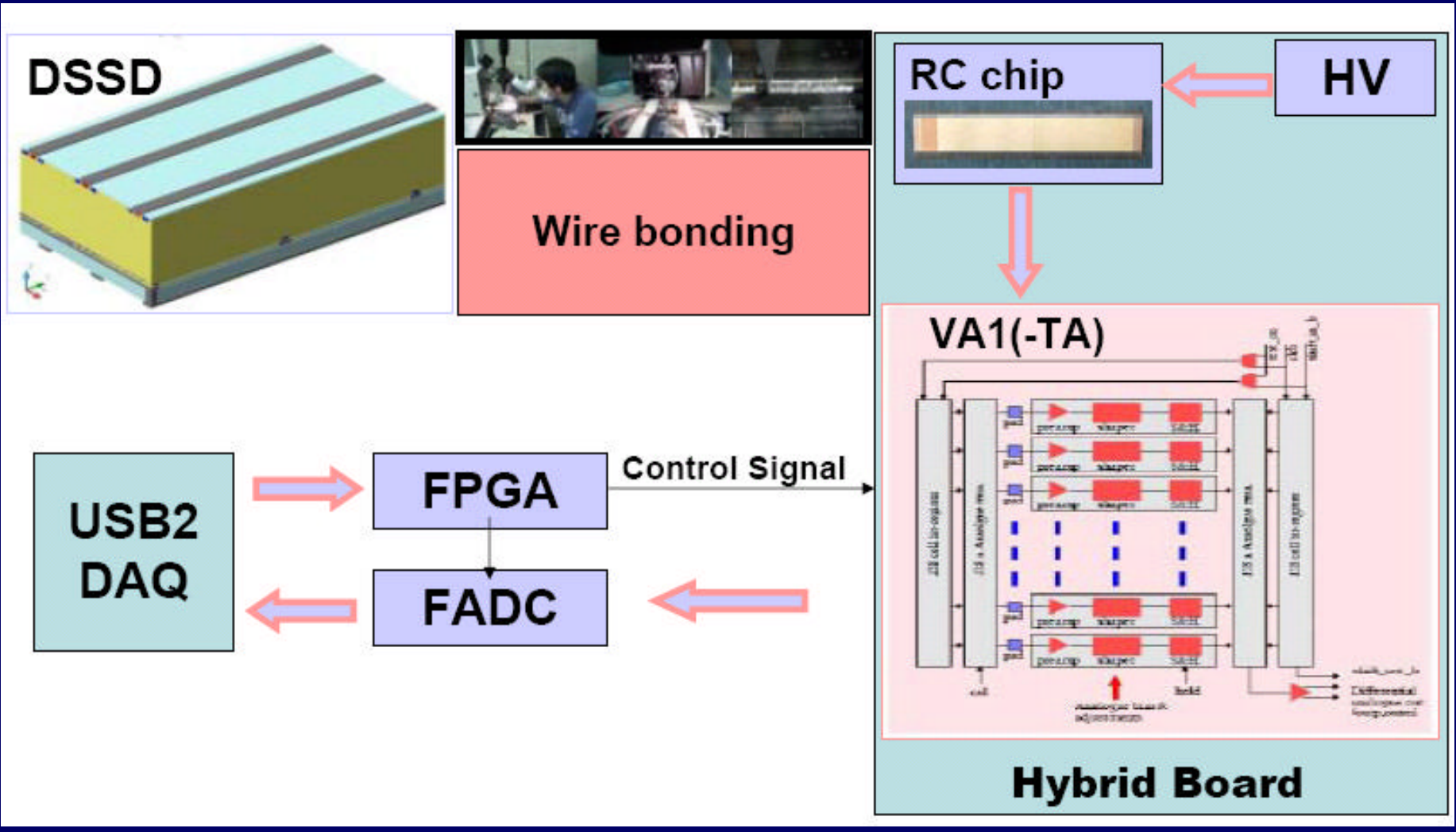
shift_out_b

out_p

small spikes (due to clock?)

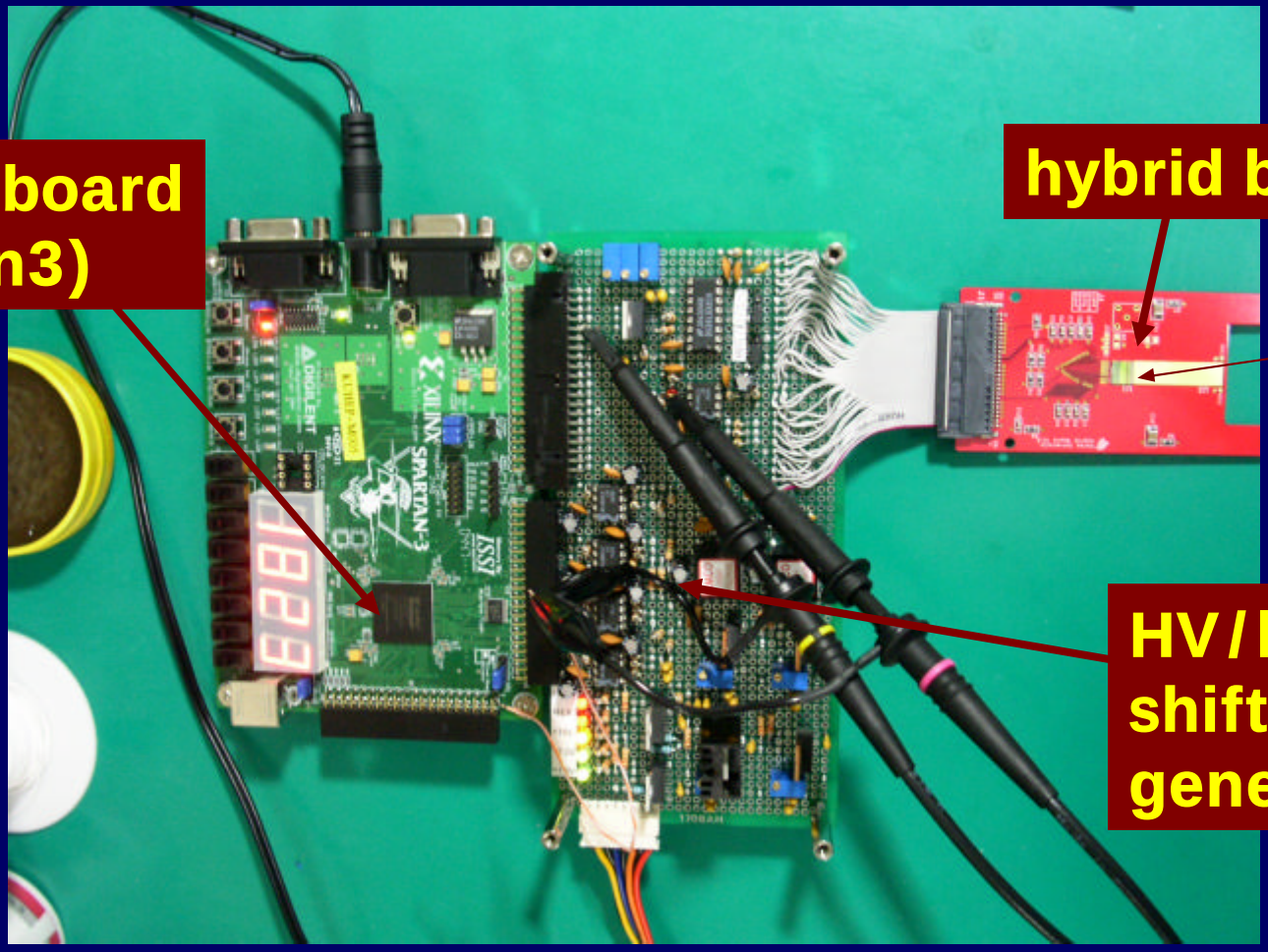


DSSD Readout Schematic

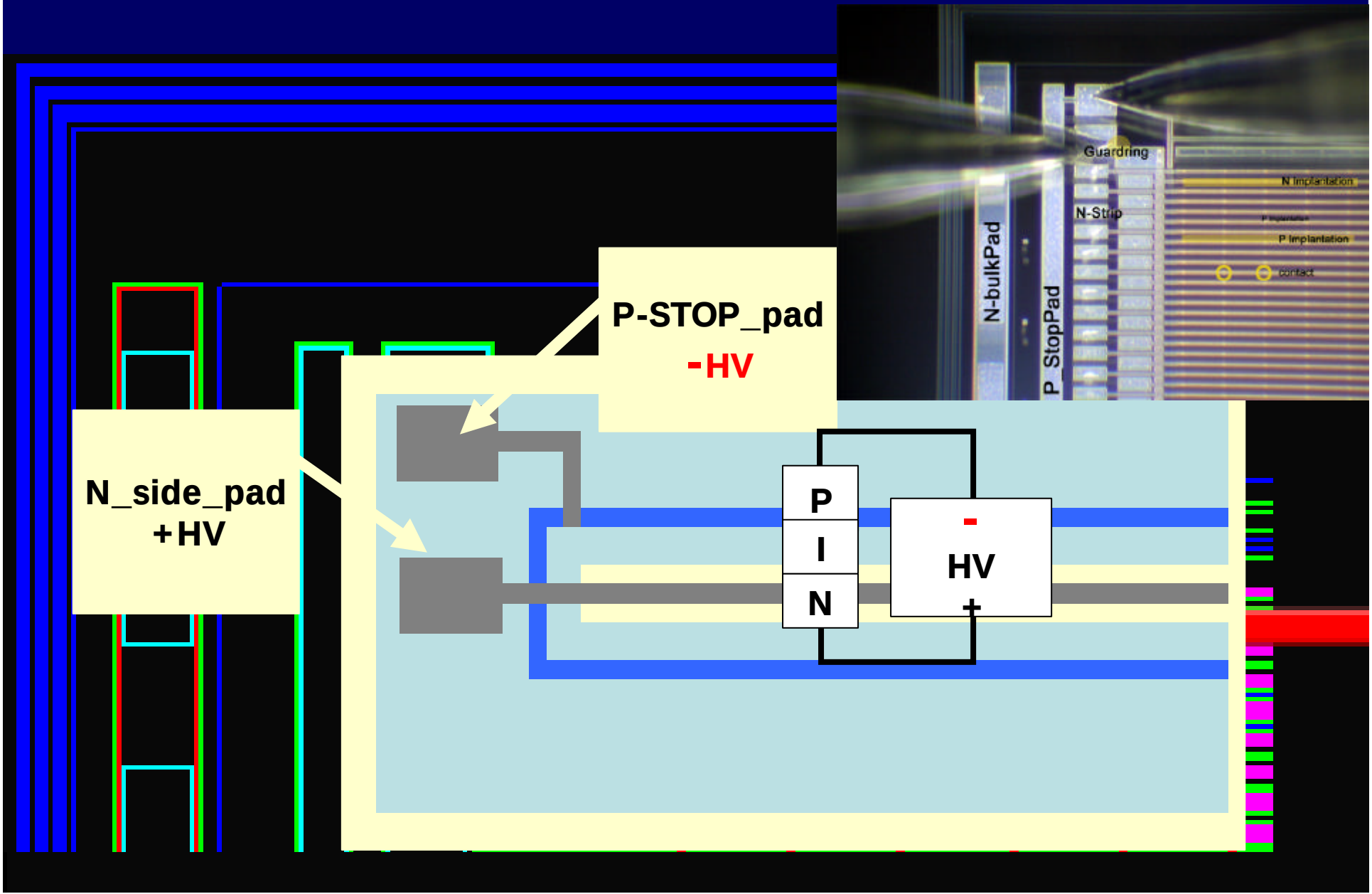


Status of Hybrid Board

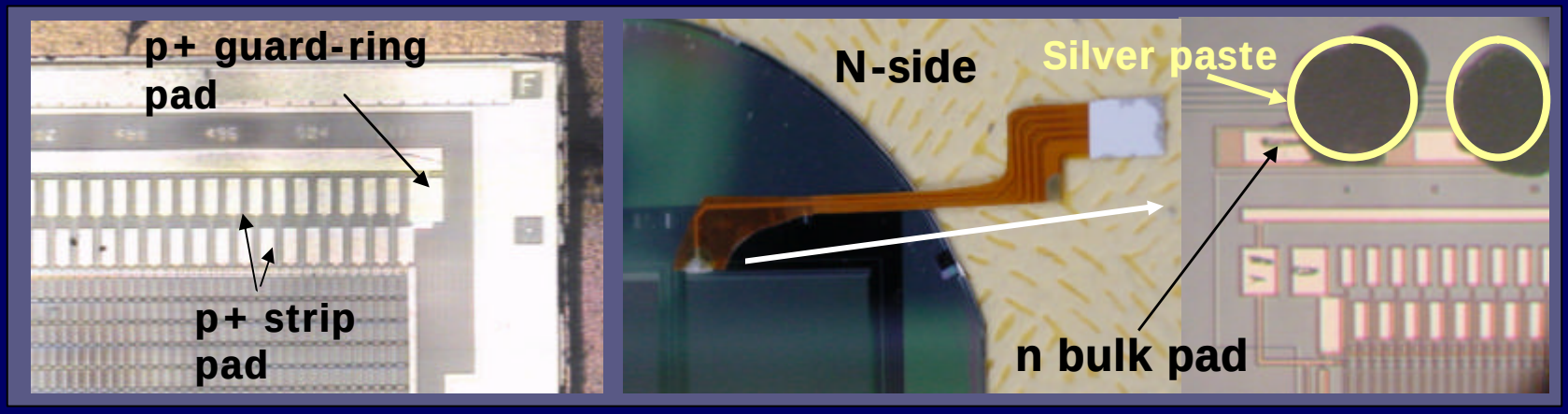
Hybrid board was powered up (July 2)



N-side Test Setup



P-side Test Setup



P-side TEST probes bulk characteristics