# Progress towards a Long Shaping-Time Readout for Silicon Strips

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SCIPP & UC Santa Cruz
Snowmass Linear Collider Workshop
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# Overview

## Status as of LCWS05

- Test bench prepared
- NLC-oriented LSTFE-1 chip received, but basic design flaw precluded testing

## Current Status

- Test-bench control system completed
- Cold-technology-oriented LSTFE-2 designed & fabricated; tests beginning
- Long-ladder assembly under construction
- Back-end (digital) architecture designed and tested

# The SCIPP/UCSC ILC HARDWARE GROUP

| Faculty/Senior | Post-Docs | Students |
|---|---|---|
| Alex Grillo | Gavin Nesom | Michael Young |
| Hartmut Sadrozinski | Jurgen Kroseberg | Kunal Arya (Com-puter Eng. |
| Bruce Schumm | | |
| Abe Seiden | | |

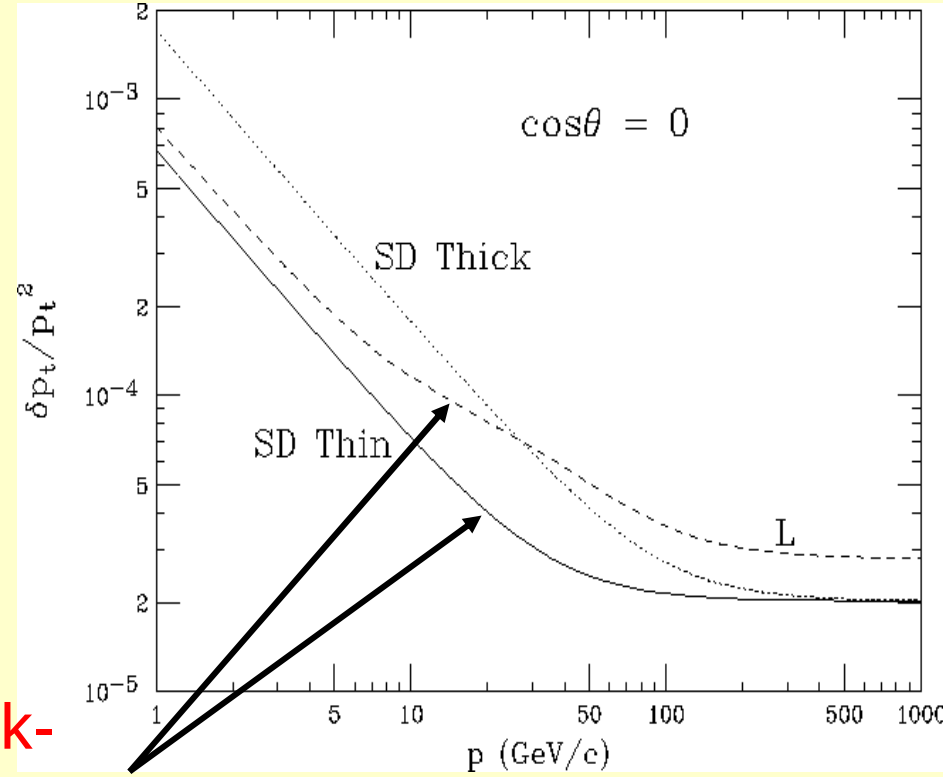
**Lead Engineer: Ned Spencer**

**Technical Staff: Max Wilder, Forest Martinez-McKinney**

# The Gossamer Tracker

Ideas:

- Long ladders ➔ substantially limit electronics readout and associated support
- Thin inner detector layers
- Exploit duty cycle ➔ eliminate need for active cooling




➔ Competitive with gaseous tracking over full range of momenta

Also: forward region...

# THE LSTFE-2 CHIP

Long shaping-time front end suppresses 1/f noise, allowing for long-ladder readout

Power cycling should reduce IR heating by close to x100

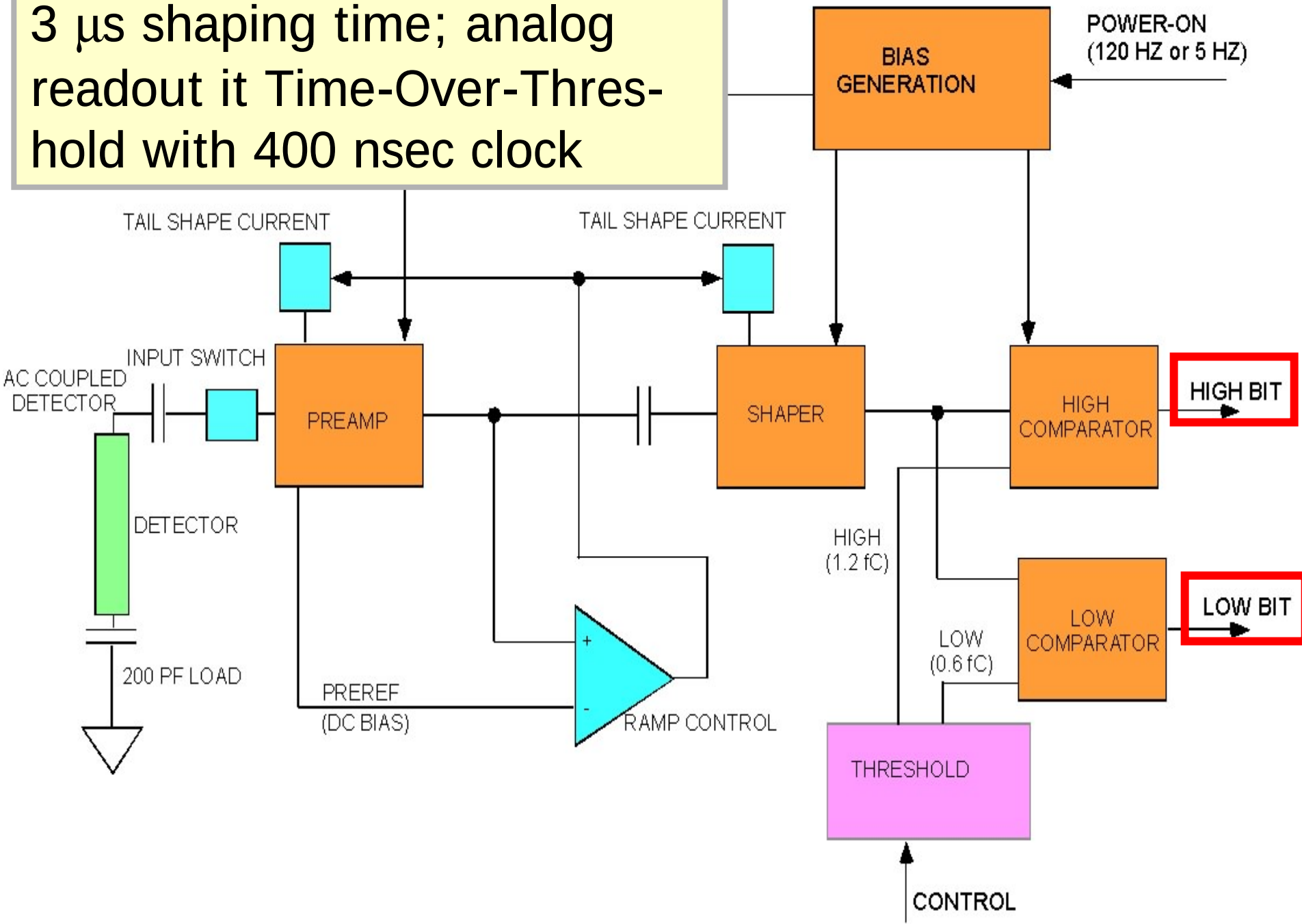
Analog measurement via time-over-threshold (TOT) from low-threshold “readout” comparator.

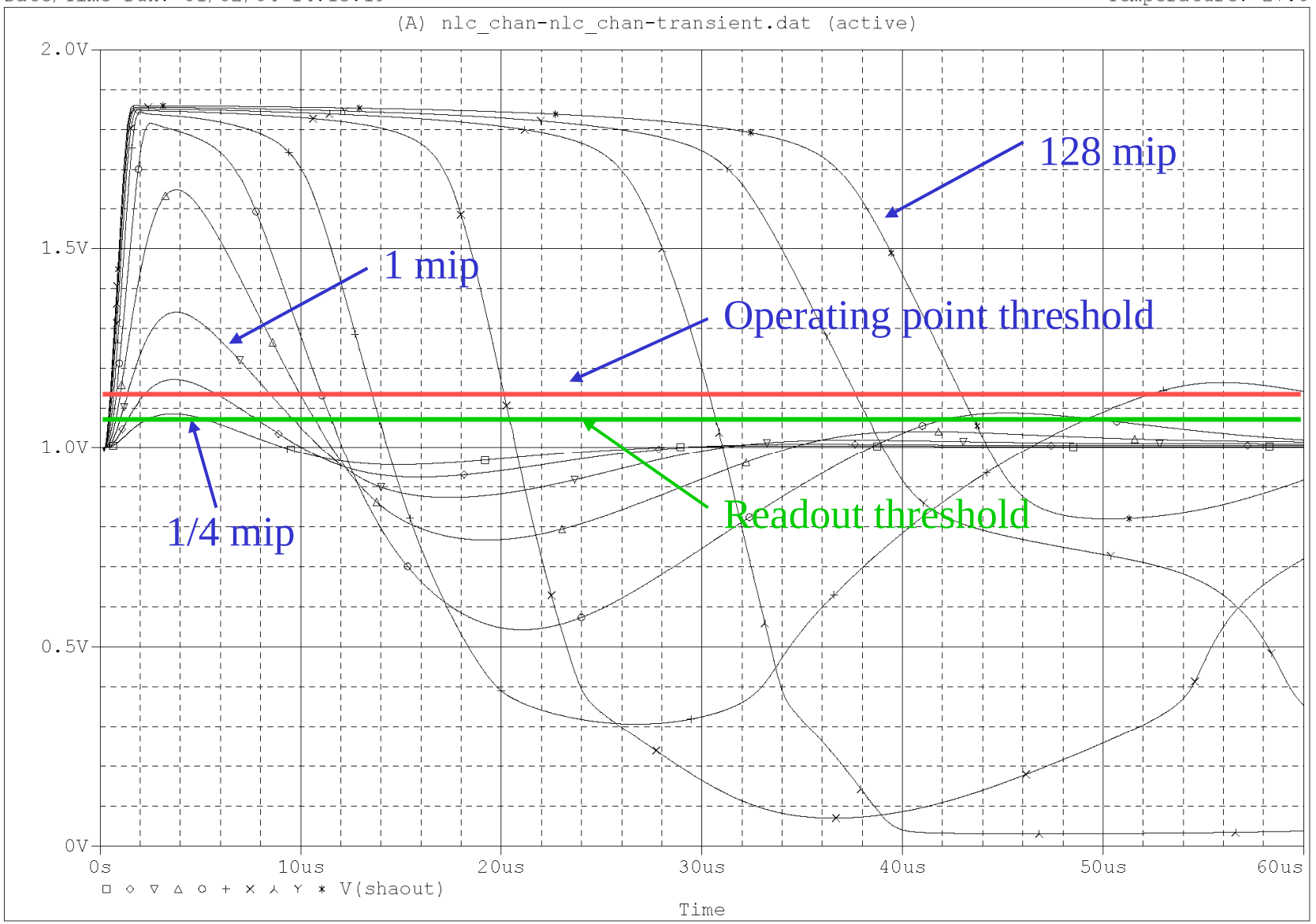
Redesigned relative to LSTFE-1 to accommodate long pulse train and exploit more relaxed (5 Hz) duty cycle.

Submitted to TSMC 0.25μm mixed-signal RF process; received August 11 (5 weeks late)

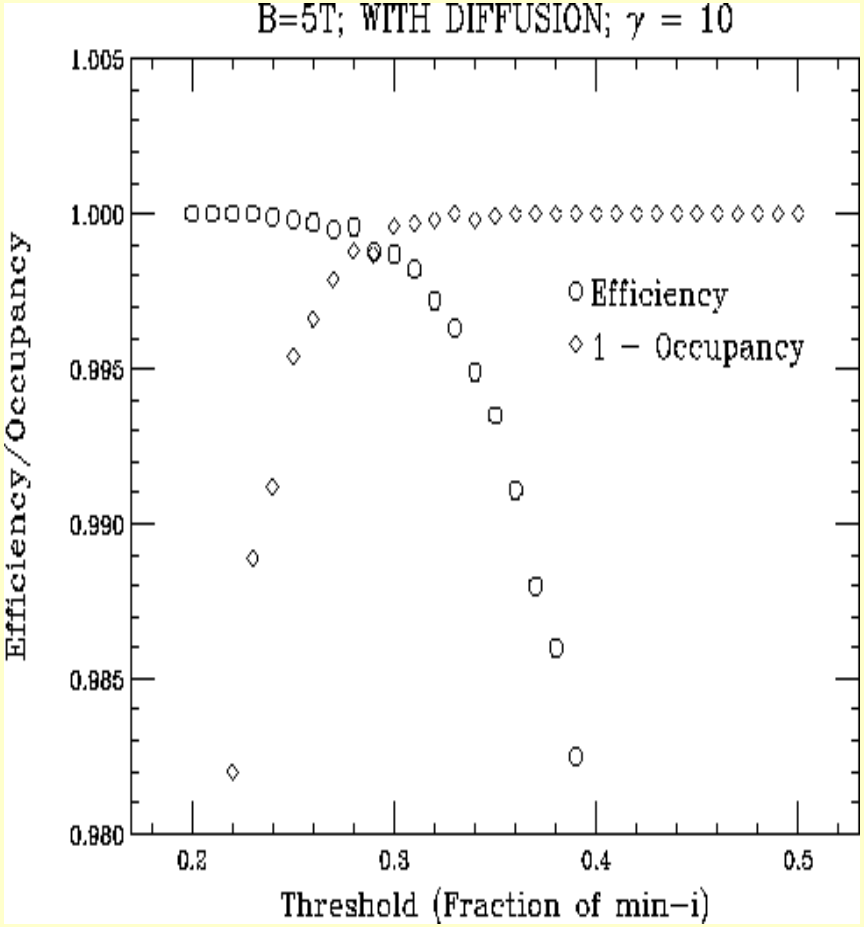
# SILICON TRACKER FRONT-END ARCHITECTURE

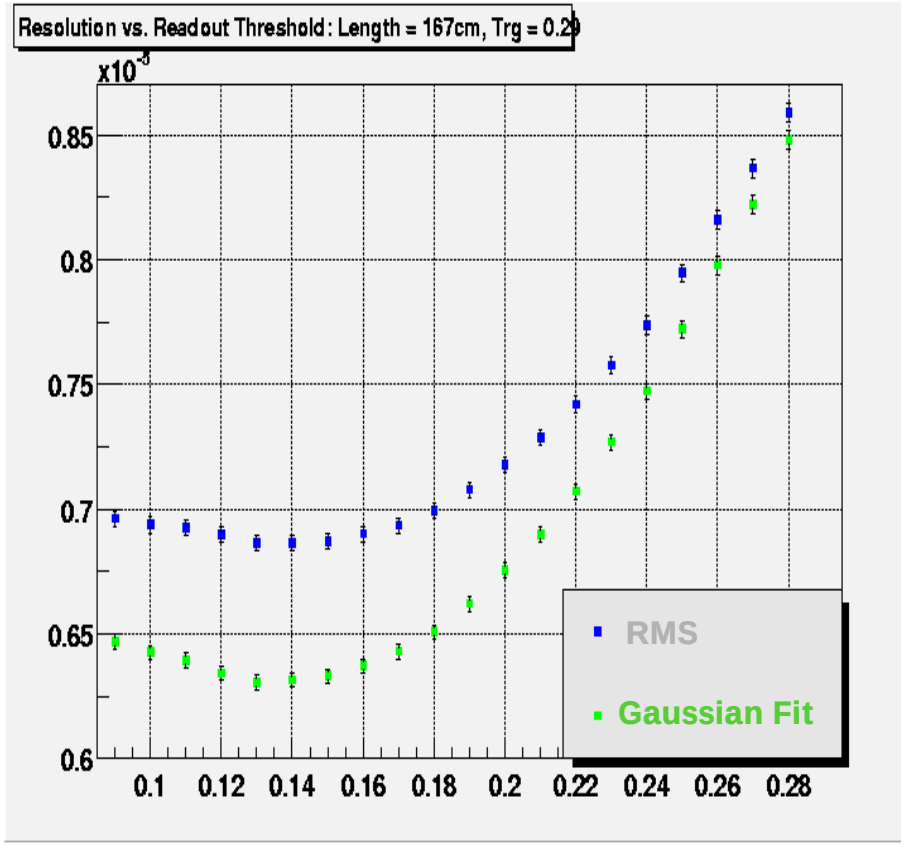
3 μs shaping time; analog readout it Time-Over-Threshold with 400 nsec clock




** Profile: "nlc_chan-transient" [ C:\Projects\NLC\preampTSMCmodels\nlc_chan-nlc_chan-transient.sim ]
Date/Time run: 01/02/04 14:15:19
Temperature: 27.0
(A) nlc_chan-nlc_chan-transient.dat (active)
2.0V
1.5V
1.0V
0.5V
0V
0s
10us
20us
30us
40us
50us
60us
128 mip
1 mip
Operating point threshold
Readout threshold
1/4 mip
V(shaout)
Time
Date: January 02, 2004
Page 1
Time: 14:18:43

# SIMULATED PERFORMANCE FOR 167cm LADDER

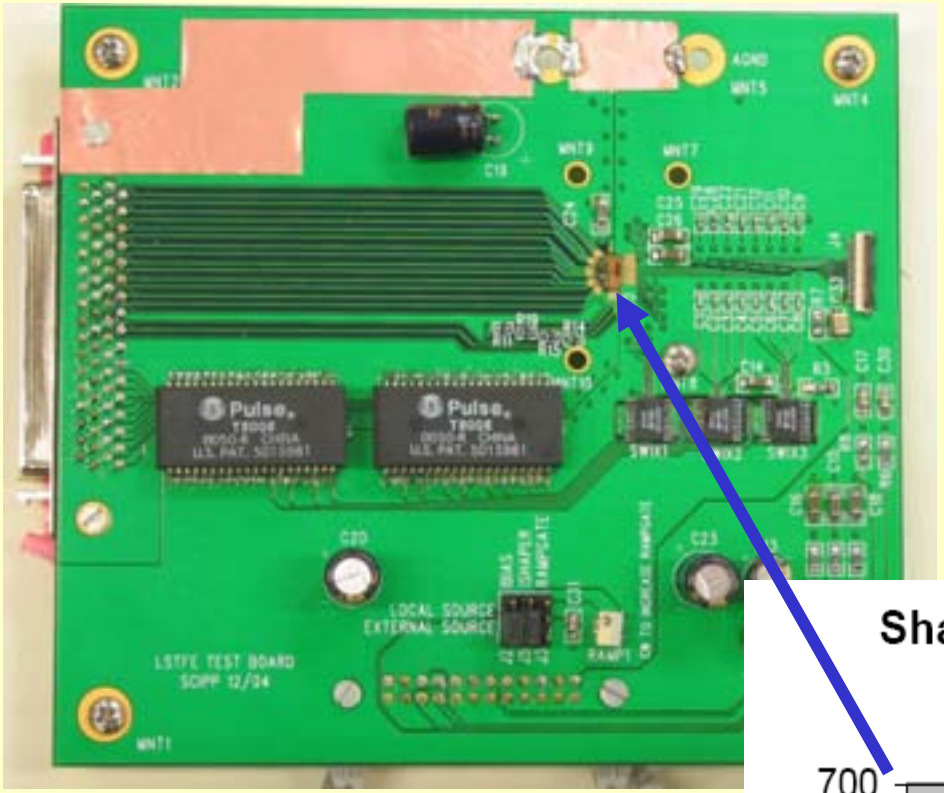


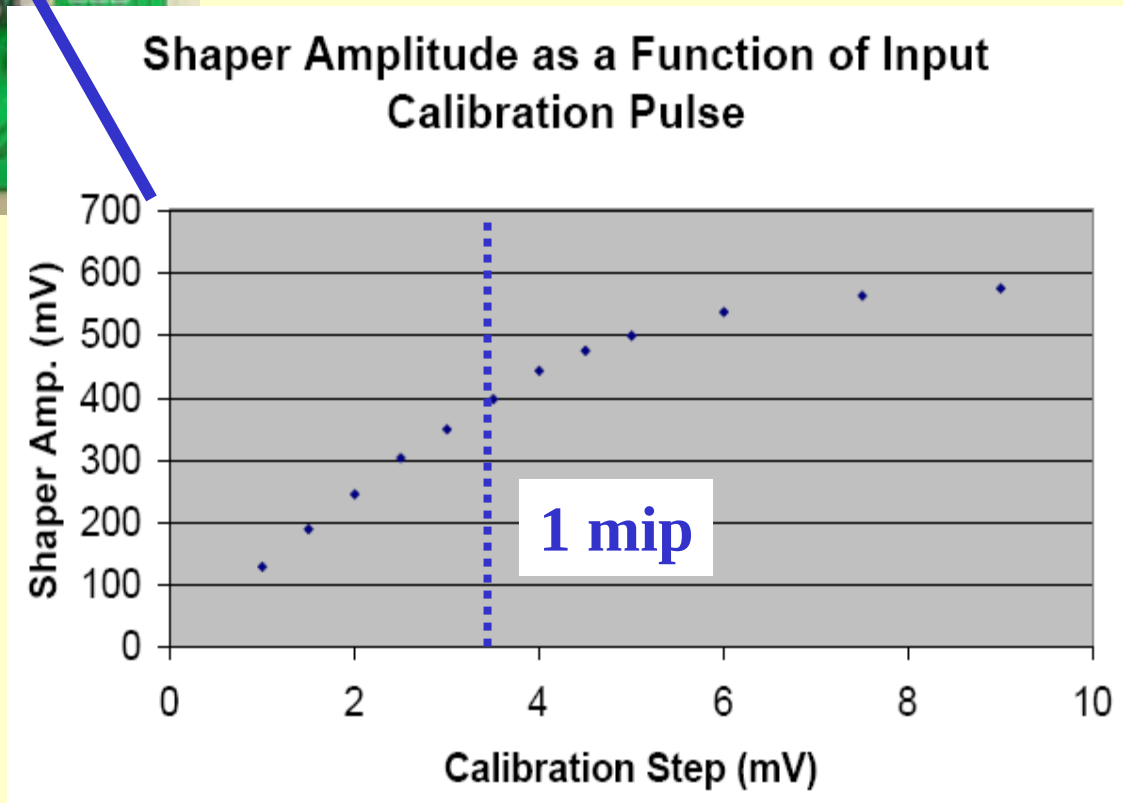

Efficiency and Occupancy as a function of high threshold

Resolution as a function of low threshold

# INITIAL RESULTS

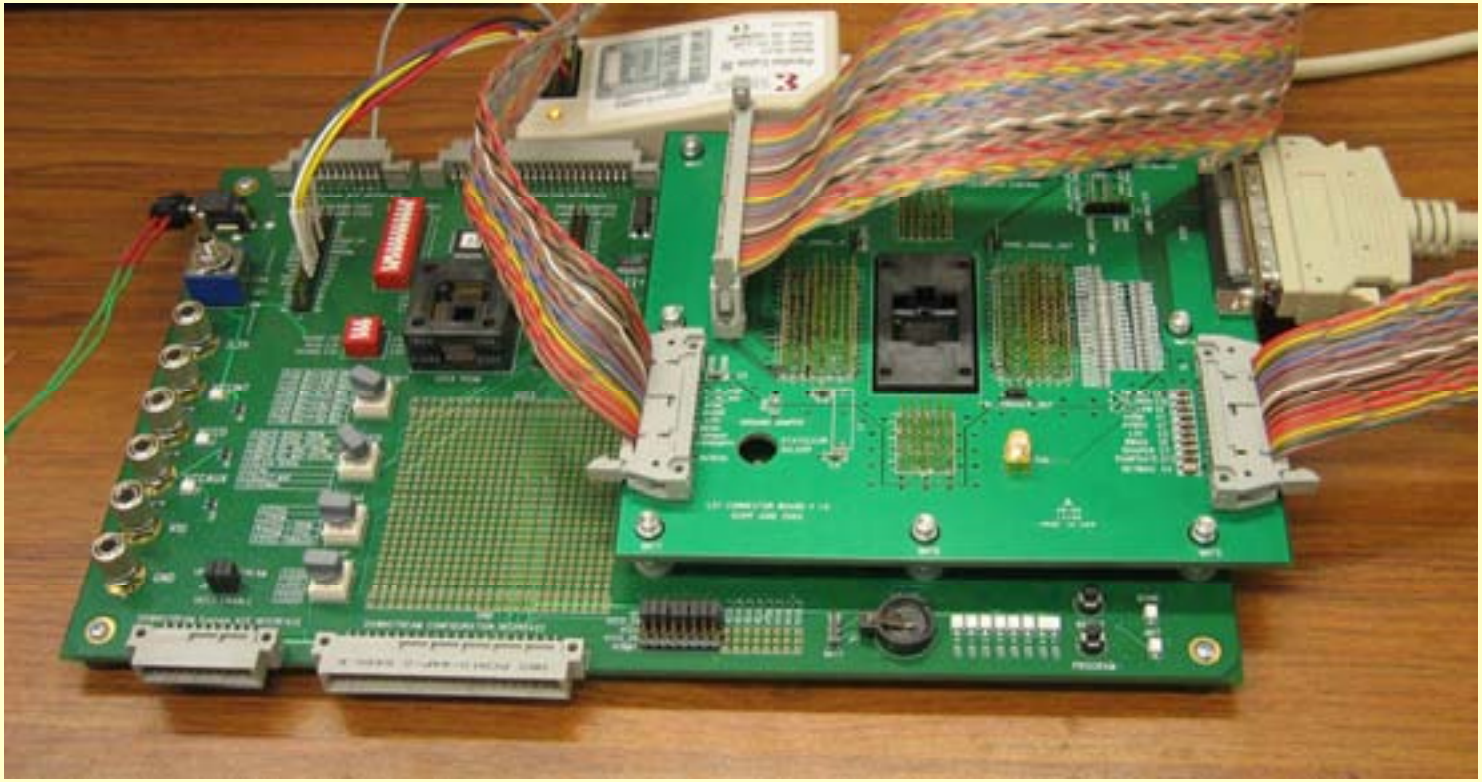


Expected analog gain of 140 mV/fC confirmed




Transition to log-arithmic response (TOT) at ~ 1.5 mip

# DIGITAL ARCHITECTURE: FPGA DEVELOPMENT

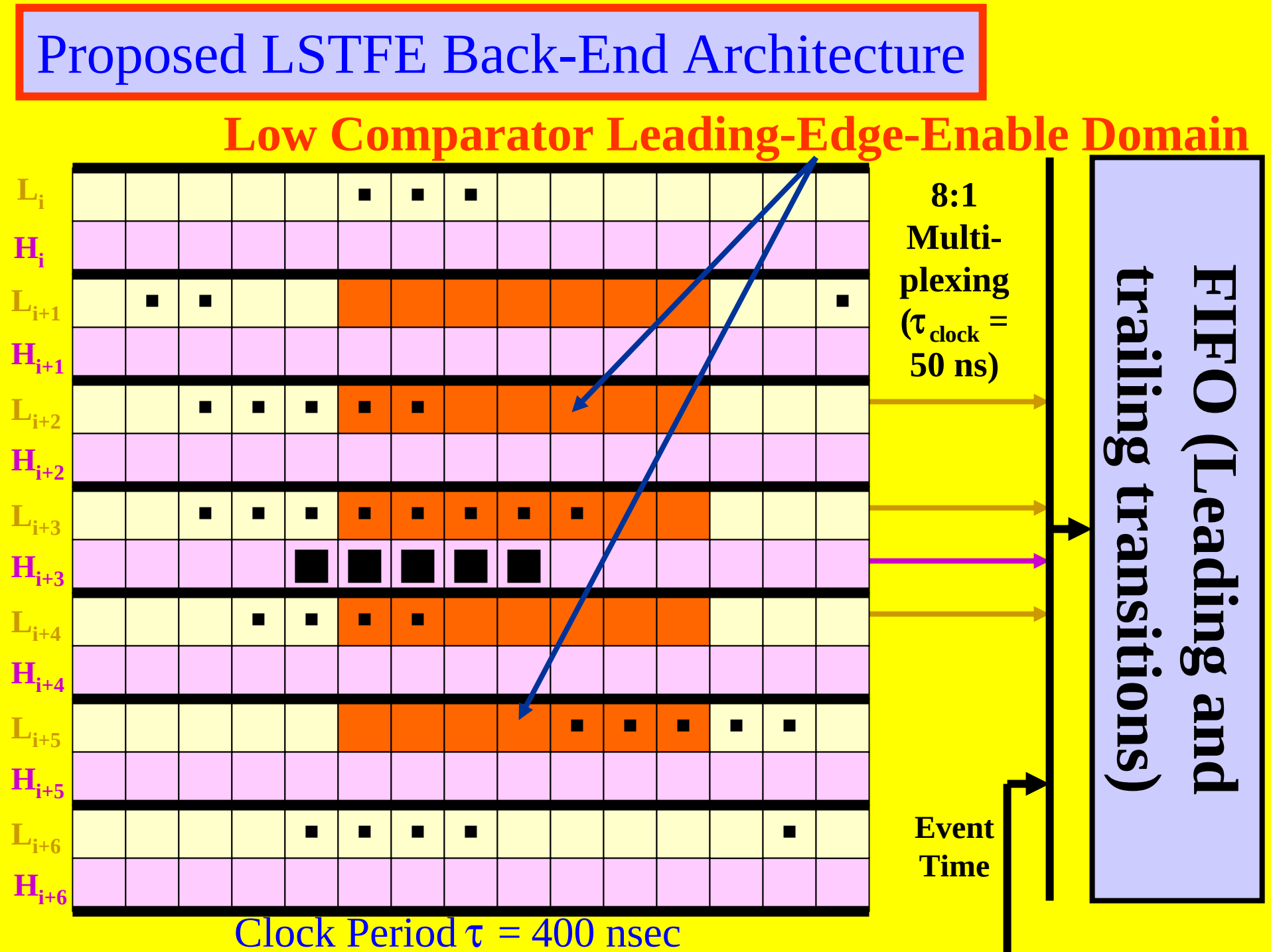


Digital logic should perform basic zero suppression (intrinsic data rate for entire tracker would be approximately 50 GHz), but must retain nearest-neighbor information for accurate centroid.

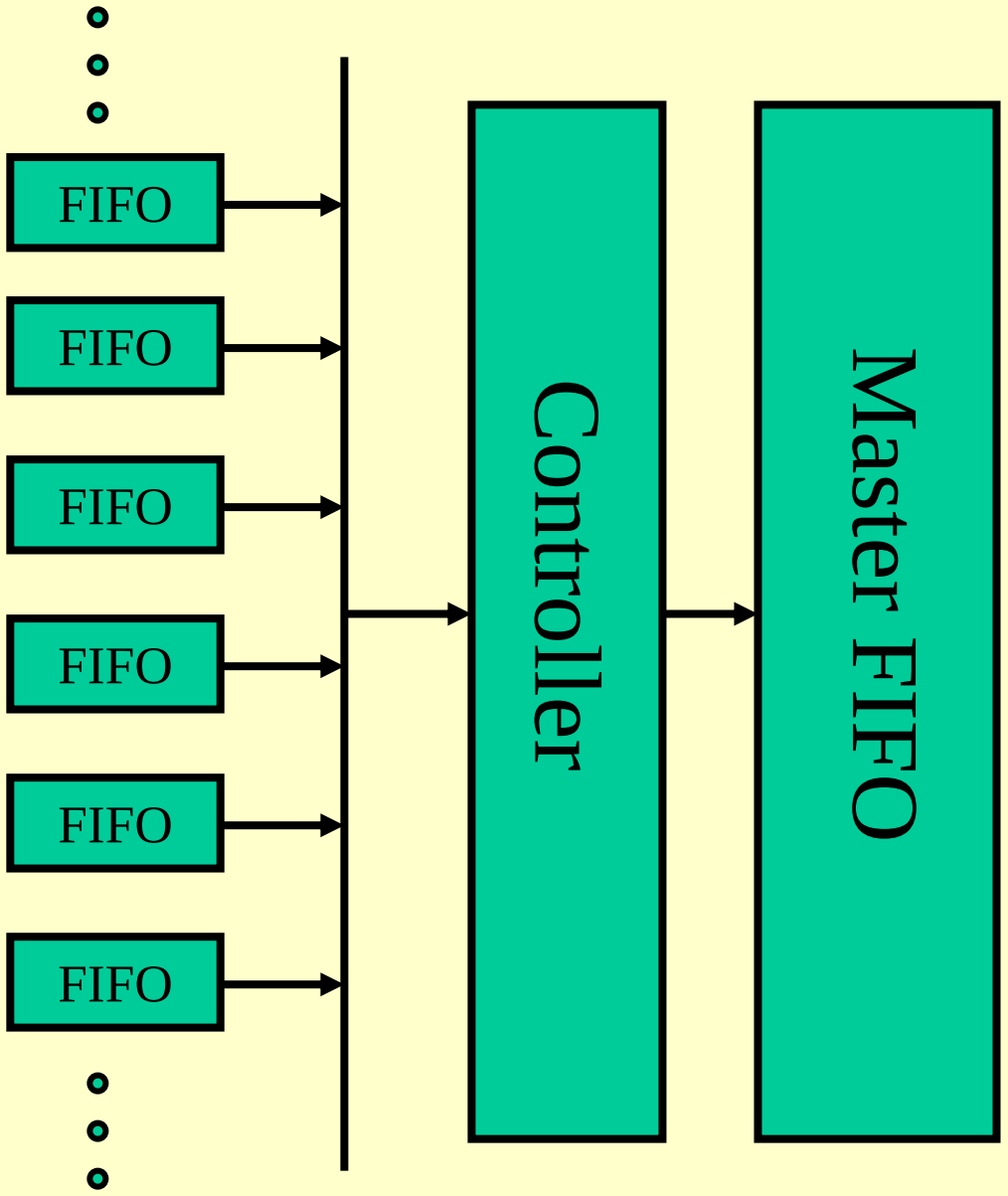
# Status of Back-End Architecture Development

- First-pass digital strategy worked out
- FPGA code developed for 8-channel system
- Simulated data stream (including noise and detector background) injected and processed in simulation
- Data rates estimated

# Proposed LSTFE Back-End Architecture



# Proposed LSTFE Back-End Architecture (cont'd)



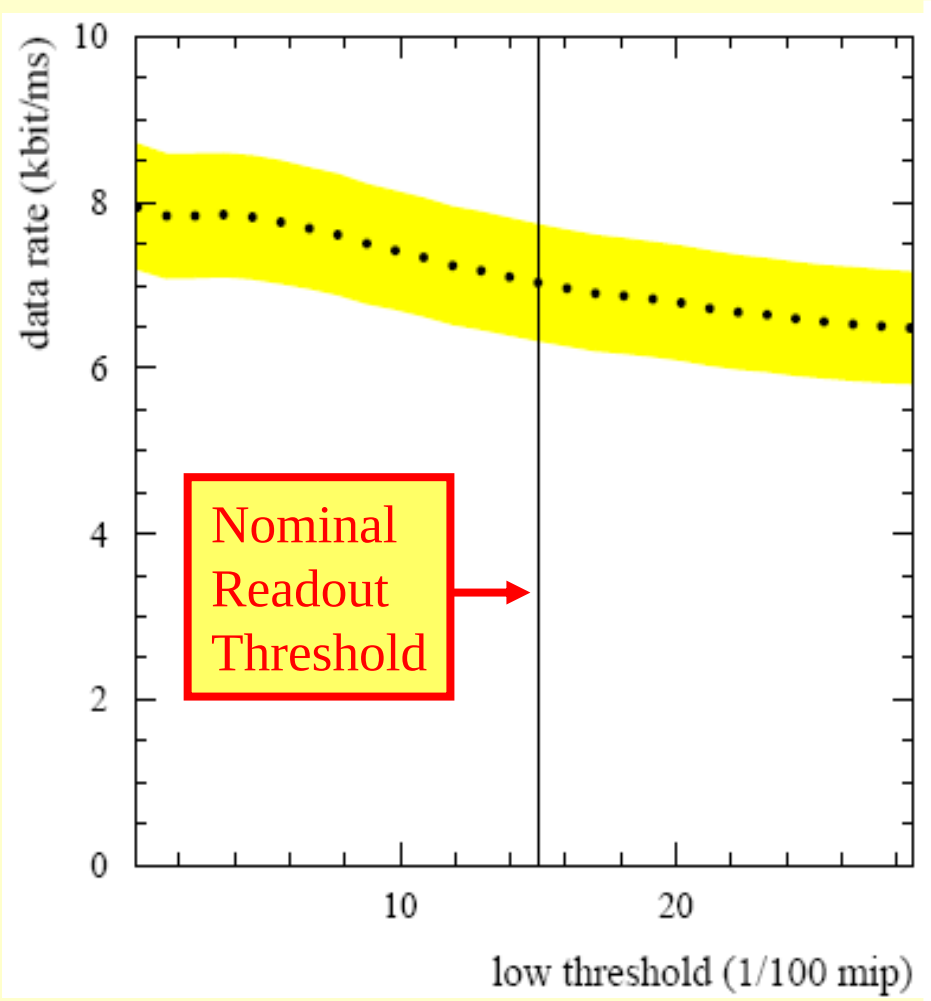

**Per 128 Channel Chip:**

**1 Master FIFO reads out 32 local FIFO's**

**Store in Master FIFO essentially complete by end of ~1ms beam spill**

# DIGITAL ARCHITECTURE VERIFICATION

ModelSim package permits realistic simulation of FPGA code (for now, up to signal propagation delay)

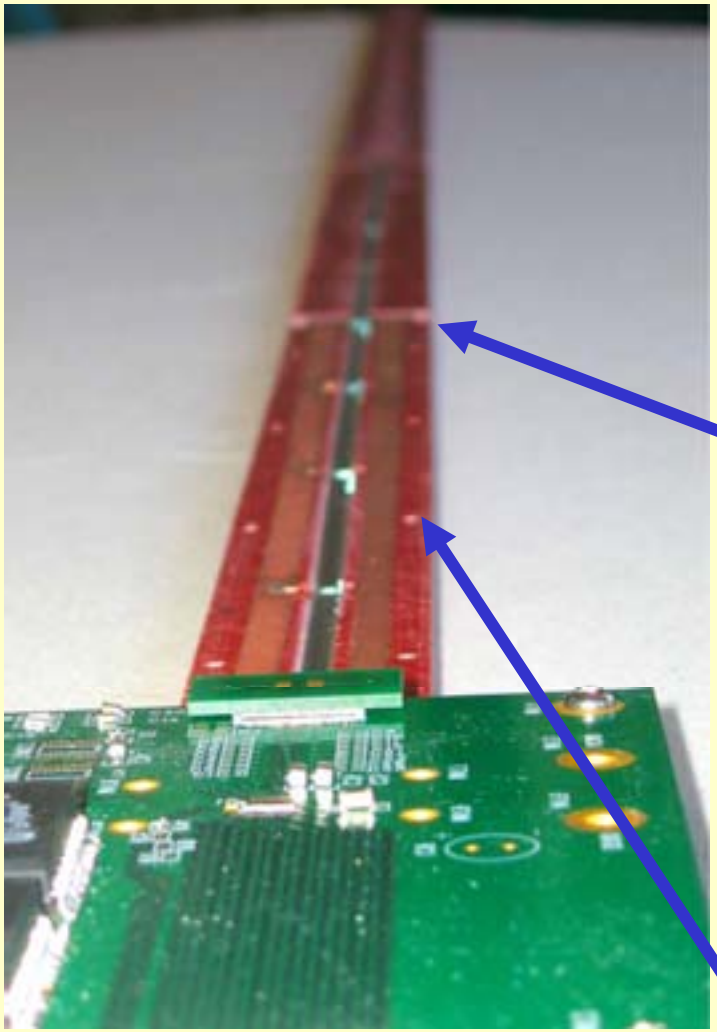


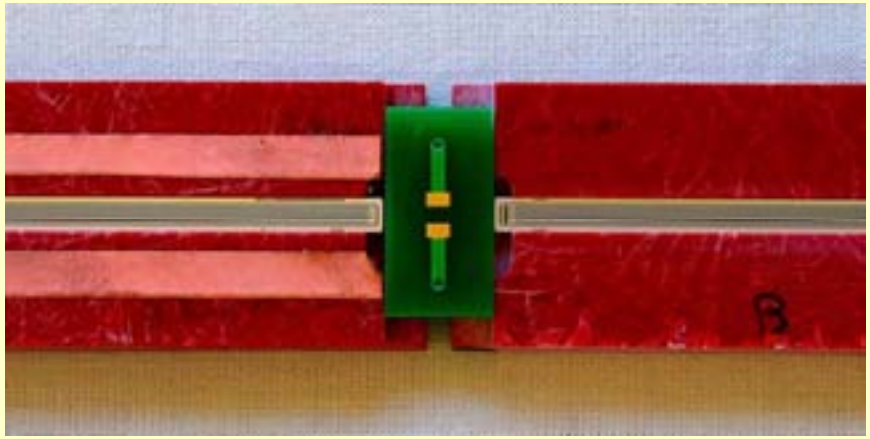

Simulate detector background and noise rates for 500 GeV running, as a function of read-out threshold.

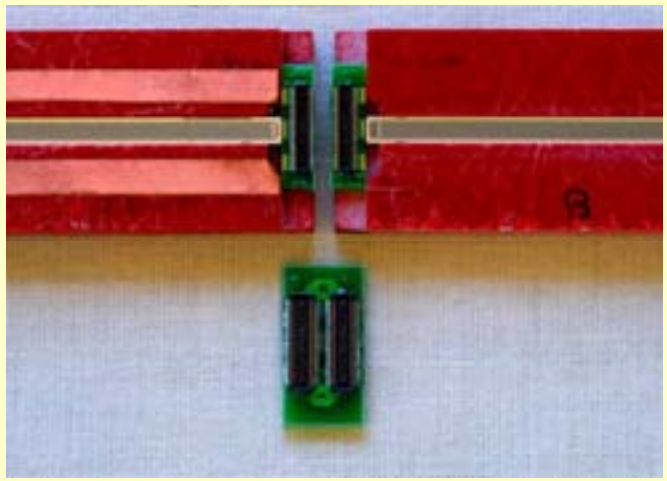
Per 128 channel chip ~ 7 kbit per spill ➔ 35 kbit/second

For entire long shaping-time tracker ~ 0.5 GHz data rate (x100 data rate suppression)

# LONG LADDER CONSTRUCTION







# SUMMARY

Progress on key fronts:

- Front-end electronics development
  LSTFE-2 chip (cold-rf optimization) designed and testing underway
- Digital architecture
  Proposed back-end architecture developed and verified; raw data rates acceptable (0.5 GHz)
- Ladder construction underway

Substantial work remains in all these areas; working towards testbeam run in late 2006