PROPOSAL AND REQUIEMENTS FOR PICOSECOND RESOLUTION MEASUREMENT DETECTOR IN A SYNCHRONOUS DETECTOR

CDF IS TAKEN AS AN EXAMPLE :

TIME BETWEEN COLLISONS =396NS

CHARGED PARTICLES PER COLLISION = APPROX 25

OVERALL SIZE OF DETECTOR ---A CYLINDER 1.5 METER RADIUS AND 3 METER LONG

SIZE OF PROPOSED DETECTOR TILE = 5 INCHES SQUARE

We require one set of input / output bus lines per 5cm of circumference which results in 189 lines for a 1.5 meter radius cylinder. The cylinder is 3 meters long which means we will have 60 modules per line. Each module covers 5cm square. The total number of 4 cell modules is then 11,340. There will be about 1 event every five collisions in each line of modules assuming 40 charge particles collision

Data generated for each cell per event is about 5 bytes .

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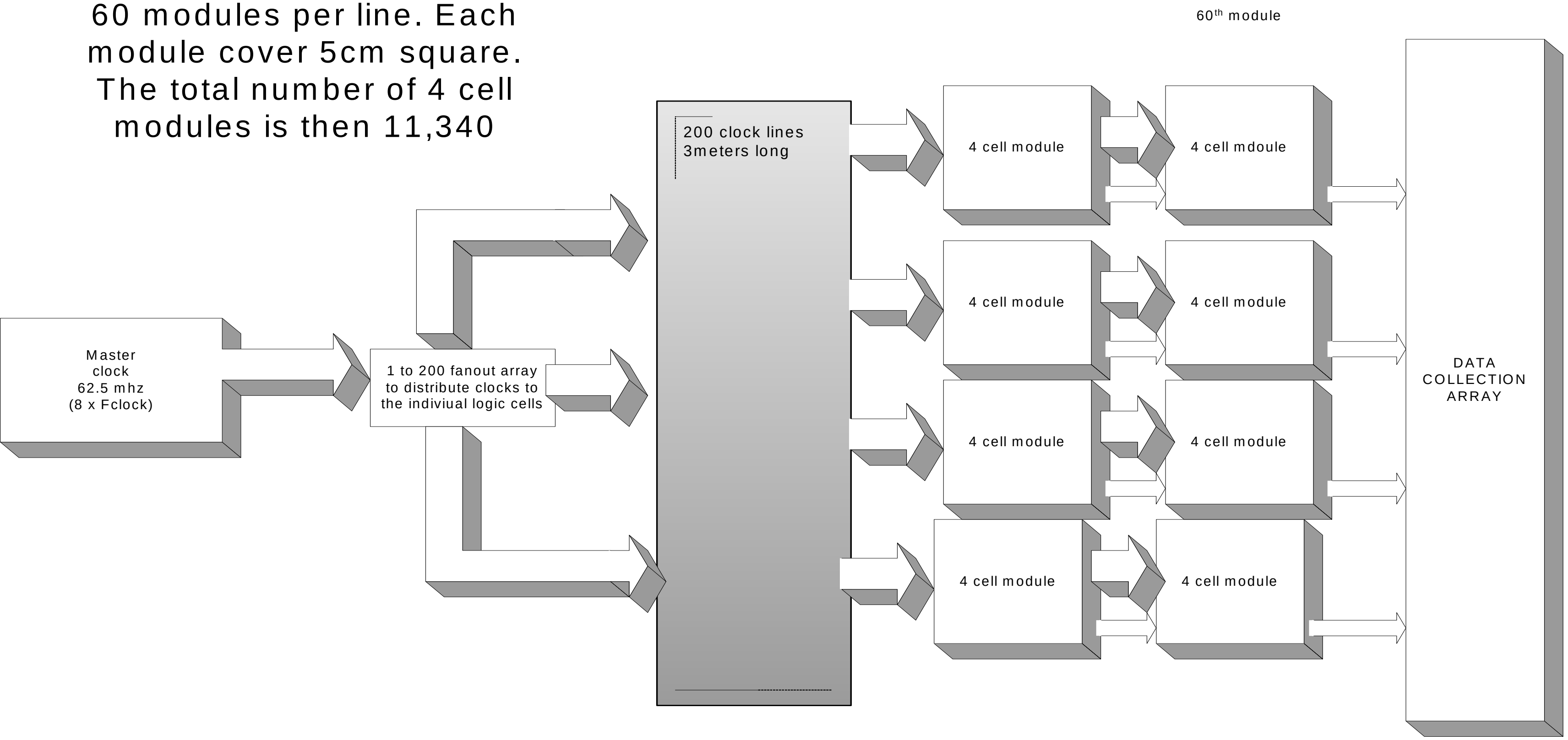
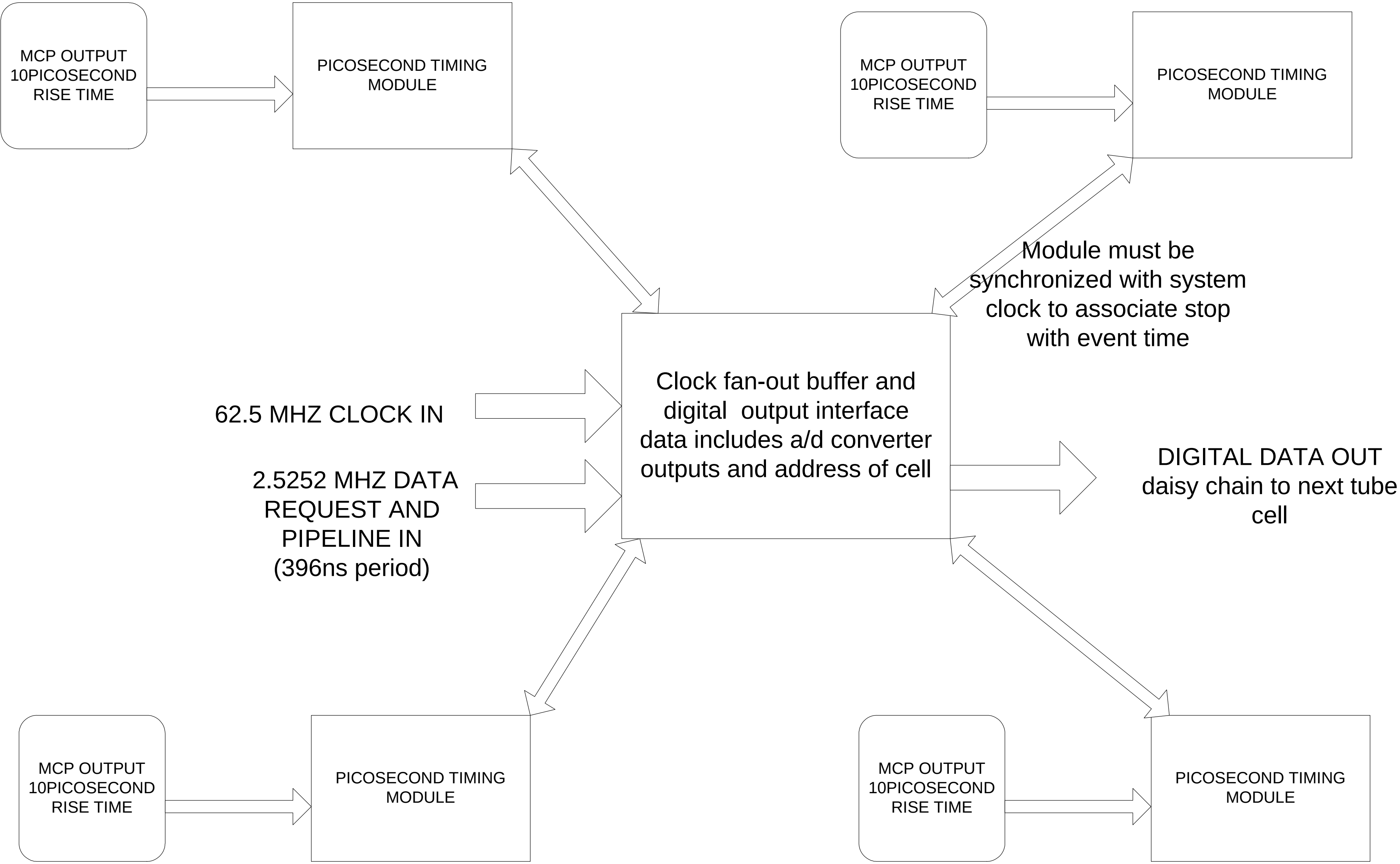
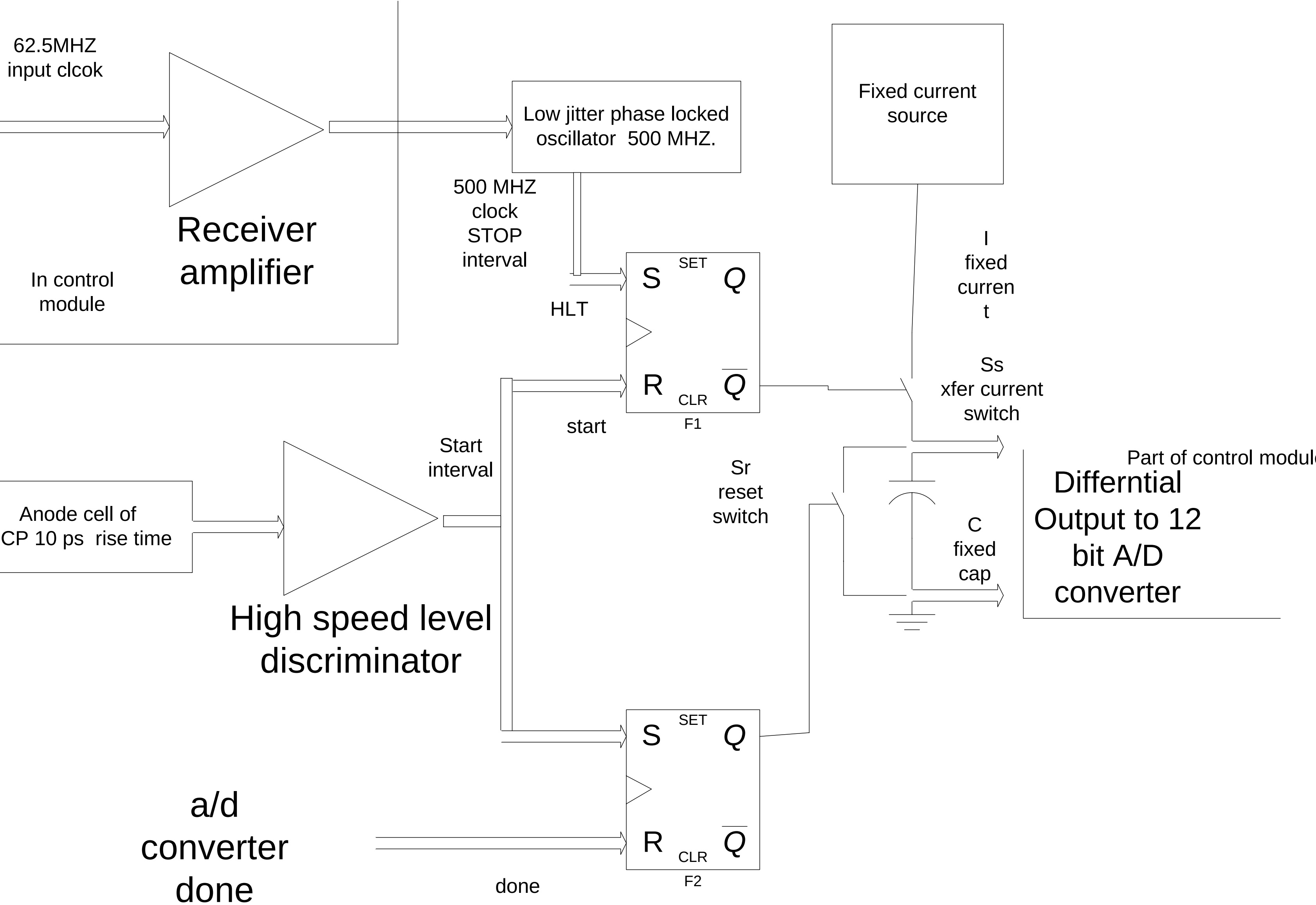


PICO-SECOND TOP BLOCK

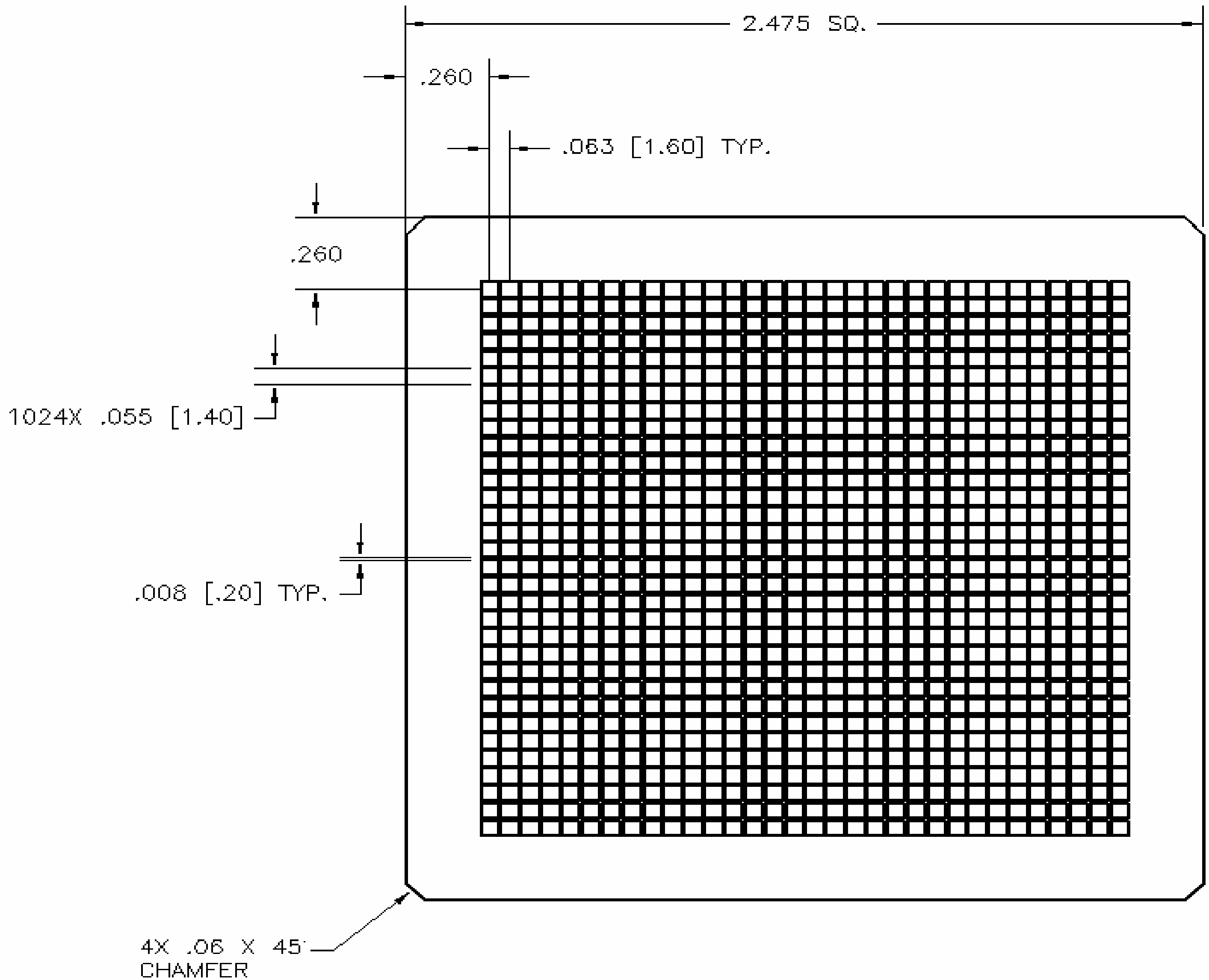


4 CELL PICO-SECOND TIMING MODULE

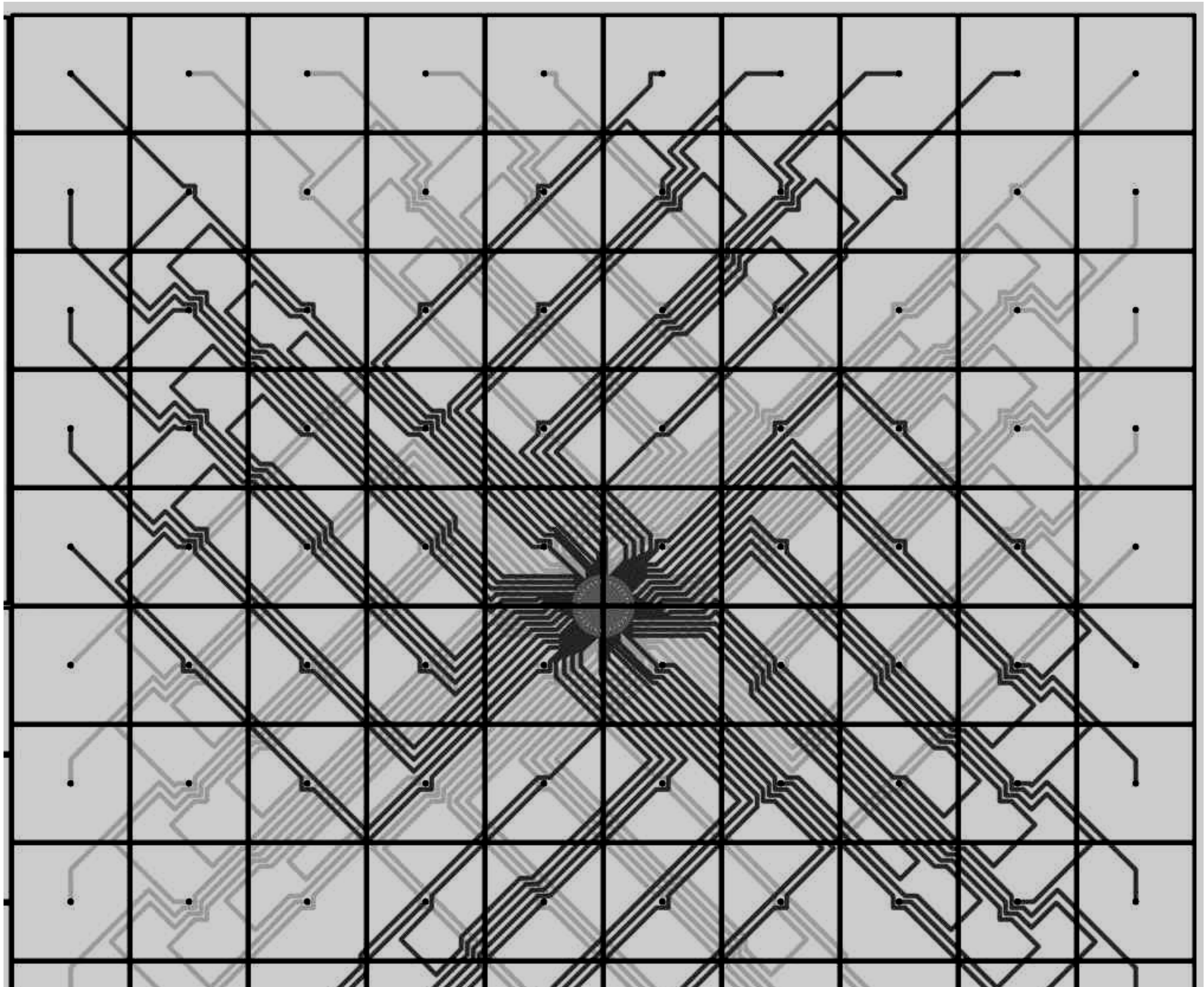


Simplified cell logic
1 0f 4 cells served by control module

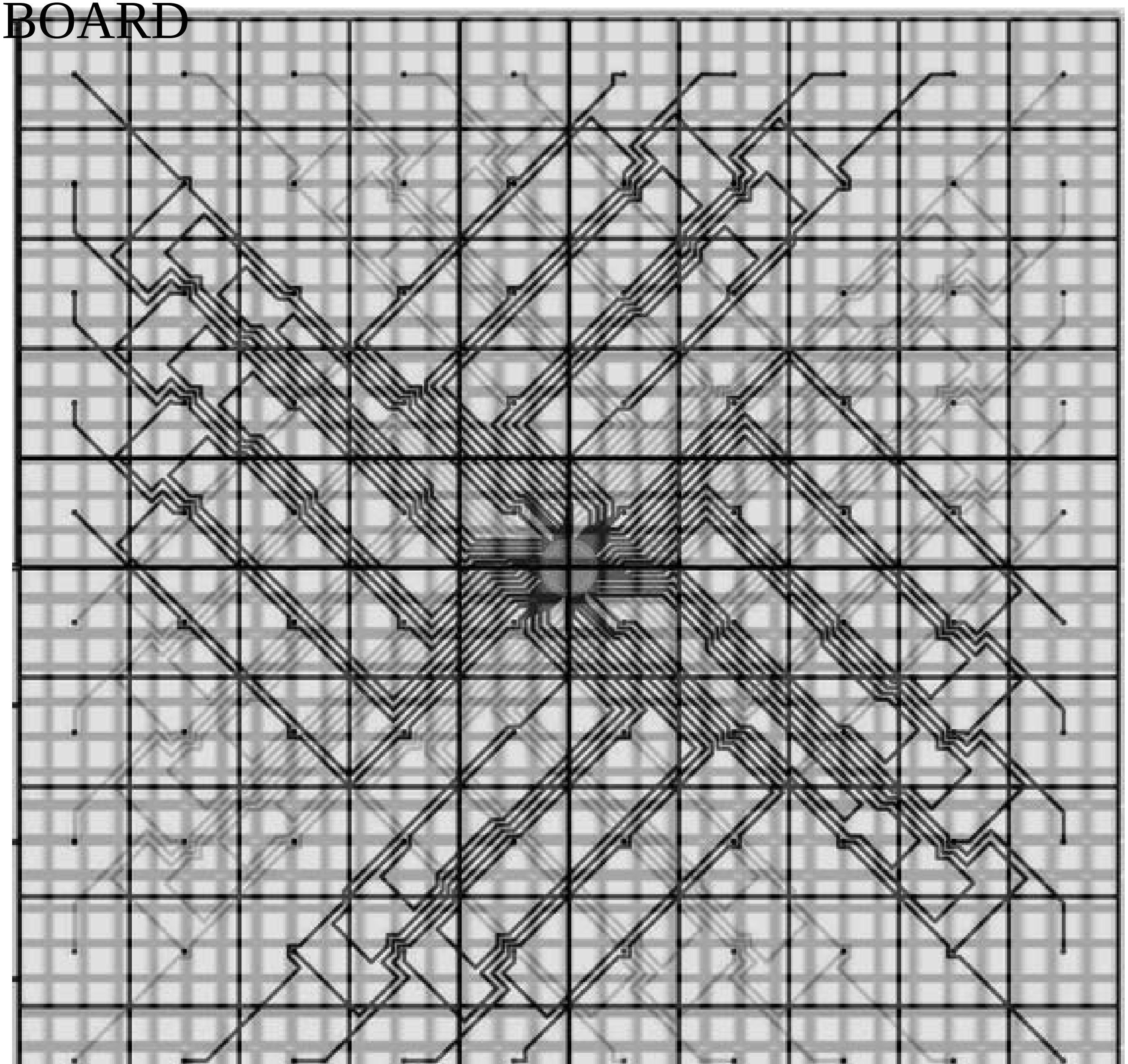
MCPT ANODE
1024 APERTURE ARRAY SHOWN



U OF C 100 SOURCE EQUAL TIME COLLECTOR BOARD

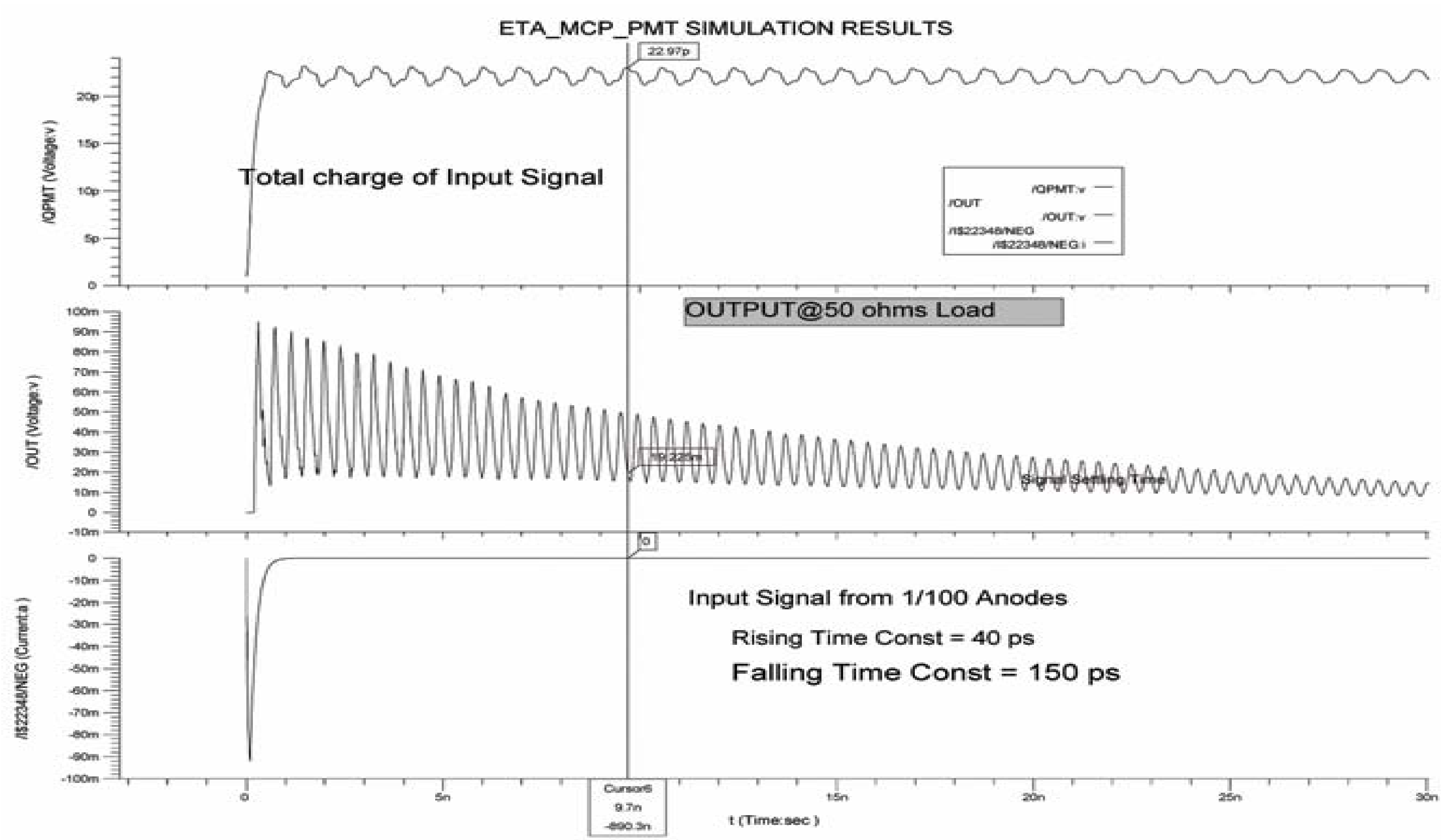


OVERLAY OF 1024 ANODE AND U OF C BOARD

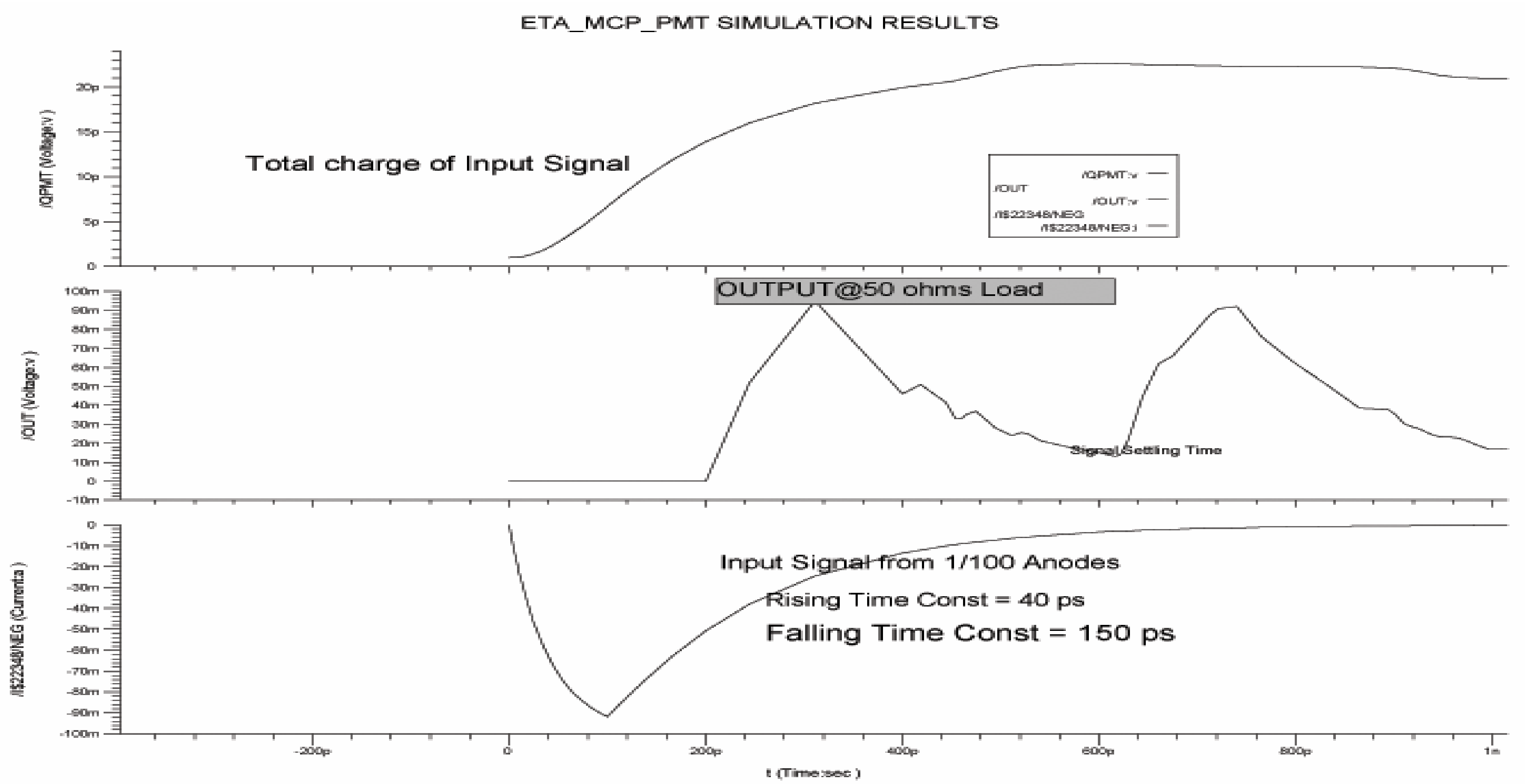


HSPICE SIMULATION OF 100 INPUT CELL ARRAY

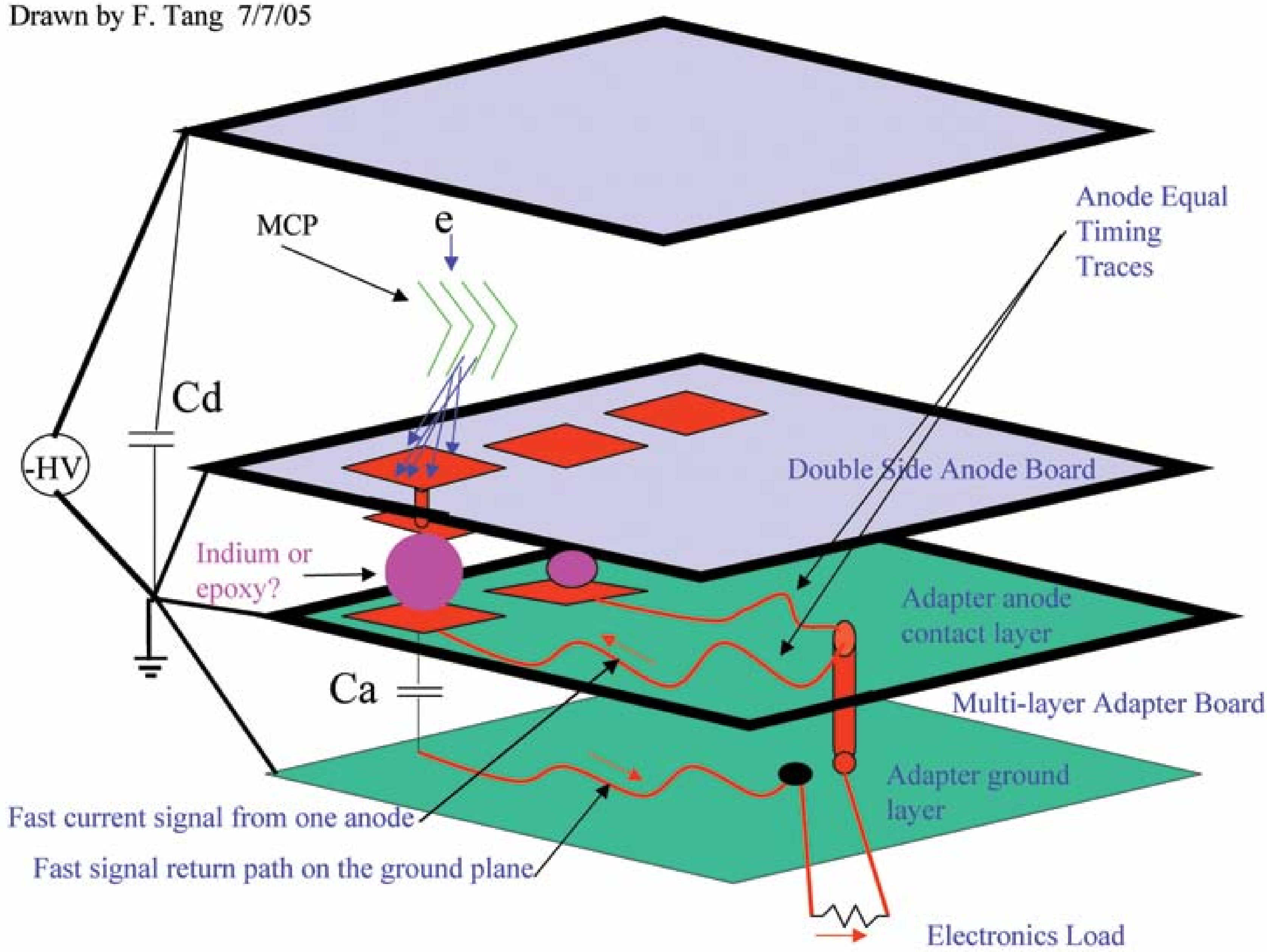
1 OUTPUT 30ns WINDOW



Simulation of array 1ns window

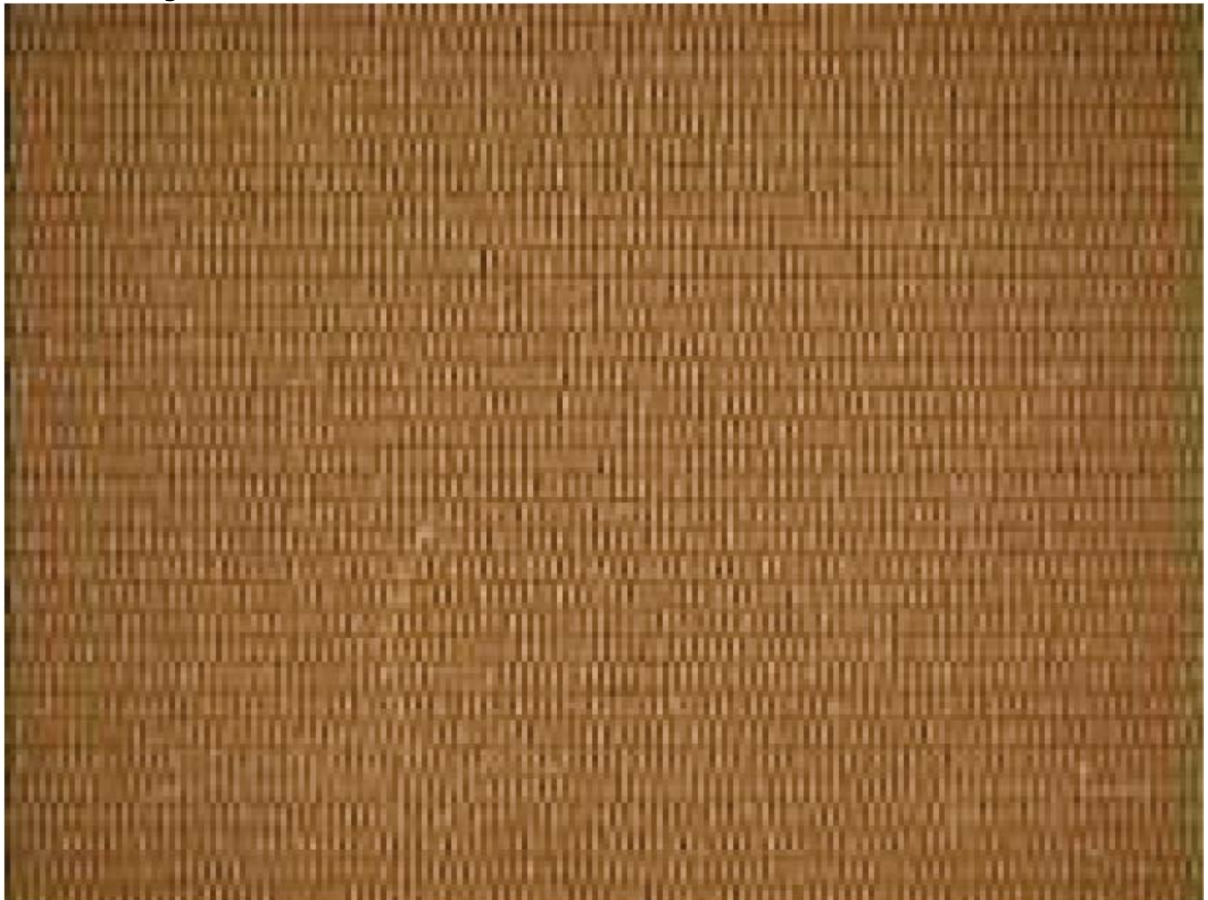


SKETCH TO SHOW PLAN TO ASSEMBLE COLLECTION ARRAY TO MCPT



TYCO ELECTRONICS ELASTOMETER TECHNOLOGY

Since the MCPT is sealed with indium solder we cannot use regular lead tin solder to connect with an external circuit board. We are planning to use either a conductive epoxy or an elastometer layer to sandwich the circuit board to the tube. The substance below is a layer of silicone with conductive wire arrayed and embedded in the silicone insulator



IBM SIGE PROCESSES AVAILABLE THROUGH MOSIS

BiCMOS

Key technology specifications

	5HP|AM|DM	5PA	5HPE	6HP	7HP	7WL
Isolation:	STI/DT	STI/DT	STI	STI/DT	STI/DT	STI/DT
HP fT/fMAX (GHz):	51.5	51.5/65	43/45	47/65	120/100	60/85
HB fT/fMAX (GHz):	29/50	23/50	19/35	27/50	30/50	45/73
HP BVceo (V):	3.3	3.3	3.3	3.3	1.8	3.3
HB BVceo (V):	5.5	7	9.6	5.7	4.2	6.0
Min. WE Drawn (μm):	0.5	0.5	0.32	0.32	0.2	0.24
CMOS generation	5S0	5S0	5SF	6SF	7SF	7SF
CMOS Lg drawn (μm):	0.5	0.5	0.4	0.25	0.18	0.18
CMOS supply (V):	3.3	3.3	5.0,3.3	2.5,3.3	1.8,3.3	1.8,3.3
BEOL metal type:	Al	Al	Al	Al	Cu+Al	Cu+Al
M1 current density:	1×	1×	1.16×	0.89×	1.24×	1.24×
Masks FEOL/BEOL:	24/8	24/8	18/7	22/7	22/9	15/7
RPT (days) **3LM:**	24.8	24.8	17.7	23.9	25	15.1

WHY SIGE PROCESS?

PUBLISHED PAPERS FROM AN IBM DESIGN GROUP ON USING EARLIER VERSIONS OF THIS PROCESS (5HP) REPORTING PLL OSCILLATORS WITH SUB PICO SECOND JITTER (IBM J RES&DEV VOL 47 NO2/3 MARCH/MAY 2003 SiGe BiCMOS INTEGRATED CICUITS FOR HIGH-SPEED SERIAL COMMUNICATIN LINKS)

OUR TOOLS, PLANS AND PROBLEMS

TOOLS INCLUDE CADENCE AND MENTOR GRAPHICS DESIGN TOOLS, IBM DESIGN KIT FOR SiGe PROCESS.

HELP FILES FROM IBM, CONTRACT WITH MOSIS TO ENABLE FABRICATION.

WHAT WE MUST DO. WE NEED 2 DIFFERENT CHIPS

DESIGN CHIPS

SIMULATE DESIGN

DESIGN BOARD

ASSEMBLE A SUITABLE TEST FACILITY

DESIGN DATA ACQUISTION FOR TESTING

BUY CHIP SAMPLE LOT (EXPENSIVE $70K)

TEST CHIPS