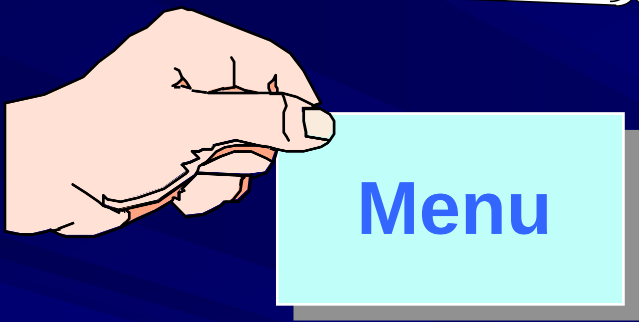
ILC Trigger & DAQ issues



By P. Le Dû

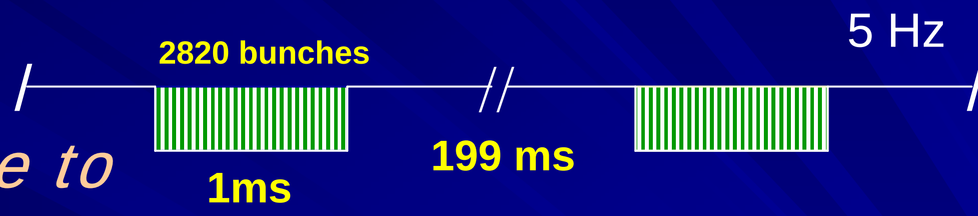
pledu@cea.fr

- Summary of present thinking
- SoftwareTrigger concept
- Data collection architecture model
- Technology forecast
- Snowmass program

ALPG_Snowmass05

Conditions

2004 International decision: « cold » machine ‘ à la Tesla’



Machine parameters close to

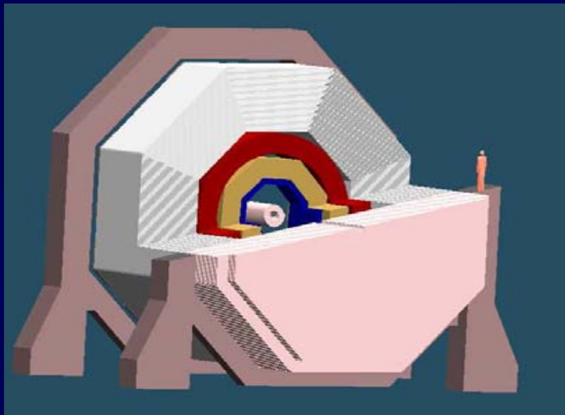
The LC is a pulsed machine

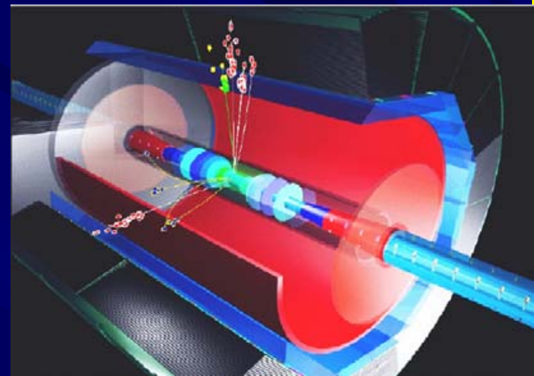
- 2 x 16 km superconducting Linear **independant** accelerators
- Max 2 interaction points
→ **2 detectors ???**
- Energy
  - nominale : 500 Gev
  - maximum : 1 Tev
- IP beam size ~ few μm
- L= 2. 10^{34} $cm^{-1}s^{-1}$

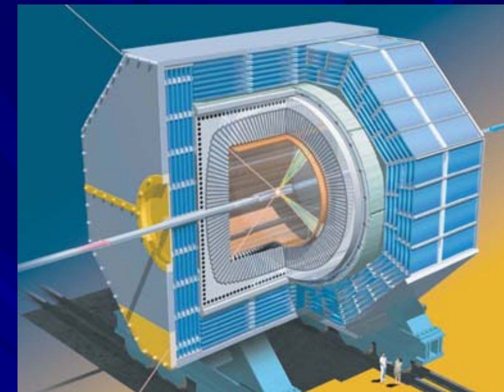
- repetitian rate 5
- bunches per train 2820 → **x 2 ?**
- bunch separation 337 ns →150ns
- train length 950 ns
- train separation 199 ms

-> long time between trains
(short between pulses)

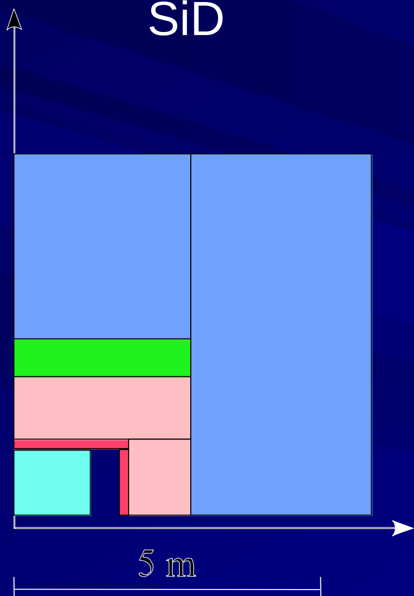
Detector concepts



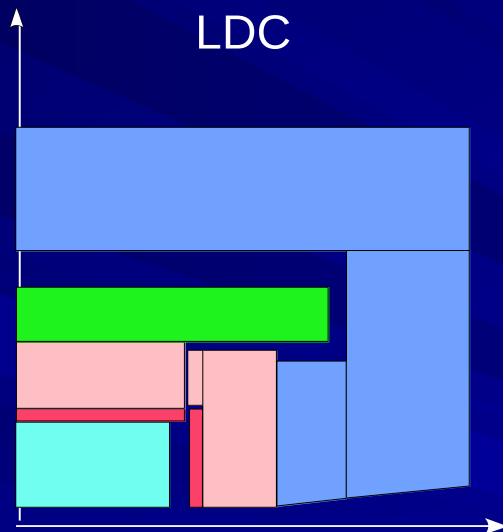




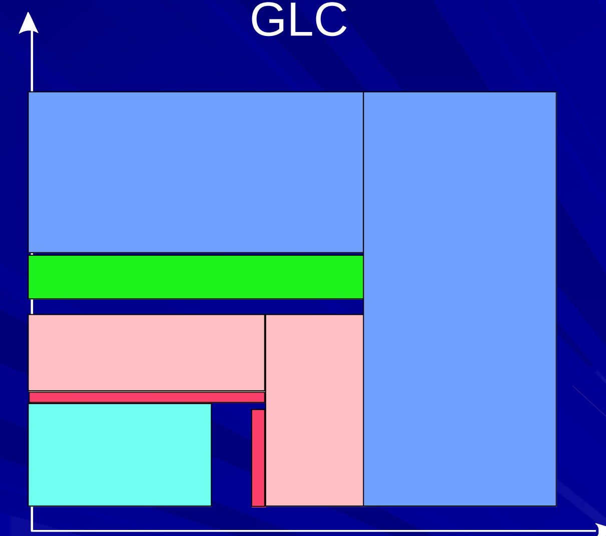
SiD



LDC



GLC



Main Tracker
EM Calorimeter
H Calorimeter
Cryostat
Iron Yoke

- Si Strips
- SiW EM
- 5 Teslas

- Large gaseous central tracking device (TPC)
- High granularity calorimeters
- High precision microvertex
- All inside 4T magnetic field

- Large Gazeous Tracker → TPC
- W/Scint EM calor.
- 3 Teslas solenoid

Evolution of basic parameters

Exp. *Year*	Collision rate	Channel count	L1A rate	Event building	Processing. Power	Sociology
UA's *1980*	3 μsec	-	-	-	5-10 MIPS	150-200
LEP *1989*	10-20 μsec	250 - 500K	-	10 Mbit/sec	100 MIPS	300-500
BaBar *1999*	4 ns	150K	2 KHz	400 Mbit/s	1000 MIPS	400
Tevatron *2002*	396 ns	~ 800 K	10 - 50 KHz	4-10 Gbit/sec	5.10^4 MIPS	500
LHC *2007*	25 ns	200 M*	100 KHz	20-500 Gbit/s	$>10^6$ MIPS	2000
ILC *2015 ?*	330 ns	900 M*	3 KHz	10 Gbit/s	$\sim 10^5$ MIPS	> 2000 ?

** including pixels*

Sub-Detector	LHC	ILC
Pixel	150 M	800 M
Microstrips	~ 10 M	~30 M
Fine grain trackers	~ 400 K	1,5 M
Calorimeters	200 K	max 30 M
Muon	~1 M	

Summary of present thinking

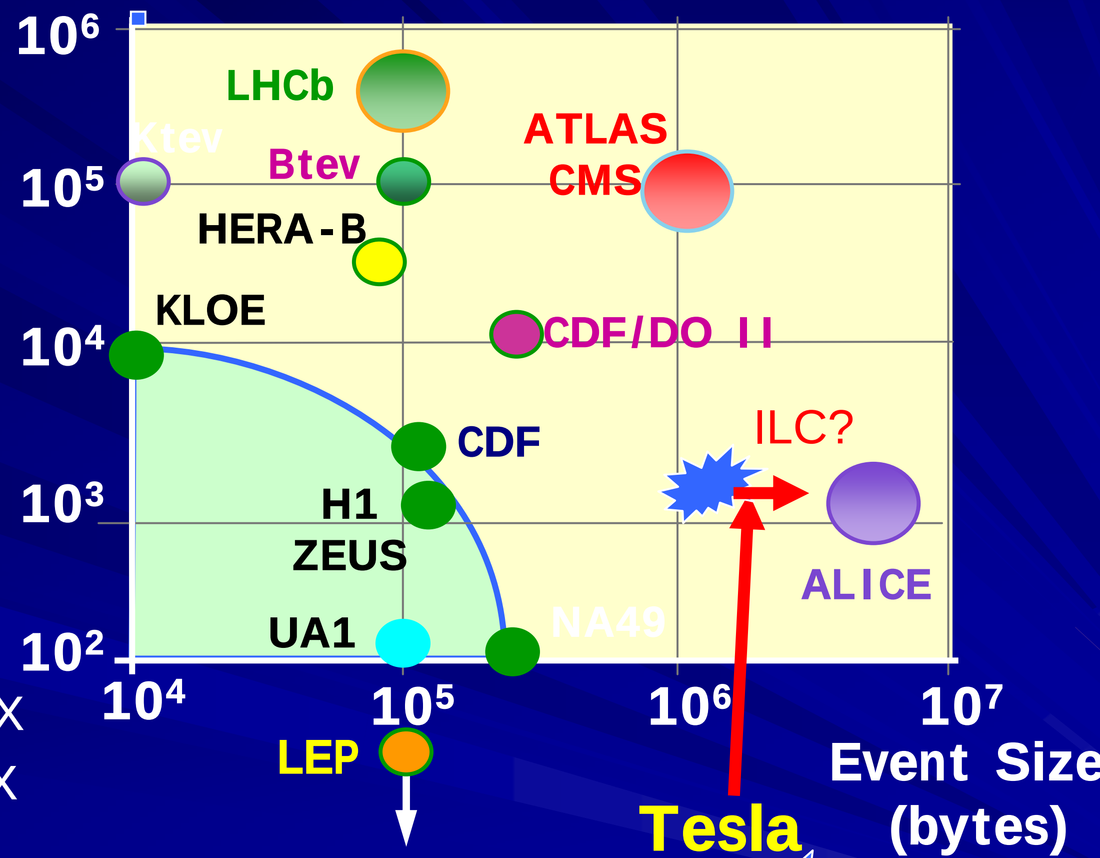
The ILC environment poses new challenges & opportunities which will need new technical advances in VFE and RO electronics → **NOT LEP/SLD, NOT LHC !**

- Basic scheme: The FEE integrates everything
  - →From signal processing & digitizer to the RO BUFFER …
- Very large number of channels to manage (Trakers & EM)
  - →should exploit power pulsing to cut power usage during interburst
- New System aspects (boundaries ..→ GDN !)
- Interface between detector and machine is fundamental
  - →optimize the luminosity → consequence on the DAQ
- Burst mode allows a fully software trigger !
  - →Looks like the Ultimate Trigger: Take EVERYTHING & sort later !

→ GREAT! A sociological simplification!

Rates and data volume from Tesla to ILC

High Level-1 Trigger (1 MHz)

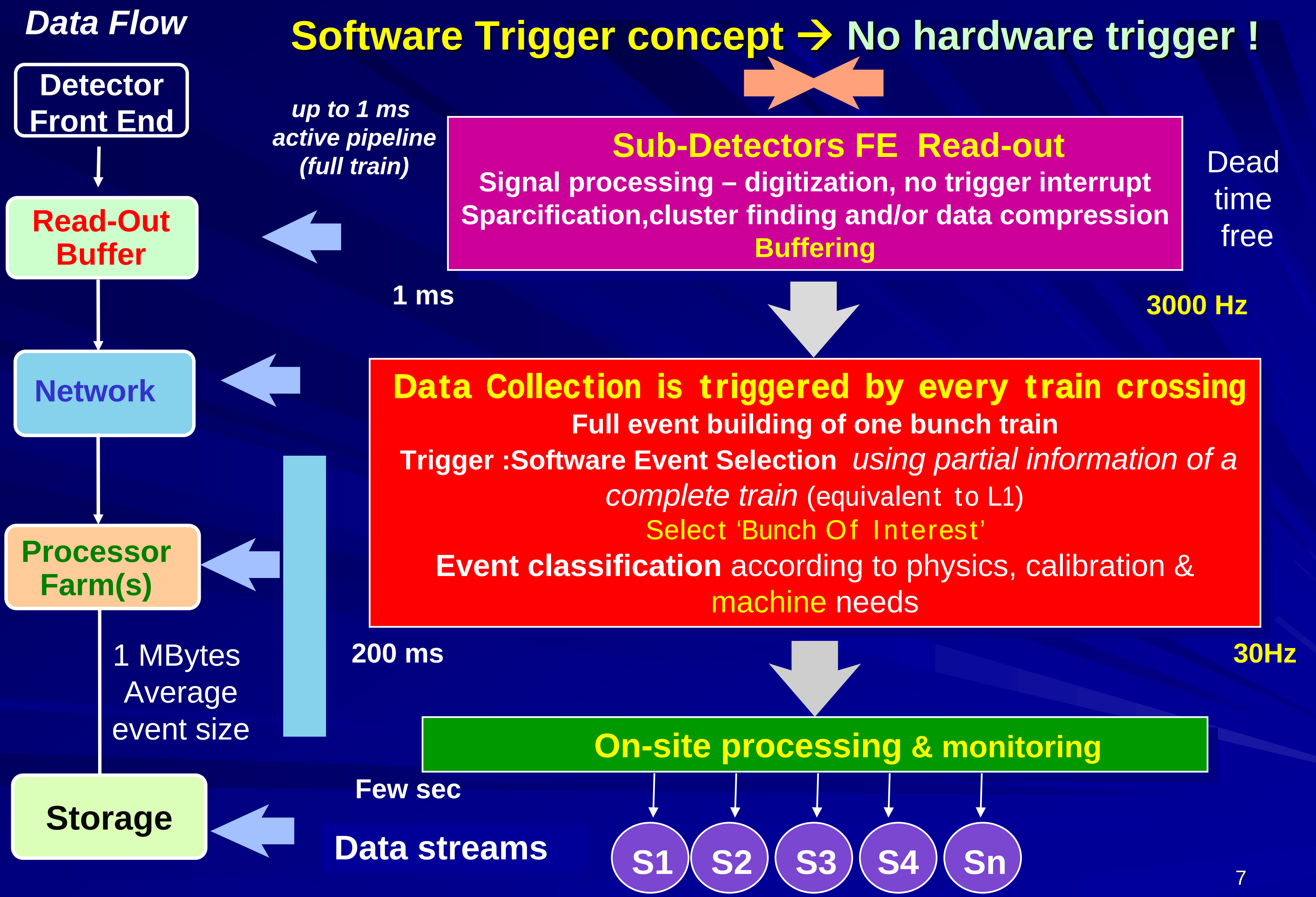


- *Physics Rate :*
  - e+ e- → X 0.0002/BX
  - e+ e- → e+ e- X 0.7/BX
- *e+ e- pair background :*
  - VXD inner layer 1000 hits/BX
  - TPC 15tracks/BX

→ ***Background is dominating the rates !***

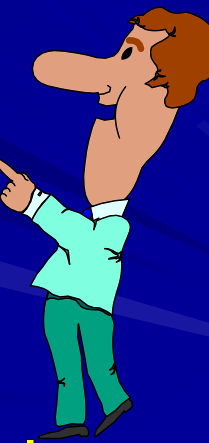
Need a new estimation for ILC

Software Trigger concept → No hardware trigger !



Advantages → all

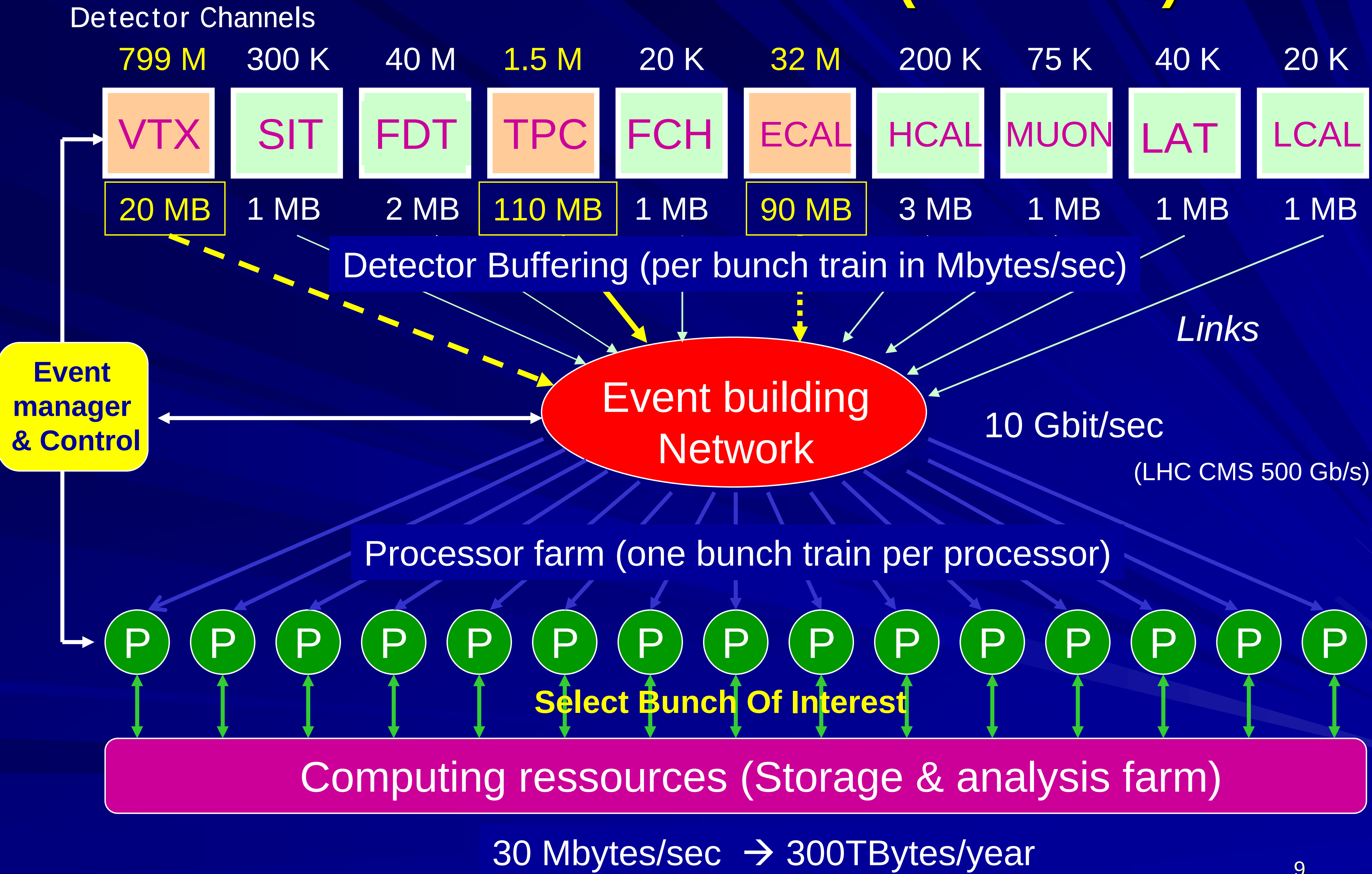
- **Flexible**
  - fully programmable
  - unforeseen backgrounds and physics rates easily accomodated
  - Machine people can adjust the beam using background events
- **Easy maintenance and cost effective**
  - Commodity products : Off The Shelf products
    (Links, memory,switches, processors)
  - Commonly OS and high level languages
  - on-line computing ressources usable for « off-line »
- **Scalable :**
  - modular system



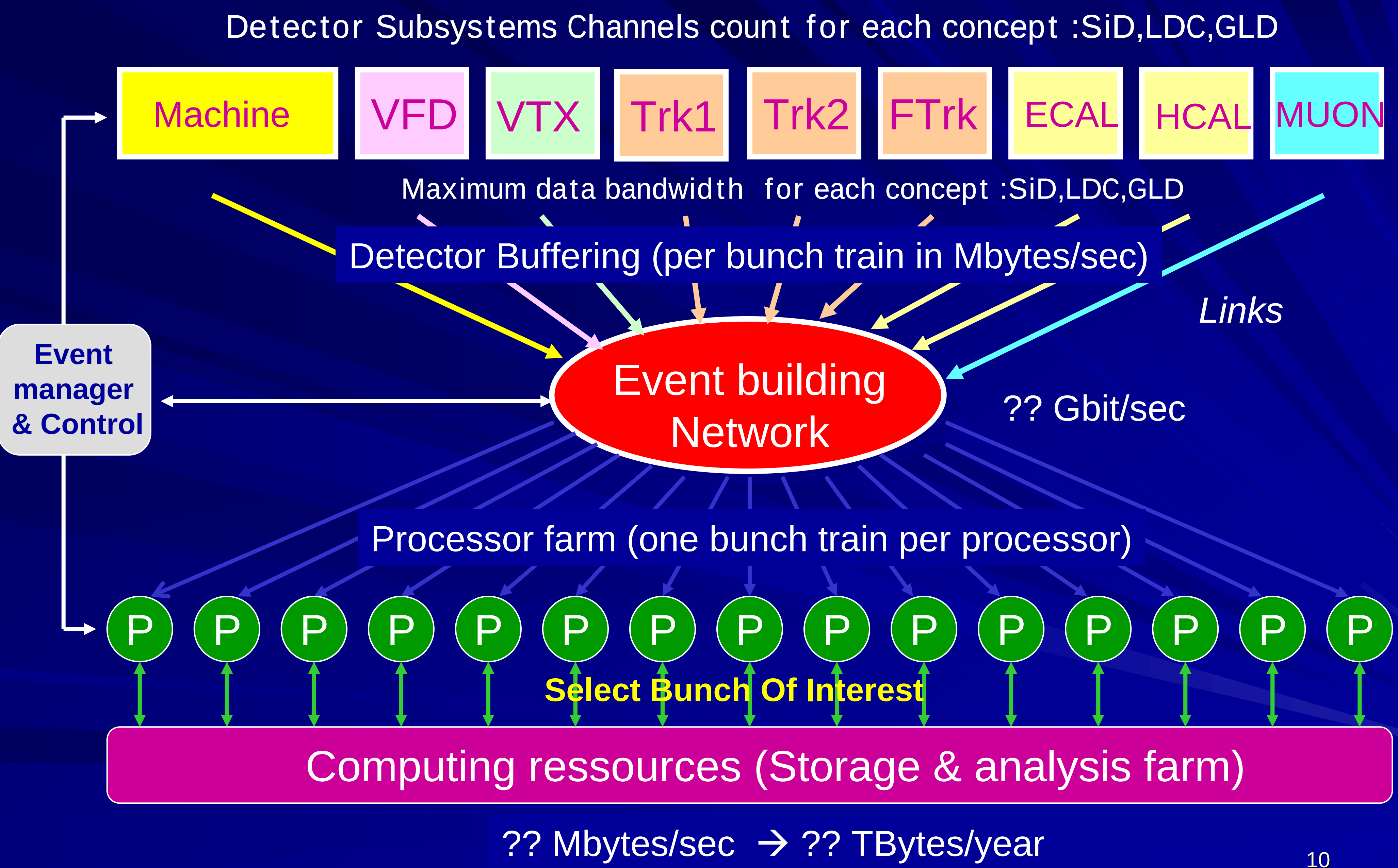
Looks like the ‘ ultimate trigger ’

→ satisfy everybody : no loss and fully programmable

Tesla Architecture (TDR 2003)



ILC DAQ conceptual Architecture (2005)



About systems boundaries …..moving due to !
→ evolution of technologies,sociology …..

NEW !

Machine
Synchronization
Detector feedback
Beam BT adjustment

Subdetectors
FE Read out
Signal processing
Local FE Buffer

Uniform interface

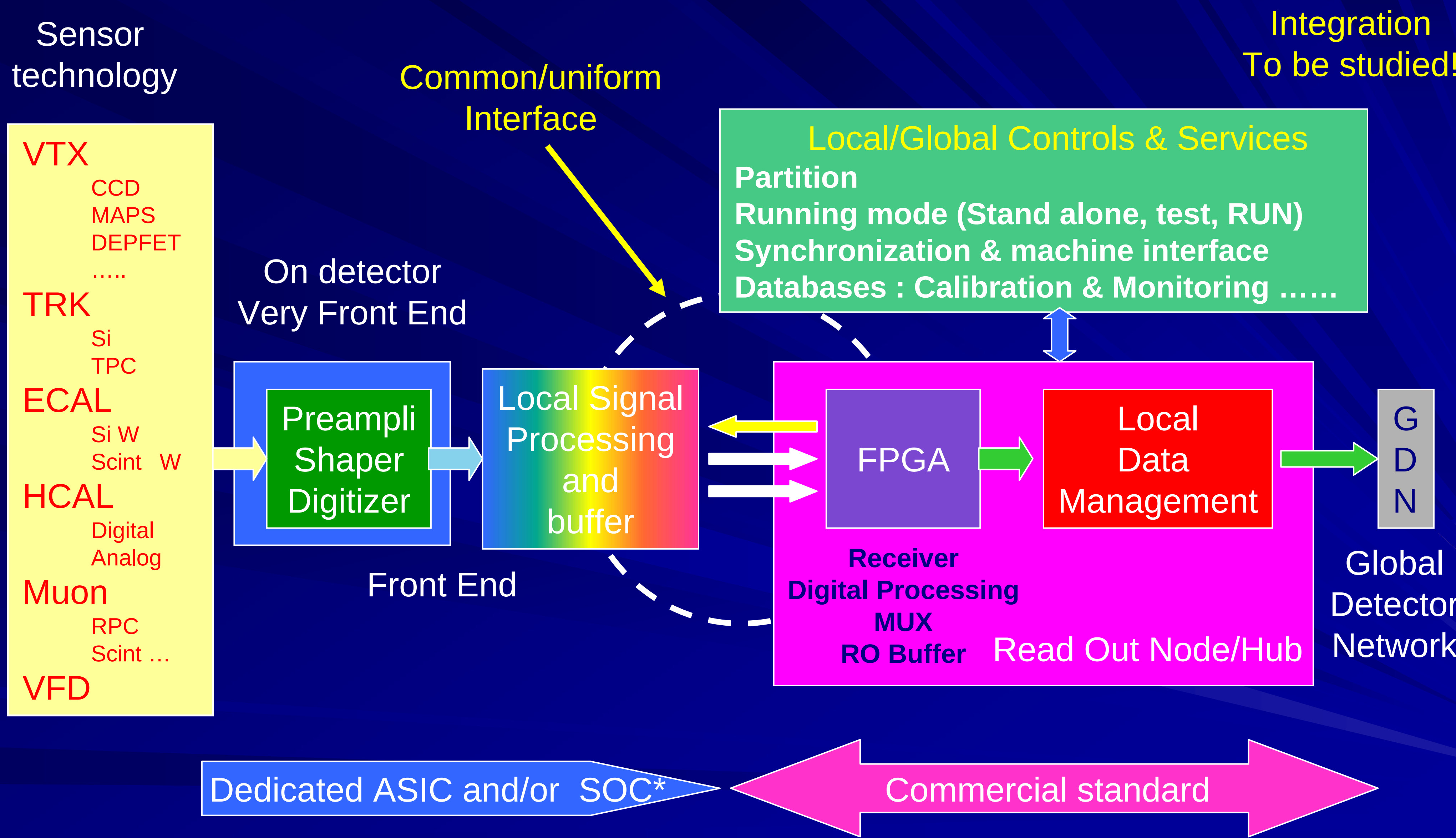
Read out Node
Partitionning
(physical and logical)

Full Integration
of Machine DAQ
In the data
collection system

Global Detector Nerwork (worlwide)
- Detector Integration
- Remote Control Rooms (3?)
  - Running modes
    - Local stand alone
    - Test
    - Global RUN
  - Remote shifts
    - Slow control
    - Detector Monitoring
- Physics & data analysis (ex On- Off line)
  - Farms
  - GRID …
- Final Data storage

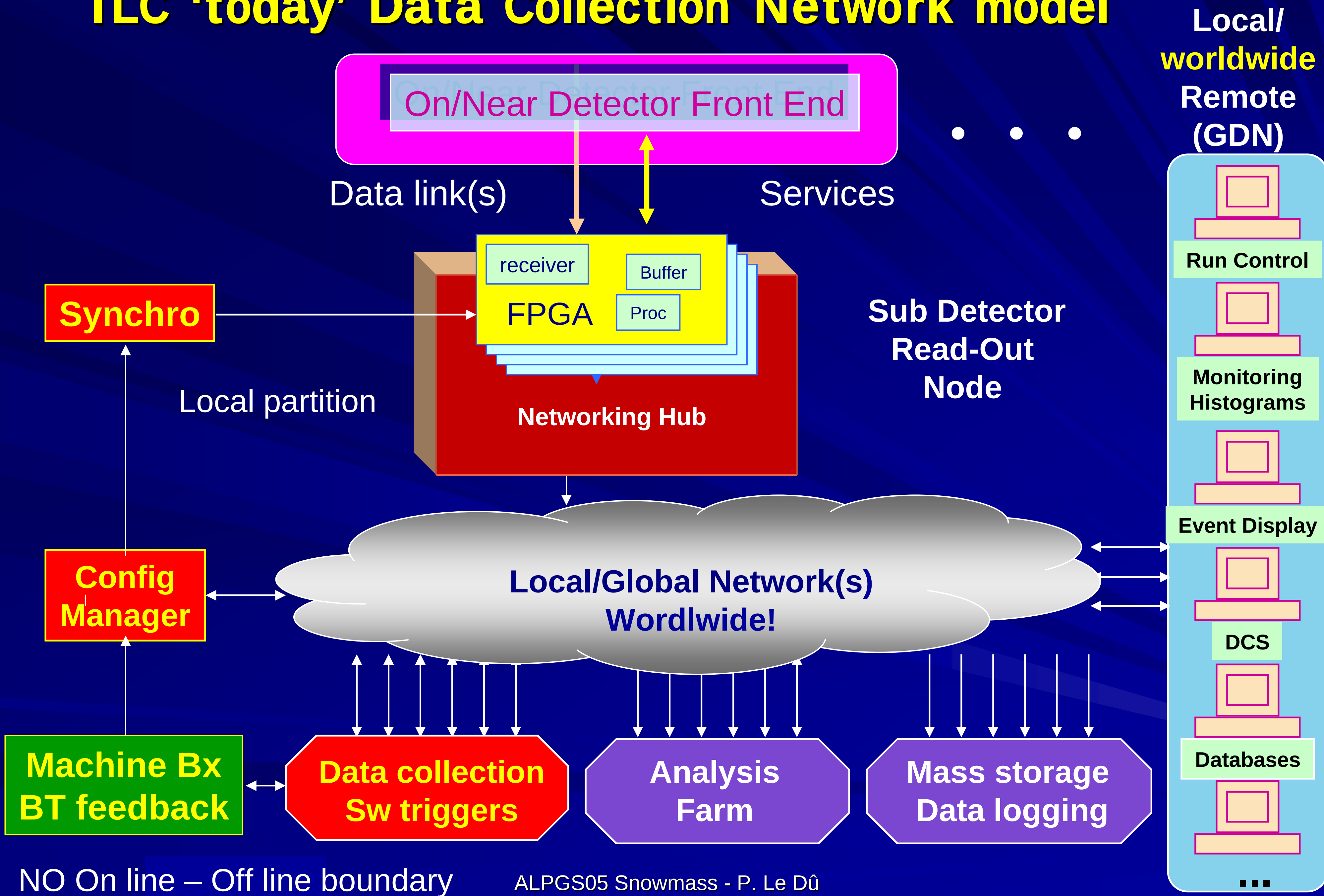
Data Collection (ex on-line)
Bunch Train Buffer RO
Event Building
Control - supervisor
On line Processing
SW trigger & algorithms
Global calibration ,monitoring and physics
Local (temporary) Data logging (Disks)

Possible common RO architecture model



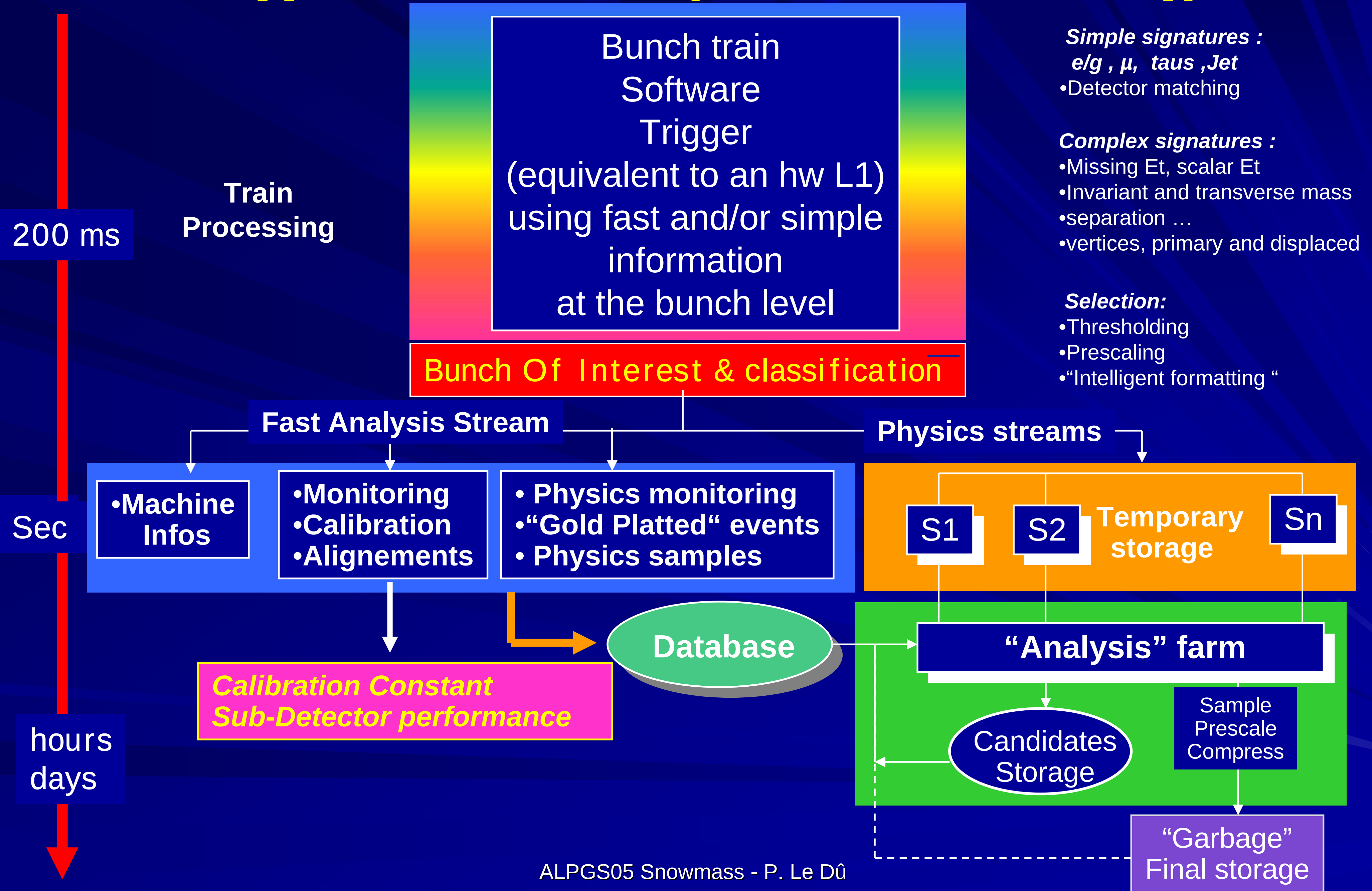
System On Chip

ILC ‘today’ Data Collection Network model



NO On line – Off line boundary

Trigger & Event Analysis common strategy

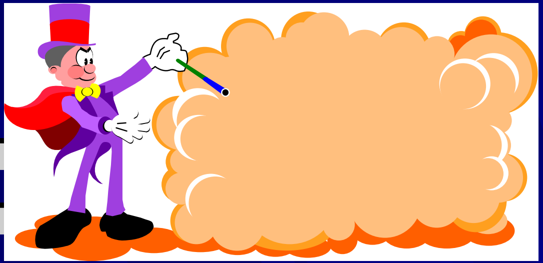


Technology forecast

Summary of the talk given by D. Calvet at the IEEE Real Time Conference ;Stockholm 4-10 june 2005.
"A Review of Techniques and Technologies for the Transport of Digital Data in Physics Experiments"

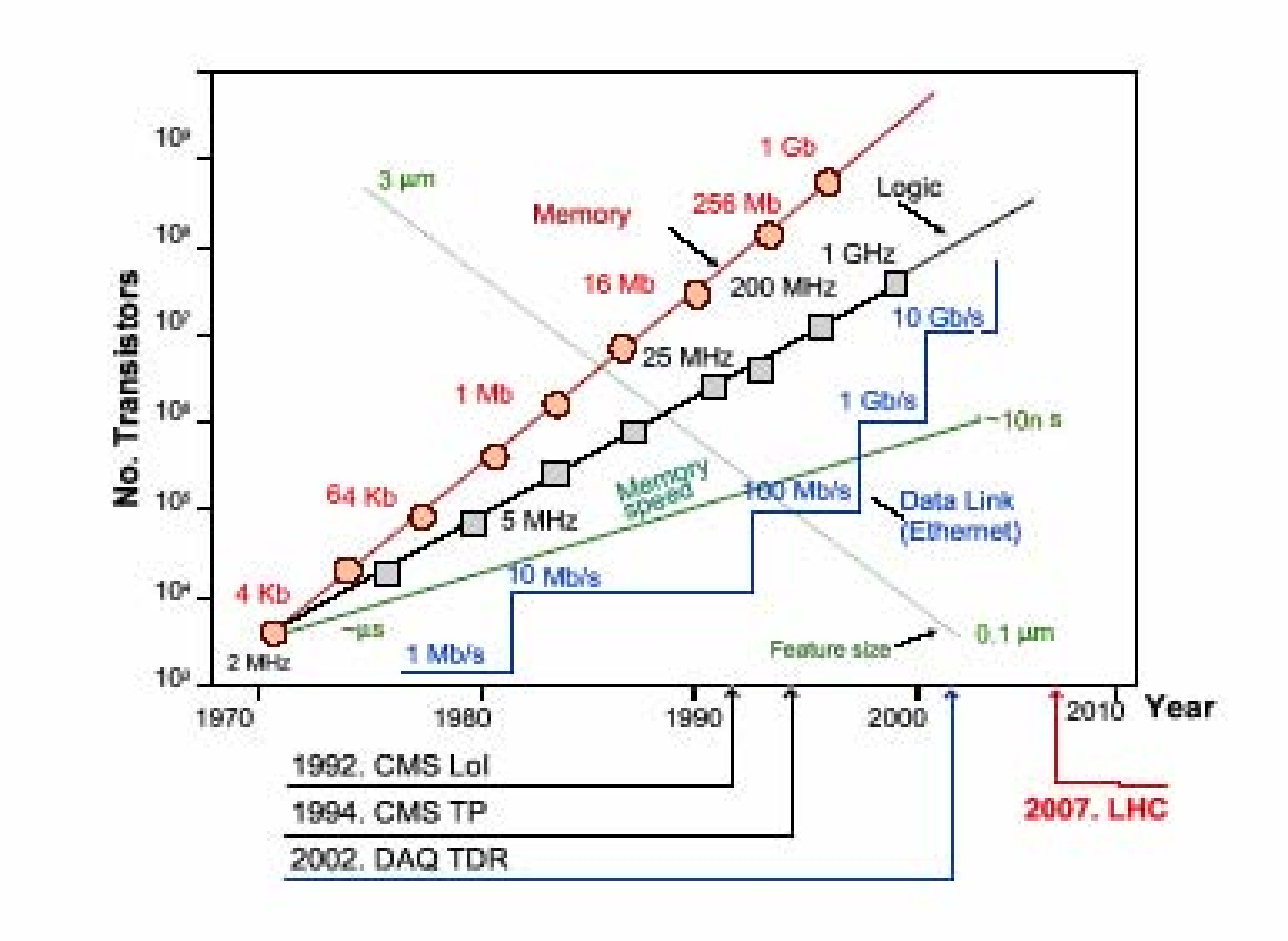
- **End of traditional parallel backplane bus paradigm**
  - Announced every year since ~1989
  - VME-PCI still there; watch PCI Express, RapidIO, ATCA
- **Commercial networking products for T/DAQ**
  - DAQ 94' Conference: ATM, DS-Link, Fibre Channel, SCI
  - Today: Gigabit Ethernet (1 → 10 → 30 GB/s)
- **The ideal processing / memory / IO bandwidth device**
  - The past: Transputers, DSPs
  - Today: FPGAs → Integrates receiver links, PPC, DSPs and memory ....
- **Point-to-point link technology**
  - The old style: Parallel Copper – Serial Optical
  - The modern style: Serial Copper – Parallel Optics
  - >3Gb/s today, 10Gb/s in demonstration

Technology forecast (Con't)



- **Processors**
  - More's law still true until 2010 !
  - Continuous increasing of the computing power
  - Today 4GHz clock → 10 to 15 GHz in 2010 !
- **Memory size quasi illimited !**
  - Today : 256 MB
  - 2010 : > 1 GB … then ?
- **Modern wisdom (about technology)**
  - *"People tend to overestimate what can be done in one year, and underestimate what can be done in 10 years."*

The LHC example



Some ideas about cost

- LHC ATLAS (manpower not included)
  - TDR (1994) → 50 MSF (30 M€) → L1,L2,L3/filter,DAQ
  - Today (2005) → 25-30 MSF (15 M€)
- ILC should not be bigger !
  - Not more than 20 M€
  - Estimate manpower ?
  - Software ?
  - Maintenance ....

What next (1) → Snowmass → LCWS06

- **Understanding in details Detectors Read out schemes**
  - Data Collection (DAQ) is starting at the Detector level
  - By Subdetectors technology→ Independently of detector concepts
  - By Detector concepts SiD,LDC,GLD → what are the particularities?
  - Propose a common architecture (VTX,TRK, CALORs,Muon …)
    - Do not forget the Very Forward !
  - Influence of technical aspects → Power cycling & beam RF pick-up ….
- **Refine the s/w trigger concept → ILC T/DAQ model**
  - Special triggers (Calibration,Tests,cosmics …)
  - Possible Scenarios for Bunch Of Interest fast selection
    - Needs for hardware preprocesing ?
- **Interface with machine**
  - Common aspects : can the machine & Detector DAQ could be similar?
  - Which infos are needed?
  - Integration of Beam Train feedback
- **Define clearly the 'boundaries' → functional block diagram**
  - Integration of GDN → Integrated computing model (GRID)
  - 'Slow controls' and monitoring
  - Partitionning …..

What next (2) → Snowmass → LCWS06

- **Milestone for 2006 (CDR) → Baseline ILC support document**
  - Define a list of technical issues and challenges to be addressed
  - Practicing state of the art technologies and evaluate commercial « new » tools & standards (FPGAs, ACTA,PCIe,wireless?,networking hubs …)

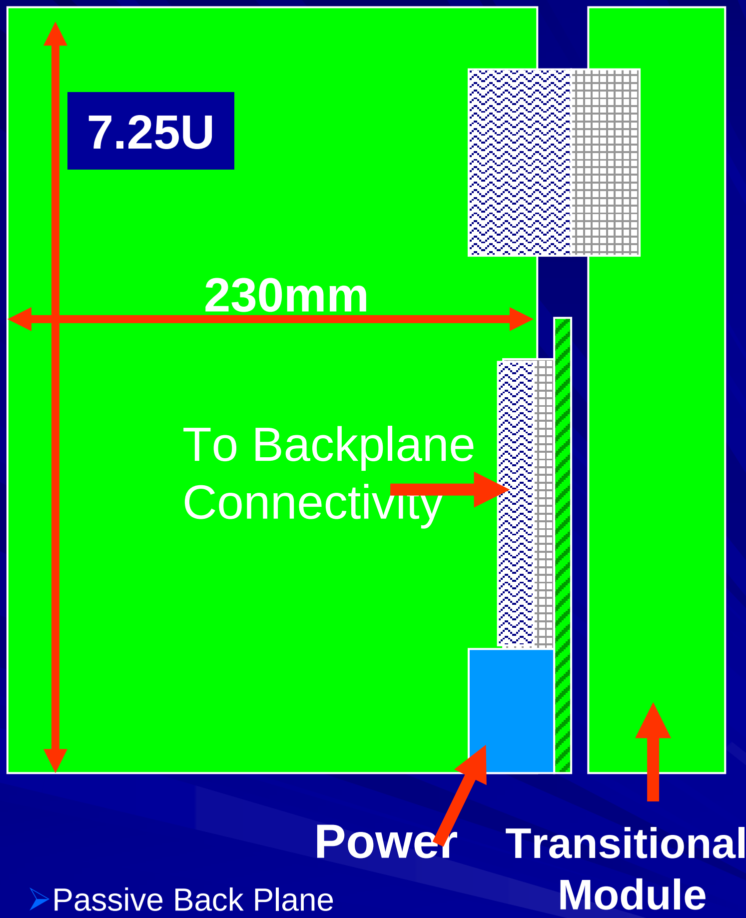
- **Toward a realistic costing model**
  - Global to the 3 detectors concepts
  - Table of parameters: Estimate number of channels, bandwidth ….
  - Estimate quantity of hardware (interfaces, processors, links …), software ? and manpower (is LHC a good model?)

- **Build a wordwide 'international 'long term' strong team**
  - Seniors with LEP/SLD,Hera/LHC/Tevatron,Babar/Belle/KEK experience
  - Younger with enthousiasm!
  - Establish list of detector contact persons for each detector/concept
  - Europ,North America and Asia → common meetings
  - Include long term sociology → NOT reinventing the wheel!
    - Build ONLY what is needed ! Not competing with industry!….

Compare ACTA* & Bus systems

**Advance Telecom Computing Architecture*

	ATCA	PCI Long	VME (6U)
Board Area cm^2	995	316	373
Power Watts	200	10/25	30
Bandwidth I/O Gb/s	20 Full Duplex	4.3 66 Mhz 64 bits	2.4 VME 2eSST
Front Panel H*W cm	30 * 2	8 * 1.2	21.5 * 2
Component height mm	21.33	14.48	13.72



- Passive Back Plane
- - 48 Volt Power in
- Specifications for PCIe, Infiniband, GigE using the same Back plane
  - AMC (Advanced mezzanine Card)
  - mTCA based on ATC specifications - 4 U PCB
  - Interconnections for Servers

PCI Express : *A New Serial Multi Gigabit Commodity Data Bus*

- New PCs have a new bus called PCI Express is a dual-simplex, point to point serial differential low voltage interconnects that will consolidate application requirements for use by multiple segments in the industrial world. The signaling rate is 2.5 Gbit per second, with 8/10 bit encoding to embed clock in the data stream. On the transmit side parallel data is shifted out serially and on the receive side serial data is shifted into registers for parallel data output. The receiver also recovers the embedded clock.

- This bus can be used to connect module or boxes via twisted pair copper wires.

Table 1: I/O Bus Bandwidth Comparison

	I/O Bus	MHz	Bus Width	Rate	Transmission	Measured
			Bits	Mbytes/sec		@ Yale
PC Buses	Industry Standard Architecture (ISA)	8.3	16	8.3		
	Extended Industry Standard Architecture (EISA)	8.3	32	33		
	Peripheral Component Interconnect (PCI)	33	32	132		
	AGP4X			1,000		
	AGP8X			2,000		
Networks	Ethernet	10	1	1.25	CAT 5 Cable	
	USB 2.0	480 mb	1	55		40
Networks	Gigabit Ethernet	1250	1	125	CAT 5 Cable	65%
	PCI Express	2500	x1	250	Dual Simplex	
			x4	1,000	Dual Simplex	
	PCI Express Gen2	5000	x1	500	Dual Simplex	
			x4	2,000	Dual Simplex	
Networks	Infiniband	2500	x4	1,000	Dual Simplex	75%
Instrumentation						
	CAMAC	1	24	3		3
	FASTCAMAC Level 1	2.5	24	7.5		7.5
	FASTCAMAC Level 2	10	24/48	30/60		40
	VME	10	16-64	20-80 ??		
	Compact PCI	33	32	132		

Toward SOC (System On Chip)

[E. Delagnes CEA-Saclay]

- System on Chip : several functions integrated
  - Ex : Front-end chip for Antarès : pipelines 1GHz, TDC, ADCs…