ILC Trigger & DAQ issues

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Summary of present thinking
Software Trigger concept
Data collection architecture model
Technology forecast
Snowmass program

ALPG_Snowmass05
**Conditions**

**2004 International decision: « cold » machine ‘ à la Tesla’**

**Machine parameters close to**

- 2 x 16 km superconducting Linear **independant** accelerators
- Max 2 interaction points
- → 2 detectors ???
- Energy
  - nominale : 500 Gev
  - maximum : 1 Tev
- IP beam size ~ few μm
- \( L = 2 \times 10^{34} \text{ cm}^{-1} \text{s}^{-1} \)

**The LC is a pulsed machine**

- repetitition rate 5
- bunches per train 2820 → x 2 ?
- bunch separation 337 ns → 150 ns
- train length 950 ns
- train separation 199 ms

-→ long time between trains (short between pulses)
Detector concepts

SiD
- Main Tracker
- EM Calorimeter
- H Calorimeter
- Crystal
- Iron Yoke
- Si Strips
- SiW EM
- 5 Teslas

LDC
- Large gaseous central tracking device (TPC)
- High granularity calorimeters
- High precision microvertex
- All inside 4T magnetic field

GLC
- Large Gaseous Tracker → TPC
- W/Scint EM calor.
- 3 Teslas solenoid
# Evolution of basic parameters

<table>
<thead>
<tr>
<th>Exp.</th>
<th>Year</th>
<th>Collision rate</th>
<th>Channel count</th>
<th>L1A rate</th>
<th>Event building</th>
<th>Processing Power</th>
<th>Sociology</th>
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<tbody>
<tr>
<td>UA’s</td>
<td>1980</td>
<td>3 µsec</td>
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<td>-</td>
<td>-</td>
<td>5-10 MIPS</td>
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<td>LEP</td>
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<td>10-20 µsec</td>
<td>250 - 500K</td>
<td>-</td>
<td>10 Mbit/sec</td>
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<td>BaBar</td>
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<td>Tevatron</td>
<td>2002</td>
<td>396 ns</td>
<td>~ 800 K</td>
<td>10 - 50 KHz</td>
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<td>LHC</td>
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<td>25 ns</td>
<td>200 M*</td>
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<td>20-500 Gbit/s</td>
<td>&gt;10^6 MIPS</td>
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<td>ILC</td>
<td>2015 ?</td>
<td>330 ns</td>
<td>900 M*</td>
<td>3 KHz</td>
<td>10 Gbit/s</td>
<td>~10^5 MIPS</td>
<td>&gt; 2000 ?</td>
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</table>

* Including pixels

## Sub-Detector

<table>
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<tr>
<th></th>
<th>LHC</th>
<th>ILC</th>
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<tr>
<td>Pixel</td>
<td>150 M</td>
<td>800 M</td>
</tr>
<tr>
<td>Microstrips</td>
<td>~ 10 M</td>
<td>~30 M</td>
</tr>
<tr>
<td>Fine grain trackers</td>
<td>~ 400 K</td>
<td>1,5 M</td>
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<tr>
<td>Calorimeters</td>
<td>200 K</td>
<td>max 30 M</td>
</tr>
<tr>
<td>Muon</td>
<td>~1 M</td>
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</table>
Summary of present thinking

The ILC environment poses new challenges & opportunities which will need new technical advances in VFE and RO electronics \( \Rightarrow \) NOT LEP/SLD, NOT LHC!

- Basic scheme: The FEE integrates everything
  \( \Rightarrow \) From signal processing & digitizer to the RO BUFFER ...  

- Very large number of channels to manage (Trakers & EM)
  \( \Rightarrow \) should exploit power pulsing to cut power usage during interburst

- New System aspects (boundaries .. \( \Rightarrow \) GDN !)

- Interface between detector and machine is fundamental
  \( \Rightarrow \) optimize the luminosity \( \Rightarrow \) consequence on the DAQ

- Burst mode allows a fully software trigger !
  \( \Rightarrow \) Looks like the Ultimate Trigger: Take EVERYTHING & sort later !

\( \Rightarrow \) GREAT! A sociological simplification!
Rates and data volume from Tesla to ILC

High Level-1 Trigger (1 MHz)

Physics Rate:
- $e^+ e^- \rightarrow X$ 0.0002/BX
- $e^+ e^- \rightarrow e^+ e^- X$ 0.7/BX

$e^+ e^-$ pair background:
- VXD inner layer 1000 hits/BX
- TPC 15 tracks/BX

→ Background is dominating the rates!

Need a new estimation for ILC
Software Trigger concept → No hardware trigger!

Sub-Detectors FE Read-out
- Signal processing – digitization, no trigger interrupt
- Sparcification, cluster finding and/or data compression
- Buffering

Data Collection is triggered by every train crossing
- Full event building of one bunch train
- Trigger: Software Event Selection using partial information of a complete train (equivalent to L1)
- Select 'Bunch Of Interest'
- Event classification according to physics, calibration & machine needs

On-site processing & monitoring

Data Flow
- Detector Front End
- Read-Out Buffer
- Network
- Processor Farm(s)
- Storage

Data streams: S1, S2, S3, S4, Sn

1 MBytes Average event size

1 ms – up to 1 ms active pipeline (full train)

3000 Hz

200 ms

30 Hz

Few sec – David time free

1 ms

30 Hz
Advantages → all

- **Flexible**
  - fully programmable
  - unforeseen backgrounds and physics rates easily accomodated
  - Machine people can adjust the beam using background events

- **Easy maintenance and cost effective**
  - Commodity products: Off The Shelf products (Links, memory, switches, processors)
  - Commonly OS and high level languages
  - on-line computing ressources usable for « off-line »

- **Scalable** :
  - modular system

Looks like the ‘ ultimate trigger ’
→ satisfy everybody: no loss and fully programmable
Tesla Architecture (TDR 2003)

Detector Channels
- VTX: 799 M
- SIT: 300 K
- FDT: 40 M
- TPC: 1.5 M
- FCH: 20 K
- ECAL: 32 M
- HCAL: 200 K
- MUON: 75 K
- LAT: 40 K
- LCAL: 20 K

Detector Buffering (per bunch train in Mbytes/sec)
- VTX: 20 MB
- SIT: 1 MB
- FDT: 2 MB
- TPC: 110 MB
- FCH: 1 MB
- ECAL: 90 MB
- HCAL: 3 MB
- MUON: 1 MB
- LAT: 1 MB
- LCAL: 1 MB

Event building
- Network 10 Gbit/sec
- Event manager & Control
- Processor farm (one bunch train per processor)
  - Select Bunch Of Interest

Computing resources (Storage & analysis farm)
- 30 Mbytes/sec $\rightarrow$ 300TBytes/year

Links
- 10 Gbit/sec (LHC CMS 500 Gb/s)
ILC DAQ conceptual Architecture (2005)

Detector Subsystems Channels count for each concept: SiD, LDC, GLD

Detector Buffering (per bunch train in Mbytes/sec)

Processor farm (one bunch train per processor)

Computing resources (Storage & analysis farm)

Maximum data bandwidth for each concept: SiD, LDC, GLD

Event manager & Control

Network ?? Gbit/sec

Select Bunch Of Interest

?? Mbytes/sec → ?? TBytes/year
About systems boundaries moving due to evolution of technologies, sociology....

**Machine**
- Synchronization
- Detector feedback
- Beam BT adjustment

**Subdetectors**
- FE Read out
- Signal processing
- Local FE Buffer

**Global Detector Network** (worldwide)
- Detector Integration
- Remote Control Rooms (3?)
  - Running modes
    - Local stand alone
    - Test
    - Global RUN
  - Remote shifts
    - Slow control
    - Detector Monitoring
- Physics & data analysis
  - Farms
  - GRID ...
- Final Data storage

**Data Collection (ex on-line)**
- Bunch Train Buffer RO
- Event Building
- Control - supervisor
- On line Processing
- SW trigger & algorithms
- Global calibration, monitoring and physics

**Read out Node**
- Partitioning (physical and logical)

**New!**
Full Integration of Machine DAQ
In the data collection system
**Possible common RO architecture model**

**Sensor technology**
- VTX (CCD, MAPS, DEPFET, ...)
- TRK (Si, TPC)
- ECAL (Si W, Scint W)
- HCAL (Digital, Analog)
- Muon (RPC, Scint ...)
- VFD

**Common/uniform Interface**
- Preamplifier
- Shaper
- Digitizer

**Local/Global Controls & Services**
- Partition
- Running mode (Stand alone, test, RUN)
- Synchronization & machine interface
- Databases: Calibration & Monitoring

**Integration**
- To be studied!

**On detector**
- Very Front End

**Front End**
- Local Signal Processing and buffer

**Read Out Node/Hub**
- FPGA
- Local Data Management
- Receiver
- Digital Processing
- MUX
- RO Buffer

**Global Detector Network**
- GDN

**Commercial standard**

**Dedicated ASIC and/or SOC**

*System On Chip*
ILC 'today' Data Collection Network model

- On/Near Detector Front End
- Data link(s)
- Services
- Networking Hub
- FPGA
- receiver
- Buffer
- Proc
- Sub Detector Read-Out Node
- Local/Global Network(s)
- Worldwide!
- Local partition
- Synchro
- Config Manager
- Machine Bx BT feedback
- Data collection Sw triggers
- Analysis Farm
- Mass storage Data logging
- Run Control
- Monitoring Histograms
- Event Display
- DCS
- Databases
- NO On line – Off line boundary

Local/ worldwide
Remote (GDN)
Trigger & Event Analysis common strategy

Bunch train
Software
Trigger
(equivalent to an hw L1)
using fast and/or simple
information
at the bunch level

Bunch Of Interest & classification

Train Processing

200 ms

Fast Analysis Stream

• Machine Infos
• Monitoring
• Calibration
• Alignements

• Physics monitoring
• “Gold Platted” events
• Physics samples

S1
S2
Temporary storage
Sn

“Analysis” farm

Database

Calibration Constant
Sub-Detector performance

Simple signatures :
e/g, \mu, \tau, Jet
• Detector matching

Complex signatures :
• Missing Et, scalar Et
• Invariant and transverse mass
• separation ...
• vertices, primary and displaced

Selection:
• Thresholding
• Prescaling
• “Intelligent formatting”

Physics streams

Sample
Prescale
Compress
“Garbage”
Final storage

Bunch Of Interest & classification

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Technology forecast

End of traditional parallel backplane bus paradigm
- Announced every year since ~1989
- VME-PCI still there; watch PCI Express, RapidIO, ATCA

Commercial networking products for T/DAQ
- DAQ 94' Conference: ATM, DS-Link, Fibre Channel, SCI
- Today: Gigabit Ethernet (1 → 10 → 30 GB/s)

The ideal processing / memory / IO bandwidth device
- The past: Transputers, DSPs
- Today: FPGAs → Integrates receiver links, PPC, DSPs and memory ....

Point-to-point link technology
- The old style: Parallel Copper - Serial Optical
- The modern style: Serial Copper - Parallel Optics
- >3Gb/s today, 10Gb/s in demonstration
Technology forecast (Con't)

- **Processors**
  - More’s law still true until 2010!
  - Continuous increasing of the computing power
  - Today 4GHz clock → 10 to 15 GHz in 2010!

- **Memory size quasi unlimited!**
  - Today: 256 MB
  - 2010: > 1 GB ... then?

- **Modern wisdom (about technology)**
  - "People tend to overestimate what can be done in one year, and underestimate what can be done in 10 years."
The LHC example
Some ideas about cost

- **LHC ATLAS (manpower not included)**
  - TDR (1994) → 50 MSF (30 M€) → L1,L2,L3/filter,DAQ
  - Today (2005) → 25-30 MSF (15 M€)

- **ILC should not be bigger!**
  - Not more than 20 M€
  - Estimate manpower?
  - Software?
  - Maintenance....
What next (1) → Snowmass → LCWS06

**Understanding in details Detectors Read out schemes**
- Data Collection (DAQ) is starting at the Detector level
- By Subdetectors technology → Independently of detector concepts
- By Detector concepts SiD, LDC, GLD → what are the particularities?
- Propose a common architecture (VTX, TRK, CALORs, Muon ...)
  - Do not forget the Very Forward!
- Influence of technical aspects → Power cycling & beam RF pick-up ....

**Refine the s/w trigger concept → ILC T/DAQ model**
- Special triggers (Calibration, Tests, cosmics ...)
- Possible Scenarios for Bunch Of Interest fast selection
  - Needs for hardware preprocessing?

**Interface with machine**
- Common aspects: can the machine & Detector DAQ could be similar?
- Which infos are needed?
- Integration of Beam Train feedback

**Define clearly the ‘boundaries’ → functional block diagram**
- Integration of GDN → Integrated computing model (GRID)
- ‘Slow controls’ and monitoring
- Partitionning .....
What next (2) → Snowmass → LCWS06

- **Milestone for 2006 (CDR) → Baseline ILC support document**
  - Define a list of technical issues and challenges to be addressed
  - Practicing state of the art technologies and evaluate commercial « new » tools & standards (FPGAs, ACTA, PCIe, wireless?, networking hubs ...)

- **Toward a realistic costing model**
  - Global to the 3 detectors concepts
  - Table of parameters: Estimate number of channels, bandwidth ....
  - Estimate quantity of hardware (interfaces, processors, links ...), software ? and manpower (is LHC a good model?)

- **Build a worldwide 'international 'long term' strong team**
  - Seniors with LEP/SLD, Hera/LHC/Tevatron, Babar/Belle/KEK experience
  - Younger with enthusiasm!
  - Establish list of detector contact persons for each detector/concept
  - Europ, North America and Asia → common meetings
  - Include long term sociology → NOT reinventing the wheel!
    - Build ONLY what is needed! Not competing with industry!....
## Compare ACTA* & Bus systems

*Advance Telecom Computing Architecture*

<table>
<thead>
<tr>
<th></th>
<th>ATCA</th>
<th>PCI Long</th>
<th>VME (6U)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Board Area cm²</strong></td>
<td>995</td>
<td>316</td>
<td>373</td>
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<tr>
<td><strong>Power Watts</strong></td>
<td>200</td>
<td>10/25</td>
<td>30</td>
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<tr>
<td><strong>Bandwidth I/O Gb/s</strong></td>
<td>20 Full Duplex</td>
<td>4.3</td>
<td>2.4</td>
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<tr>
<td></td>
<td></td>
<td>66 Mhz 64 bits</td>
<td>2eSST</td>
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<tr>
<td><strong>Front Panel H*W cm</strong></td>
<td>30 * 2</td>
<td>8 * 1.2</td>
<td>21.5 * 2</td>
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<tr>
<td><strong>Component height mm</strong></td>
<td>21.33</td>
<td>14.48</td>
<td>13.72</td>
</tr>
</tbody>
</table>

- Passive Back Plane
- 48 Volt Power in
- Specifications for PCIe, Infiniband, GigE using the same Back plane
- AMC (Advanced mezzanine Card)
- mTCA based on ATC specifications - 4 U PCB
- Interconnections for Servers
New PCs have a new bus called PCI Express is a dual-simplex, point to point serial differential low voltage interconnects that will consolidate application requirements for use by multiple segments in the industrial world. The signaling rate is 2.5 Gbit per second, with 8/10 bit encoding to embed clock in the data stream. On the transmit side parallel data is shifted out serially and on the receive side serial data is shifted into registers for parallel data output. The receiver also recovers the embedded clock.

This bus can be used to connect module or boxes via twisted pair copper wires.
<table>
<thead>
<tr>
<th>I/O Bus</th>
<th>MHz</th>
<th>Bus Width</th>
<th>Rate Mbytes/sec</th>
<th>Transmission</th>
<th>Measured @ Yale</th>
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<tr>
<td>PC Buses</td>
<td></td>
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<td>Industry Standard Architecture (ISA)</td>
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<td>16</td>
<td>8.3</td>
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<td>Extended Industry Standard Architecture (EISA)</td>
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<td>AGP4X</td>
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<td></td>
<td>1,000</td>
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<td>AGP8X</td>
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<td>2,000</td>
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<td>1.25</td>
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<td>Gigabit Ethernet</td>
<td>1250</td>
<td>x1</td>
<td>125</td>
<td>CAT 5 Cable</td>
<td>65%</td>
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<td>PCI Express</td>
<td>2500</td>
<td>x4</td>
<td>250</td>
<td>Dual Simplex</td>
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<td></td>
<td>5000</td>
<td>x1</td>
<td>500</td>
<td>Dual Simplex</td>
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<td>PCI Express Gen2</td>
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<td>Infiniband</td>
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</table>
Toward SOC (System On Chip)

- System on Chip: several functions integrated
  - Ex: Front-end chip for Antares: pipelines 1GHz, TDC, ADCs...

[Image of a circuit diagram with labels such as PMT, Time base, ARS1 Circuit, and a chip with dimensions 4mm x 5mm]

[E. Delagnes CEA-Saclay]