Results with the Prototype Detectors for the Si/W ECAL

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- Physics Design Requirements
- Detector Concept
- Silicon Detectors - Capacitance and Trace Resistance
- Implications of Accelerator Technology Choice
- MIPS, sources and laser

Si-W work – personnel and responsibilities

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Electronics	**Bump Bonding**, Mechanical Design, **Cabling**	**Electronics**, Mechanical Design, Simulation	**Si Detectors**, Mechanical Design, Simulation

* This work includes contributions from Oregon students Tyler Neely and Mary Robinson.

ECAL Design Requirements

- Optimal contribution to the reconstruction of multijet events:
  - Excellent separation of γ's from charged particles
    Efficiency $> 95\%$ *for energy flow*
  - Excellent linkage of ECAL with tracker (important for SiD)
  - Good linkage of ECAL with HCAL
  - Good reconstruction of $\pi^{\pm}$, detection of neutral hadrons
  - Reasonable EM energy resolution ($\sim 15\%/\sqrt{E}$)

Physics case: jet reconstruction important for many physics processes.

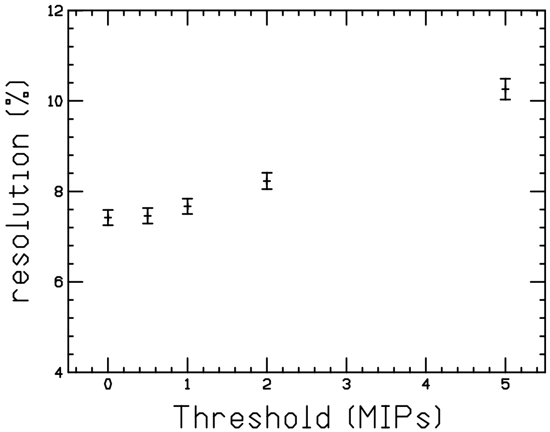
- Longitudinal Sampling, 30 layers needed for EM energy resolution

$$\frac{\sigma_E}{E} \sim 20\% \sqrt{\frac{X}{E}}$$

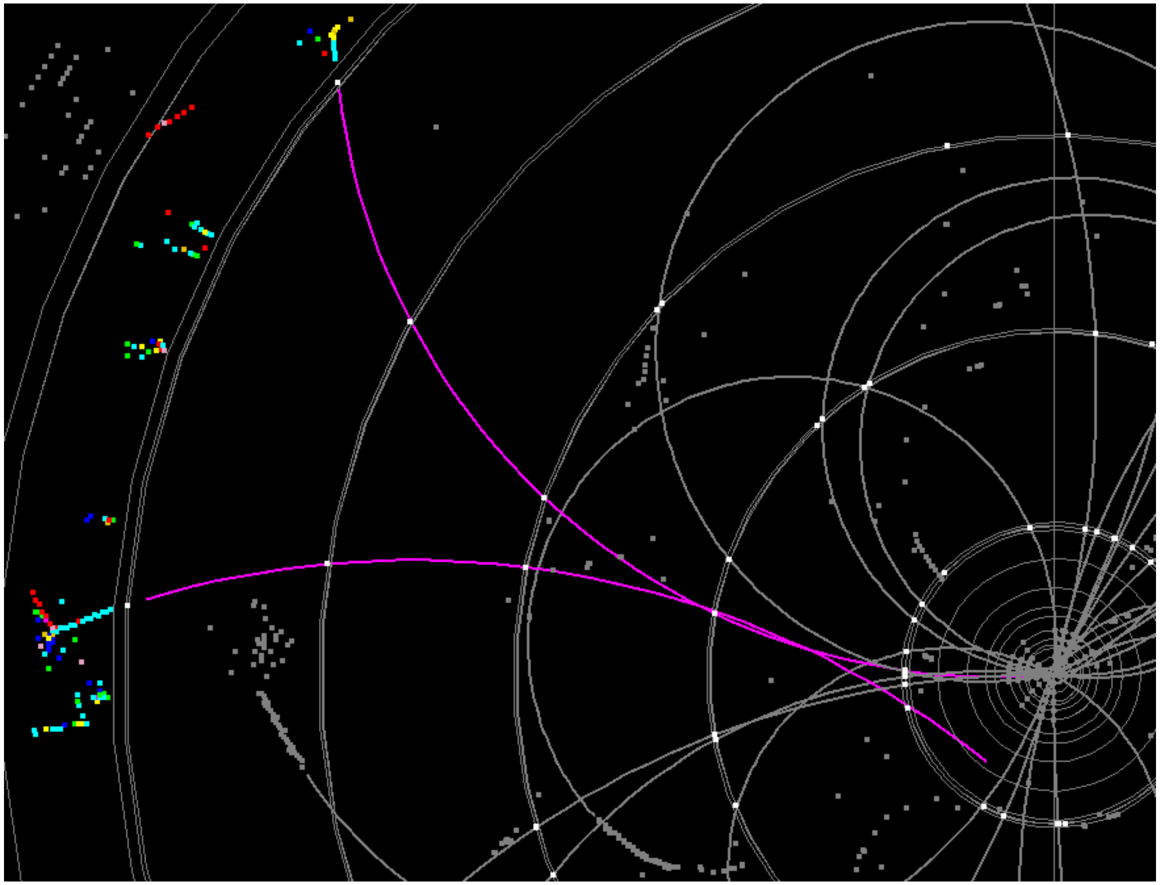
X is the sampling in radiation length.

- Useful for K^0 tracking, etc.

- **Can tolerate small, random inefficiency**

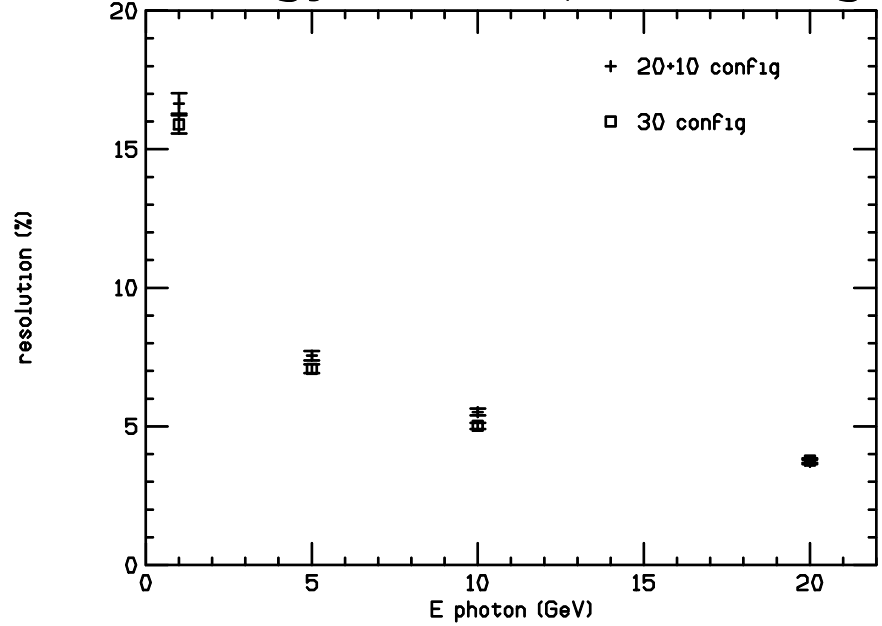


Resolution of 5 GeV photon insensitive to threshold

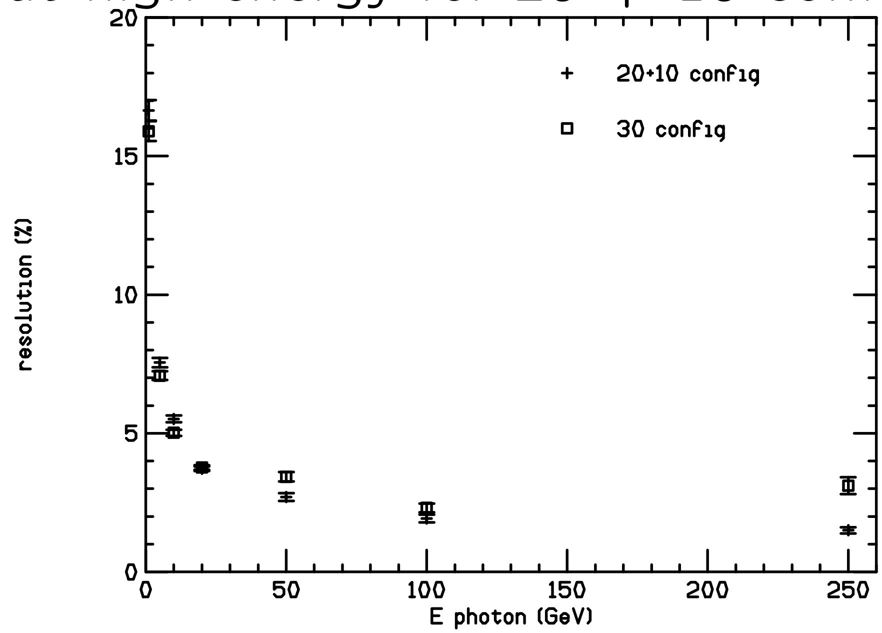


Eckhard von Toerne, LCWS05

- Energy a bit worse at low energy for 20 + 10 configuration



- Energy much better at high energy for 20 + 10 configuration



Importance of Granularity

- Figure of merit for energy reconstruction is

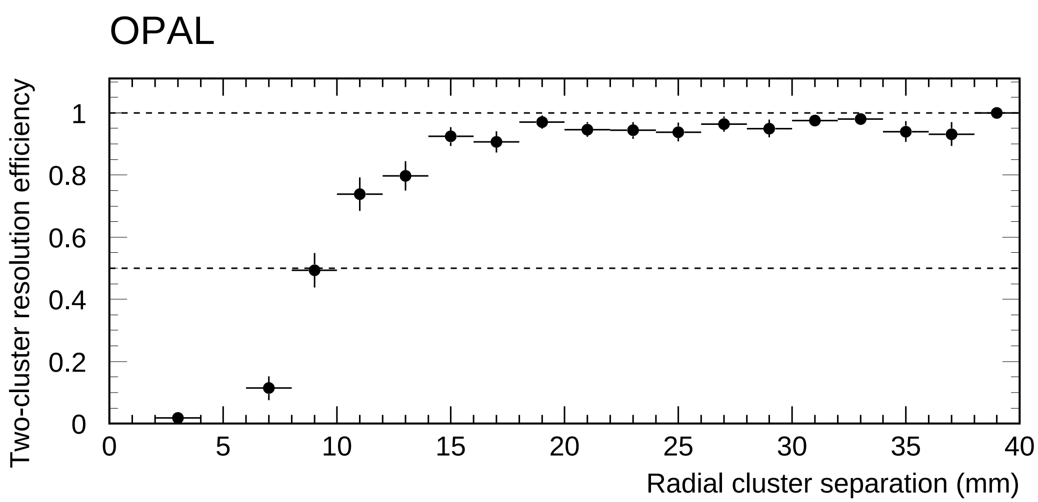
$$f_E \simeq \frac{R_{cal}}{\sqrt{R_M^2 + (4d_{pad})^2}}$$

where R_M is the Molière radius, d_{pad} is the detector pad size and R_{cal} is the inner radius of the calorimeter

Example (OPAL SiW luminosity monitor, $1X_0$ radiator, 3mm gap)

- Photons resolved to $\frac{1}{2}$ of Molière radius

- Pads must be at least $2\times$ smaller



$d = 2.5$mm , $R_M \sim 17$mm

- The costs of the calorimeters, coil, and muon system have

$$\text{cost} \propto R_{cal}^n$$

where n is $\sim 2-3$.

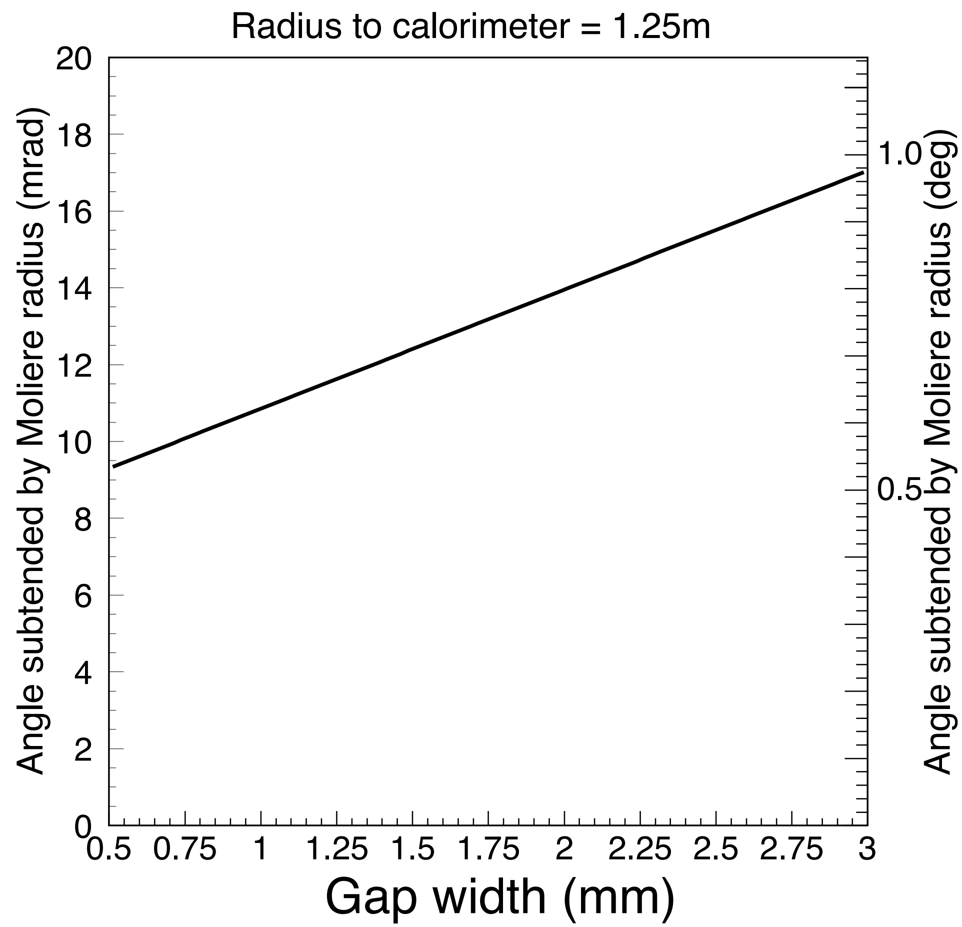
- Thus a 10% increase in the Molière radius of the calorimeter leads to a $>20\%$ increase in cost of the detector for constant f_e.

- Conclusion: try and make the calorimeter as dense as possible

Critical parameter: gap between tungsten layers.

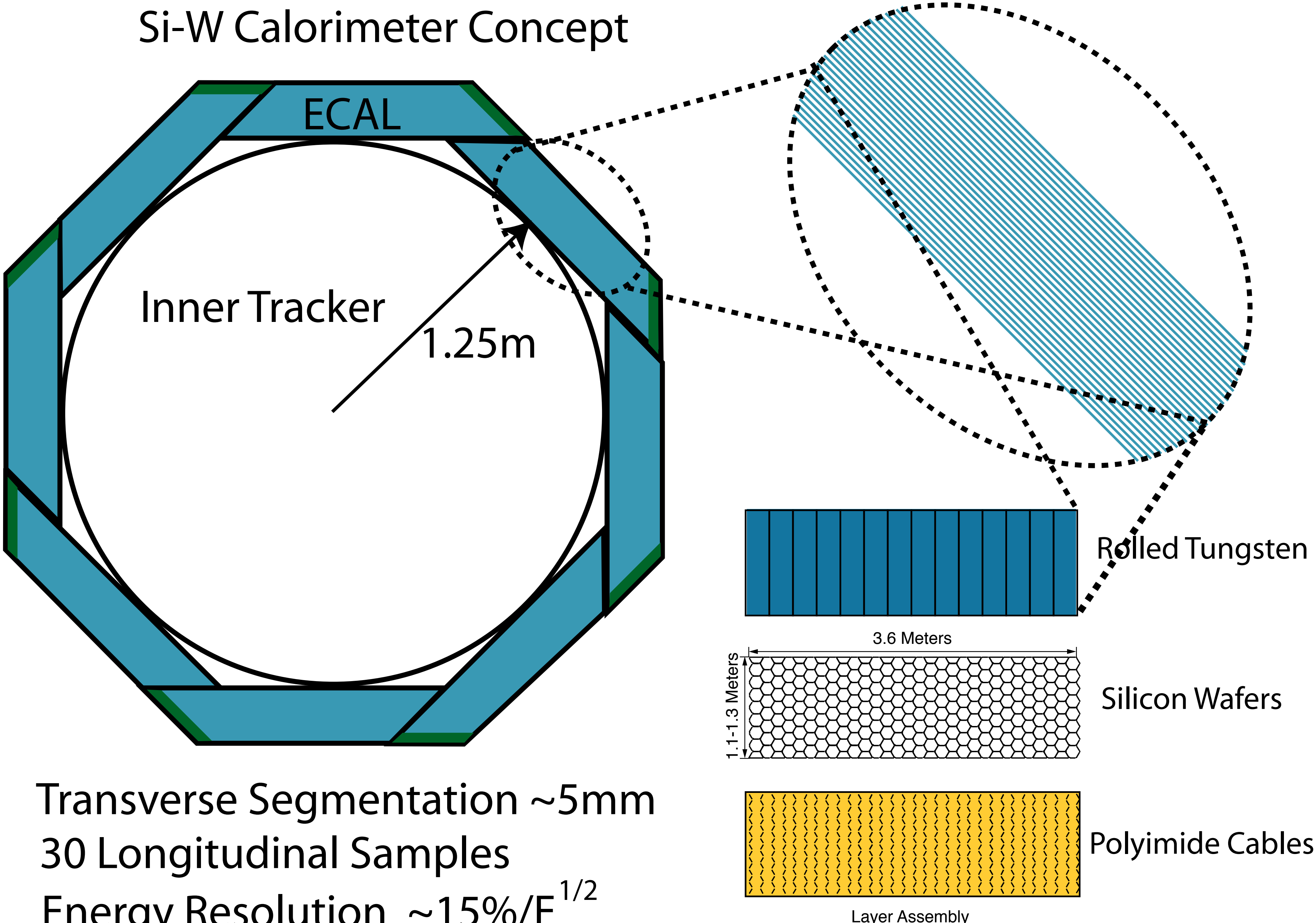
Config.	Radiation length	Molière Radius
100% W	3.5mm	9mm
92.5% W	3.9mm	10mm
+1mm gap	5.5mm	14mm
+1mmCu	6.4mm	17mm

Assumes 2.5mm thick tungsten absorber plates



Calice 3mm gap with 1.7m TESLA radius gives $\frac{R_M}{R_{Cal}} = 13\text{mrad}$

Si-W Calorimeter Concept



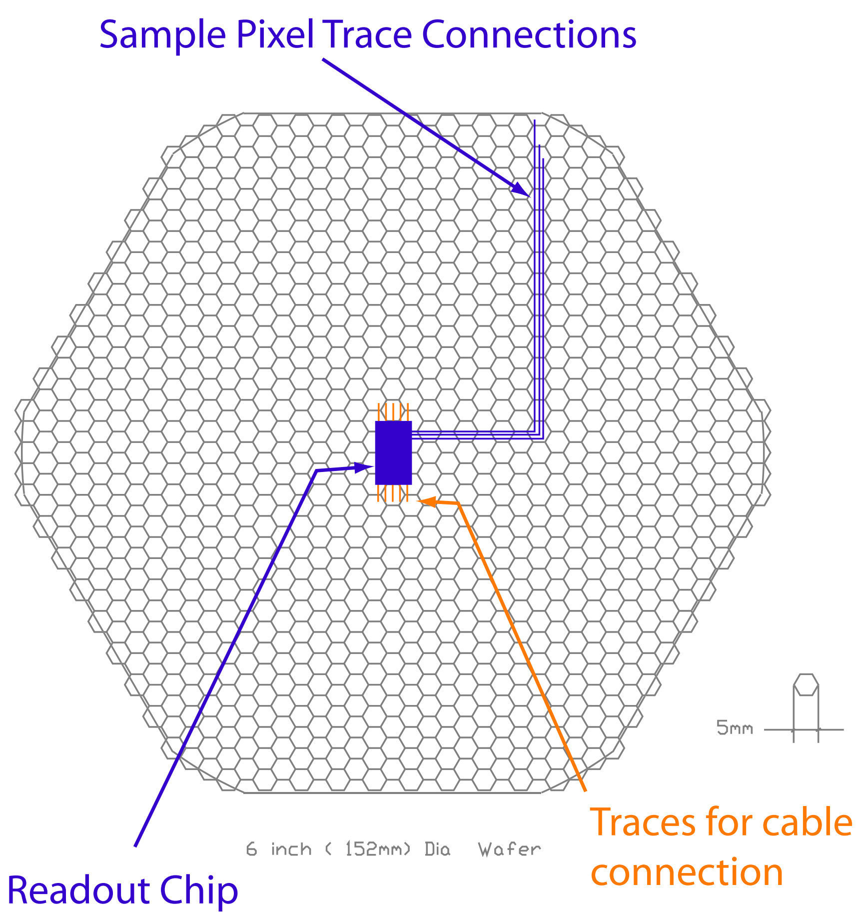
Transverse Segmentation ~5mm

30 Longitudinal Samples

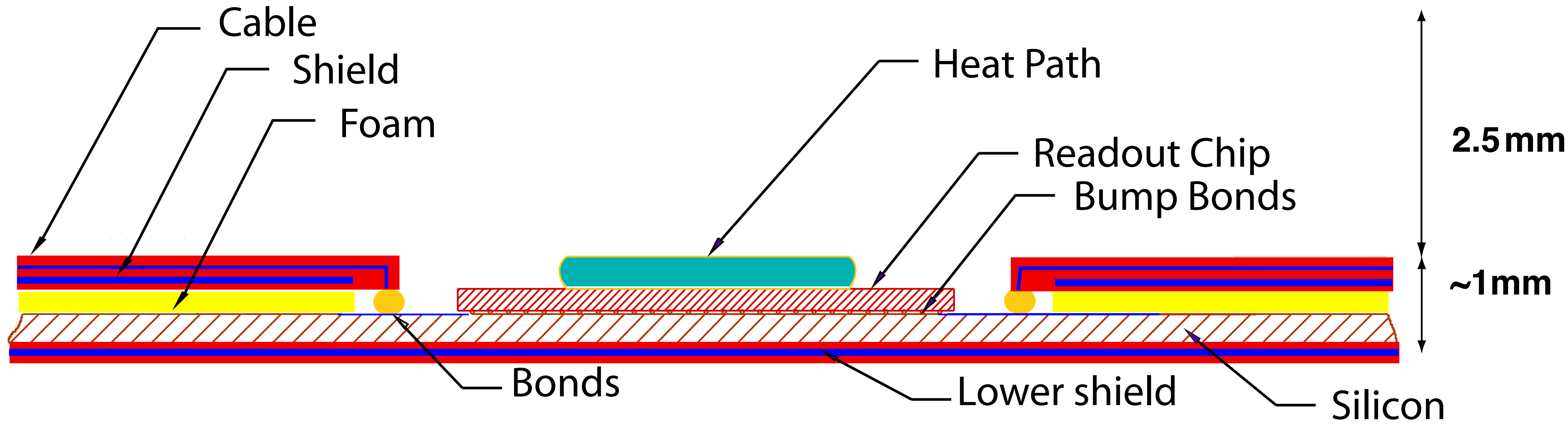
Energy Resolution ~15%/$E^{1/2}$

Silicon Concept

- Readout each wafer with a single chip
- Bump bond chip to wafer
- To first order cost independent of pixels /wafer
- Hexagonal shape makes optimal use of Si wafer
- Channel count limited by power consumption and area of readout end chip
- May want different pad layout in forward region



Critical parameter: minimum space between tungsten layers.



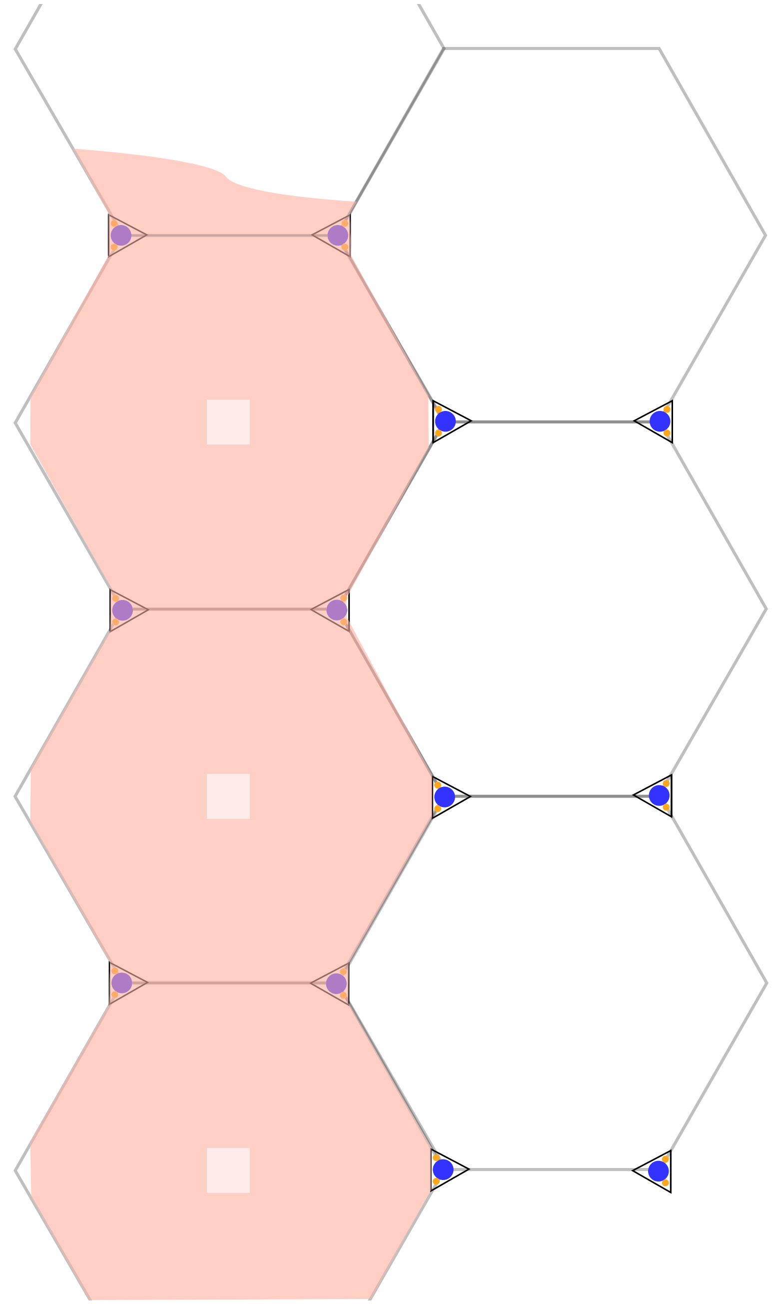
- Cartoon represents my personnel view

- Note elimination of on–wafer capacitors and the addition of upper and lower shields. Requires low resistance connection between and upper and lower side of wafer

- Bias may require an additional connection (figure assumes top side bias)

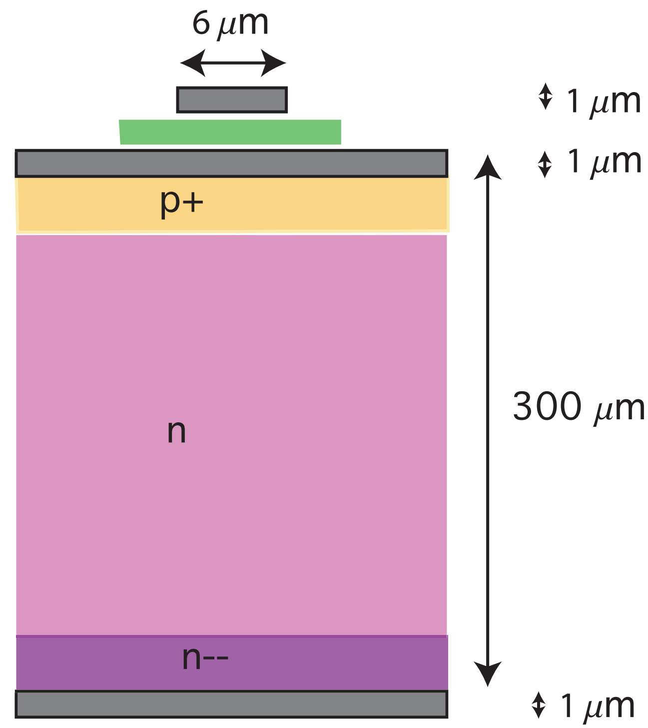
Cable Concept
(UC Davis)

- Anchor cables at vertices
- Tungsten plates held off by spacers at vertices

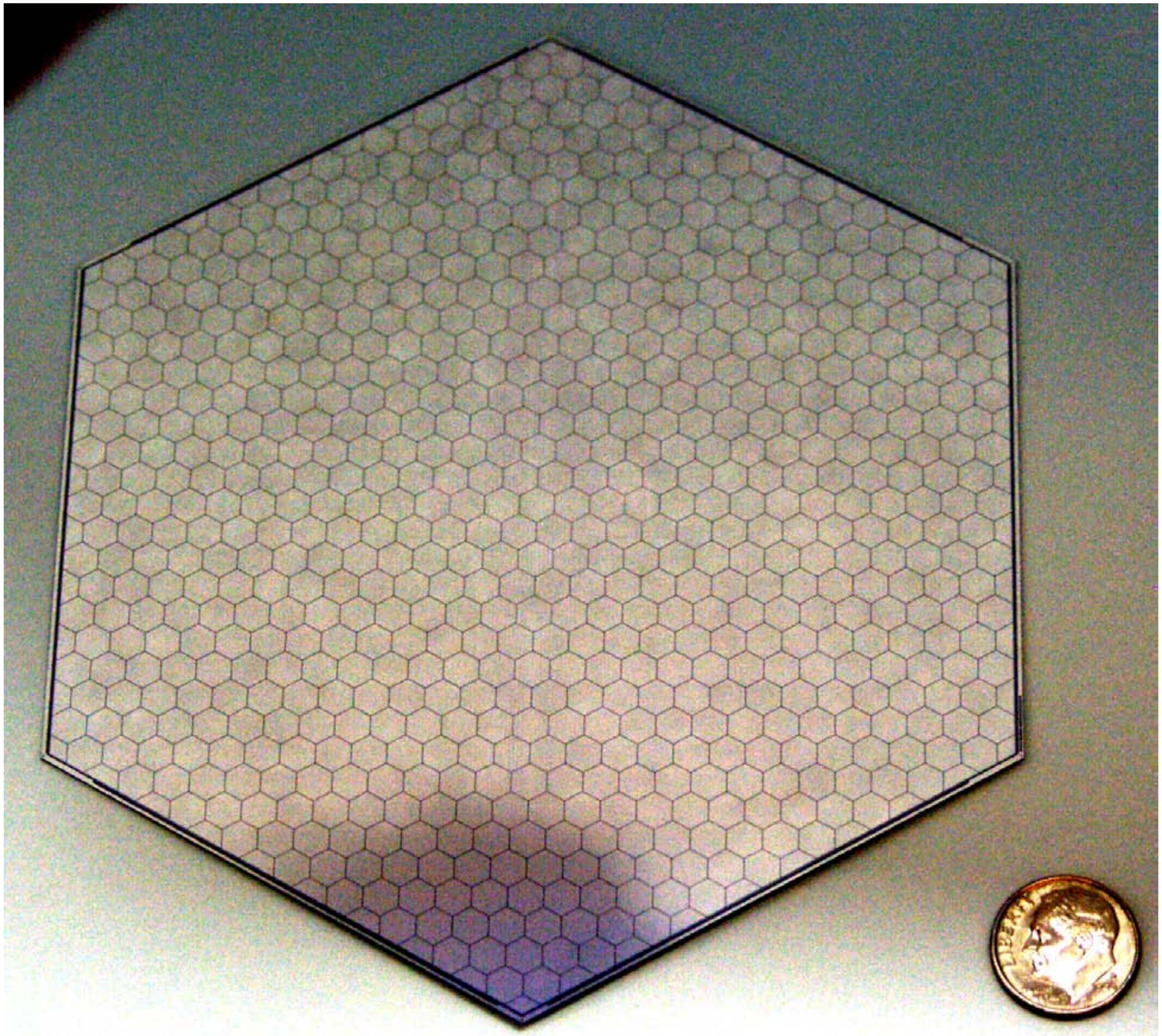


Silicon Detector Design

- DC coupled detectors (avoids bias resistor network)
- Two metal layers
- Keep Si design as simple as possible to reduce cost
- Cross talk looks small with current electronics design
- Trace capacitances (up to 30pF) are bigger than the 5pF pixel capacitance

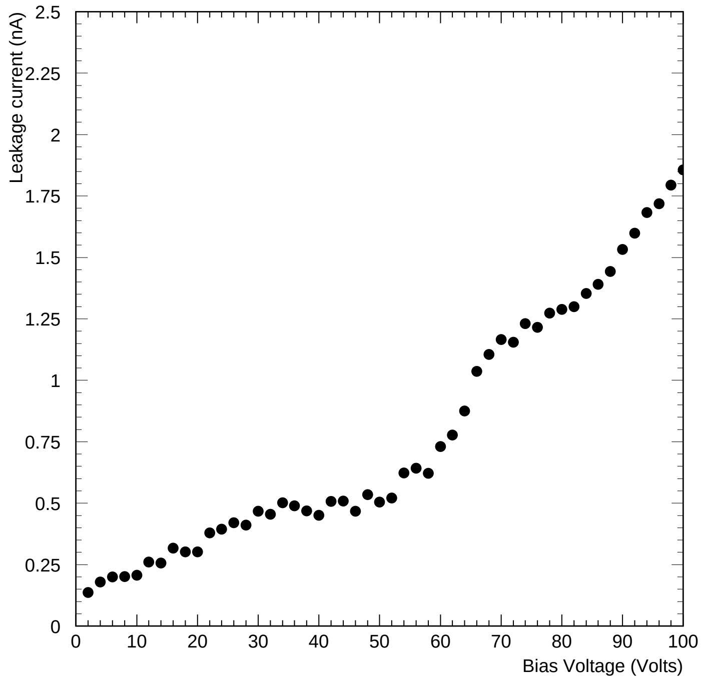


Ten Hamamatsu detectors are in hand



Measurements on Silicon Detector Prototypes

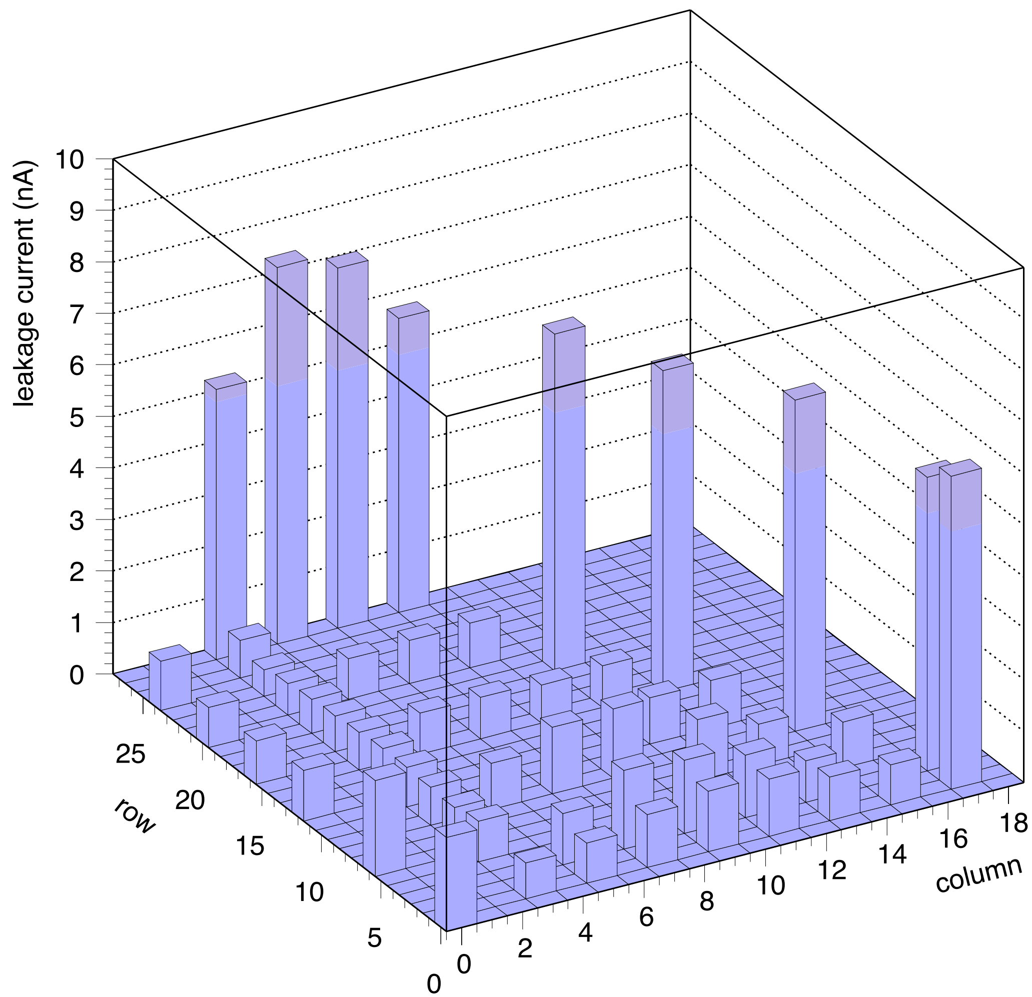
Leakage Current Looks Fine:



(10nA for 1μs gives only 250 electrons noise)

NB: Neighboring pixels are not grounded.

Spot check of leakage current in one quadrant is as expected.



Note edge pixels have larger currents. In these tests the guard ring was left floating.

⇒ **Measurement of resistance slightly larger than nominal**

Series resistance for 1μm by 6 μm :

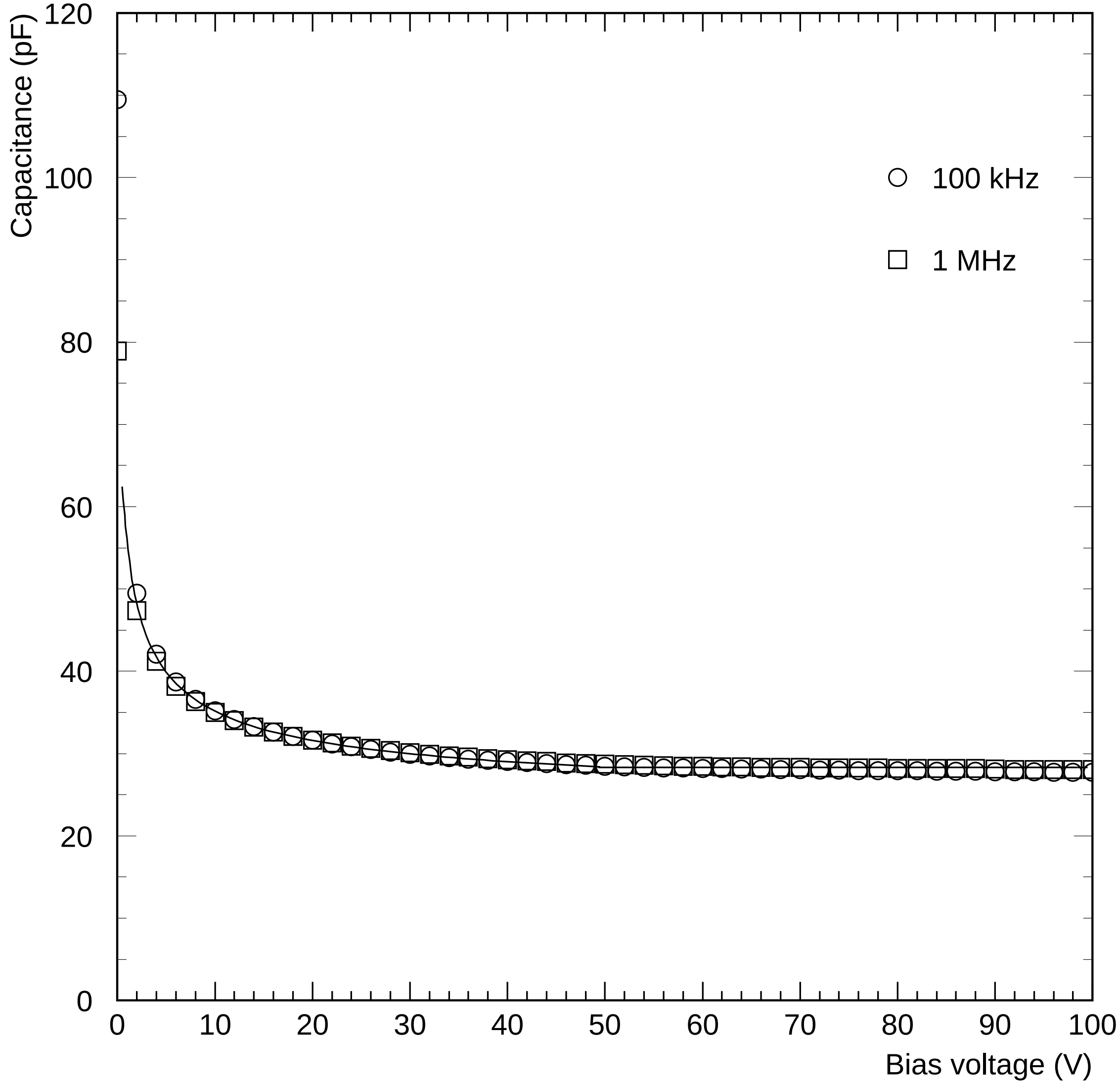
Expected (pure Al)	Measured
47 Ω/cm	$(57 \pm 2)\Omega$/cm

Expected contributions to detector capacitance:

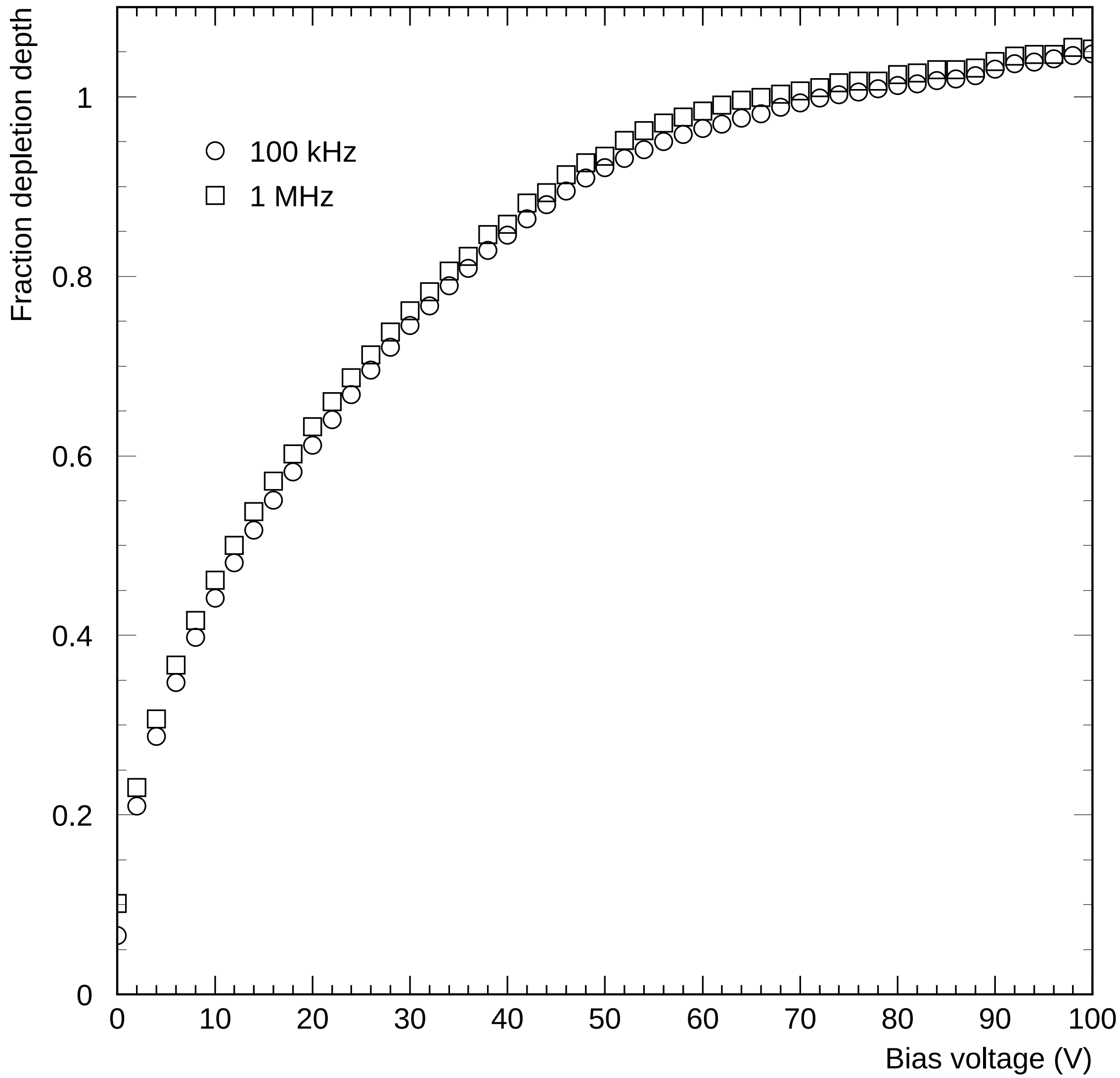
- 5.3pF from pixel capacitance (C_{geom} for 325μm Si)
- $\sim$ 20pF for sum of trace capacitance and capacitance from other traces connecting to other pixels. (C_{stray})
- Pixels under the bump-bond array have additional stray capacitance from probing and bonding pads (currently $\simeq$ 100pF)

Expected curves

$$\begin{aligned} C_{tot} &= C_{stray} + C_{geom}\sqrt{\frac{V_{dep}+V_{bi}}{V_{bias}+V_{bi}}} \qquad && V_{bias} < V_{dep} \\ C_{tot} &= C_{stray} + C_{geom} && V_{bias} > V_{dep} \end{aligned}$$



Typical CV curve as measured in lab



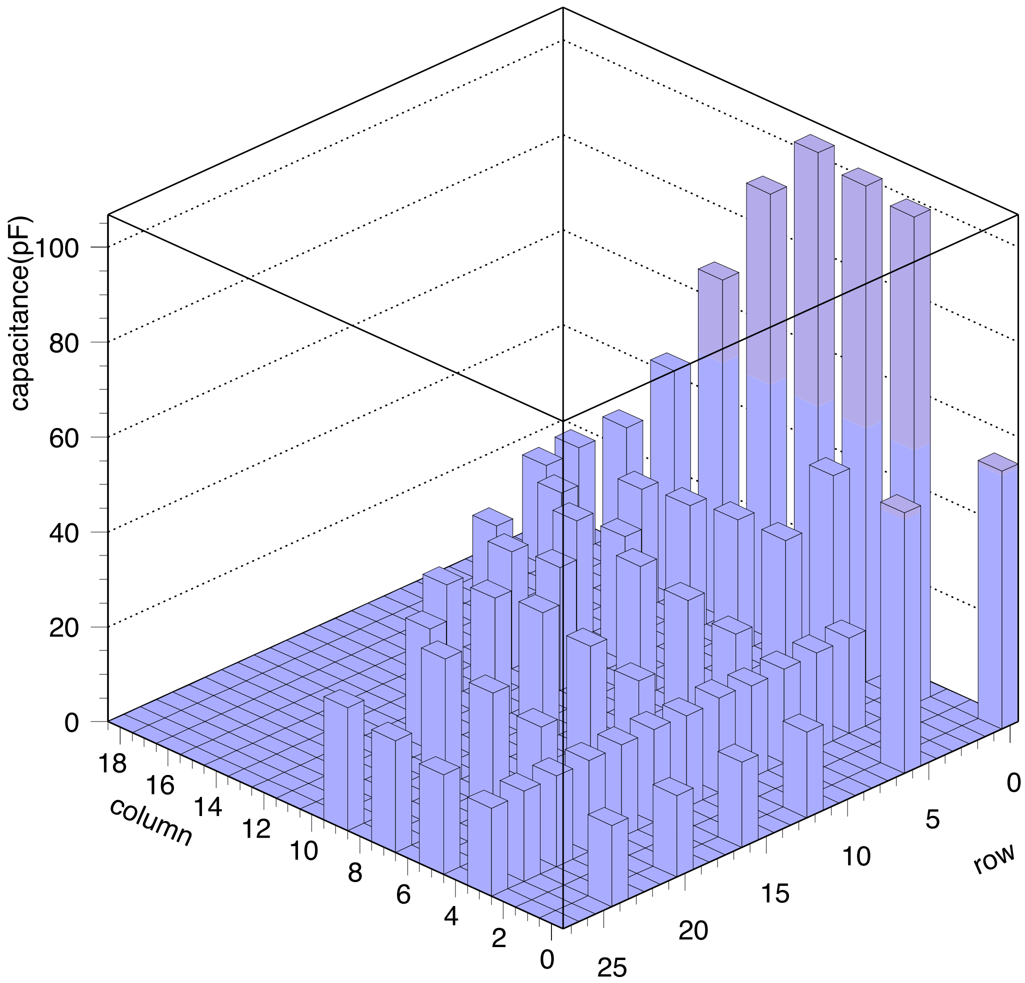
Relative depletion depth as a function of voltage.

Sample stray capacitance measurements obtained from a fit to the CV curve and calculation:

Pixel	Column	Row	Calculated Capacitance(pF)	Measured Capacitance(pF)
567	7	9	23.35±0.61	25.07±0.25
564	7	15	22.96±0.61	24.70±0.24
561	7	21	22.56±0.61	24.23±0.24
558	7	27	22.17±0.61	23.60±0.21
515	5	3	44.00±0.90	46.55±0.42
512	5	9	21.63±0.61	22.55±0.23
509	5	15	21.18±0.61	22.06±0.22
506	5	21	20.73±0.61	21.73±0.22
503	5	27	20.28±0.61	21.00±0.20

$\Rightarrow$ **Measurement agrees with expectation for 0.9 μm thick oxide and 6μm wide traces (3.1 pF/cm).**

Spot check of capacitances in one quadrant is as expected.



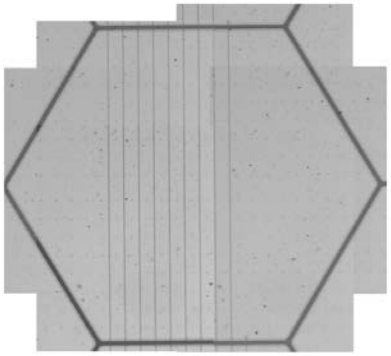
Impact of Detector Technology on Detector Design

$\Rightarrow$ In a warm machine, exceptional pixels with large capacitance or series resistance lead to degraded time tag measurements

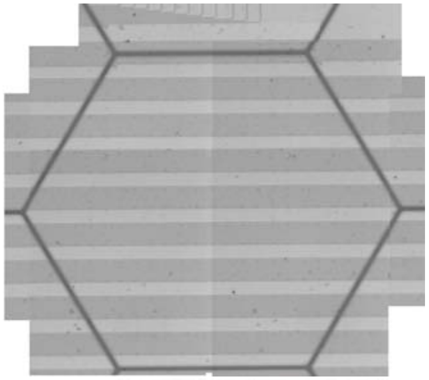
- Small impact on tagging performance since bad channels can be de-weighted in determining the average time of a track

$\Rightarrow$ In a cold machine, exceptional pixels with large capacitance or series resistance lead to a higher rate of noise events in buffers

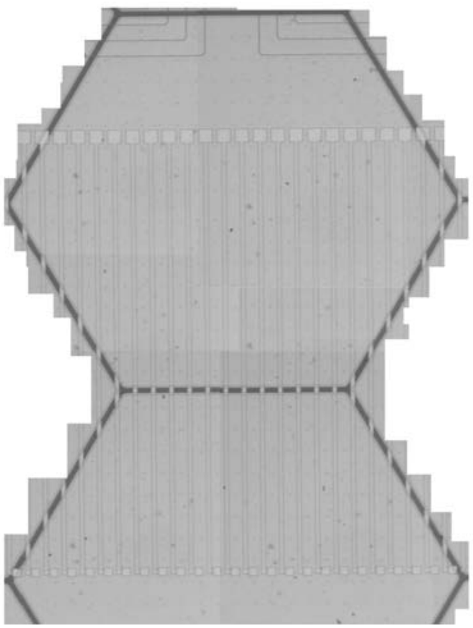
- Could lead to inefficiency late in the bunch train due to buffer overflow a.)



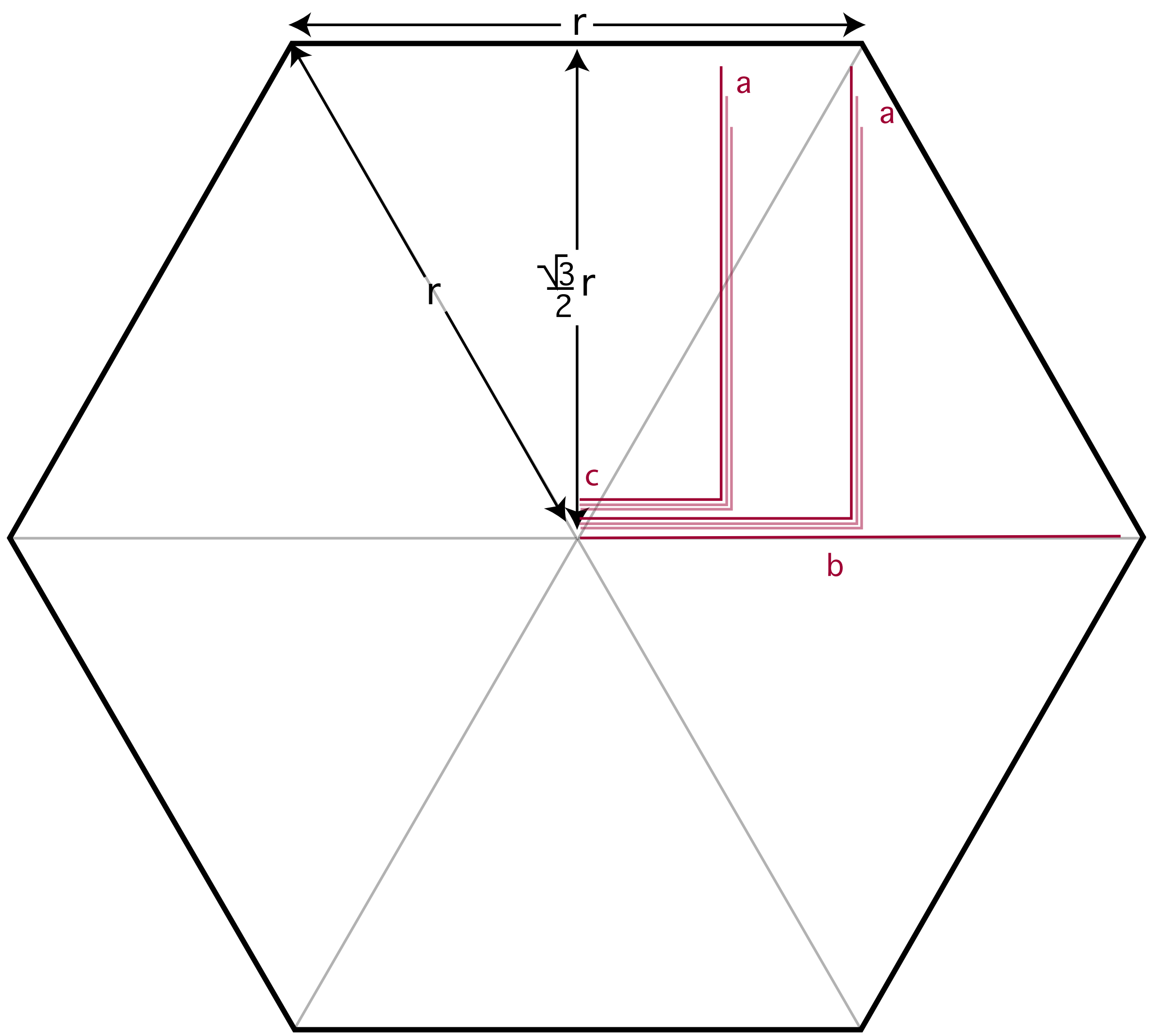
b.)



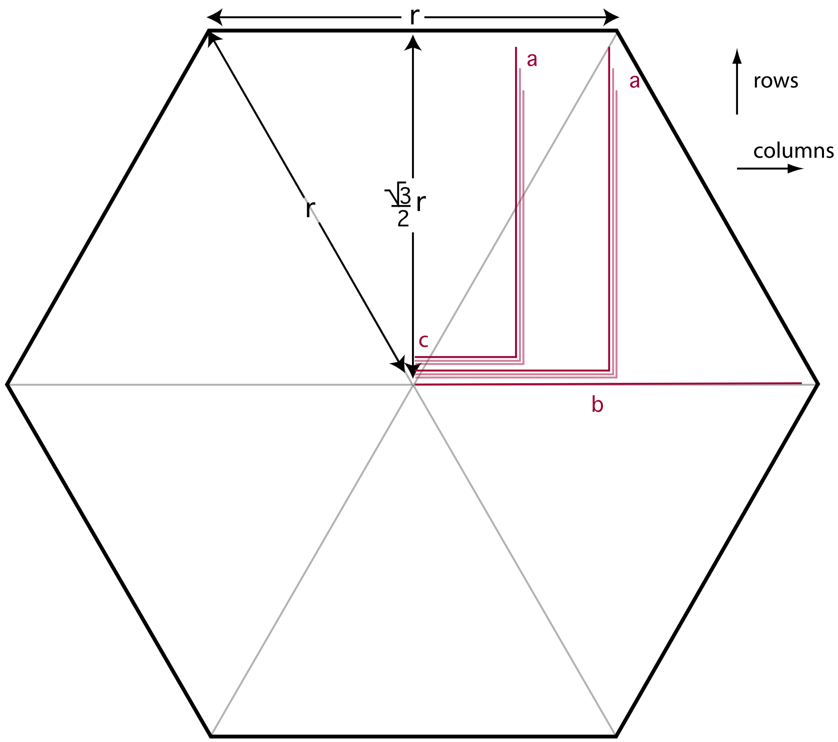
c.)

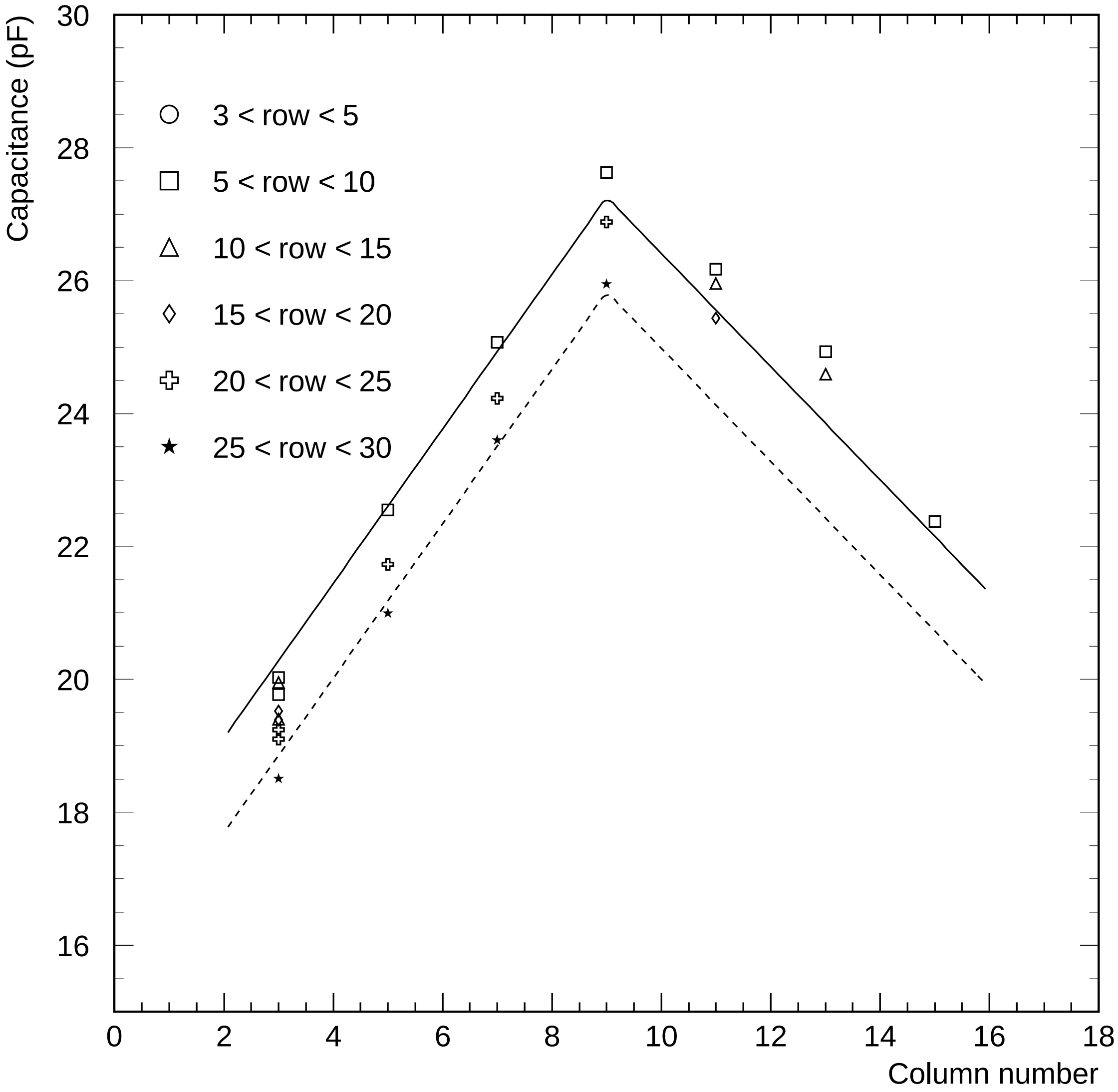


Examples of capacitances

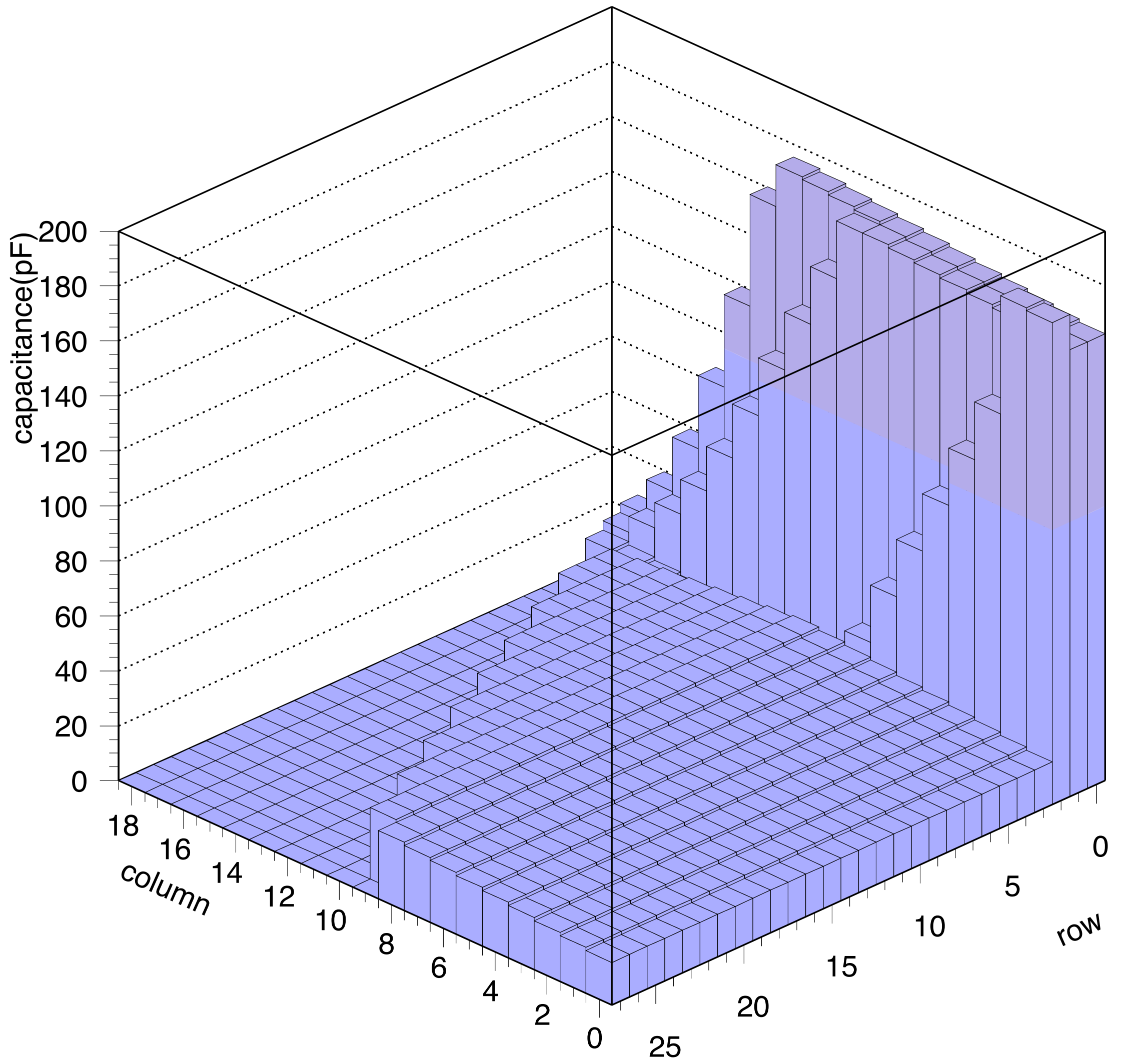


Note that all pixels in a given row have nearly the same capacitance:





A simple model is under development for use in Monte Carlo simulations:



(Over estimates capacitance in region b because of unused channels in the 32 $\times$ 32 channel array)

• For areas near the edge of the detector fundamental limit to noise is given by (for e.g. correlated double sampling)

$$ENC_{R_s} \sim C_{tot}\sqrt{4\frac{KT}{q_e^2}R_s\frac{1}{2\tau}}$$

where R_s is the series resistance, C_d and τ is the shaping time of the electronics.

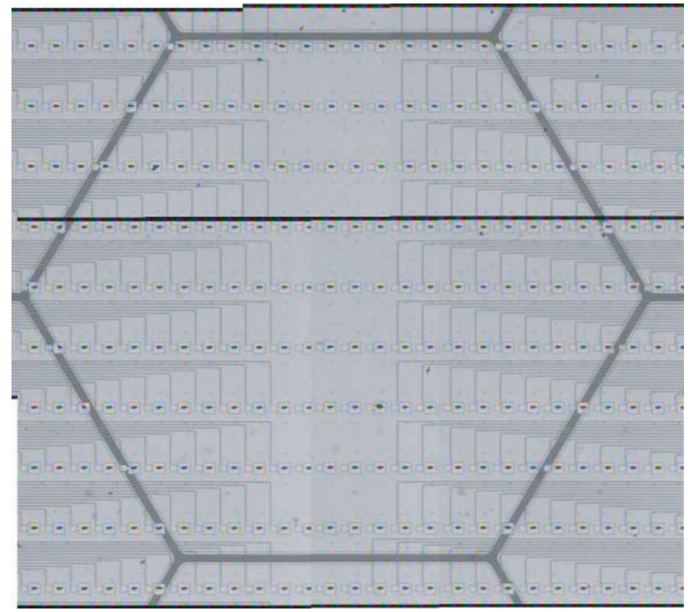
• For $\tau = 1\mu$s, $R_s = 580\,\Omega$ and $C_{tot} = 40\,$pF this gives ~600 electrons noise, which is not really a problem.

• We can slightly improve noise performance by decreasing the trace width, perhaps by a factor of 2, i.e.

$$ENC_{R_s} \propto \sqrt{w}$$

where w is the trace width.

• In region b, near the bump bonding array, we will have a large number of traces crossing a pixel. No series resistance, but amplifier FET noise similar:



Possible ways to decrease capacitance in region b:

• Move probing pads on to pixels.

• Decrease trace width in area near central pixels, here

$$ENC_{amp} \propto w$$

• Use a long skinny chip (e.g. 100 μm x 600 μm grid)

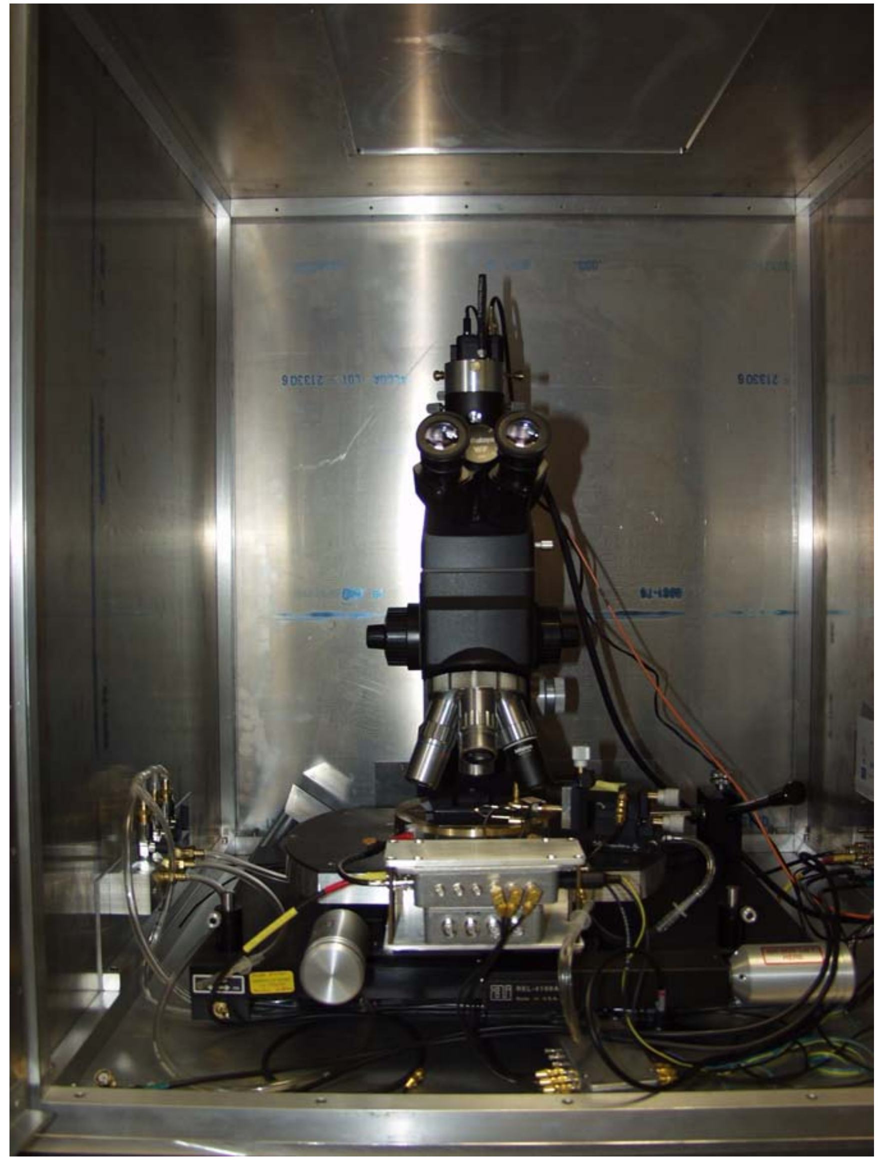
After these three measures, worst case capacitance is ~70 pF.

Test Setup for Cosmics, Sources and Laser

- Modified probe station, allows laser to be target on entire detector

- IR microscope objective used to focus laser to $\sim 10\,\mu$m spot

- Bias applied to backside of detector using insulated chuck



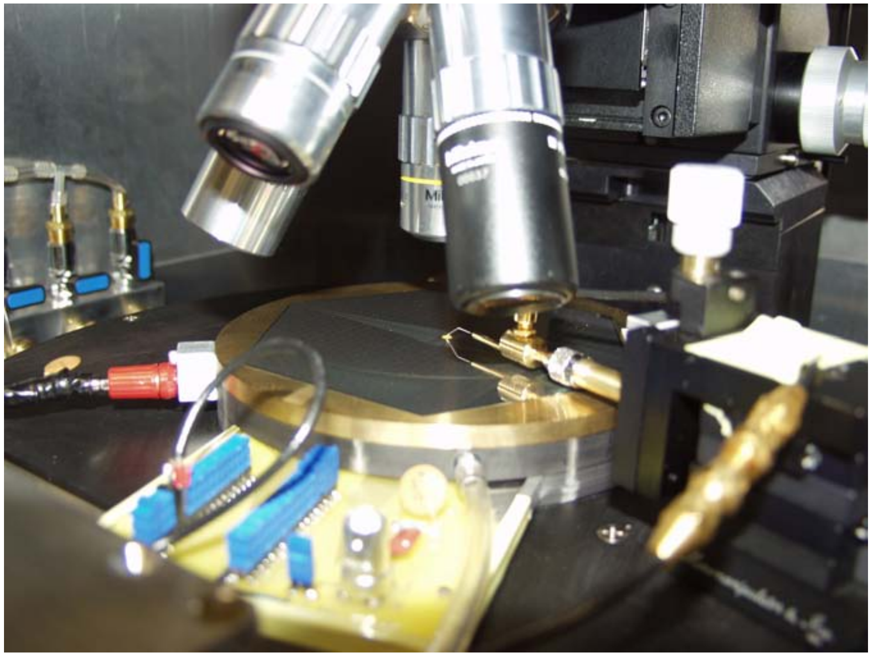
Test Setup – detector probing

- Contact made to test pads on bump bonding array using an AC probe

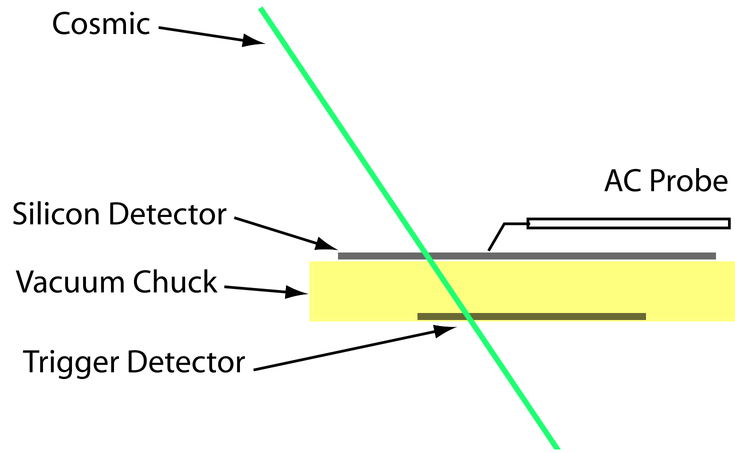
- Cables add $\sim$ 20 pF of additional capacitance, but noise performance is somewhat better than readout chip

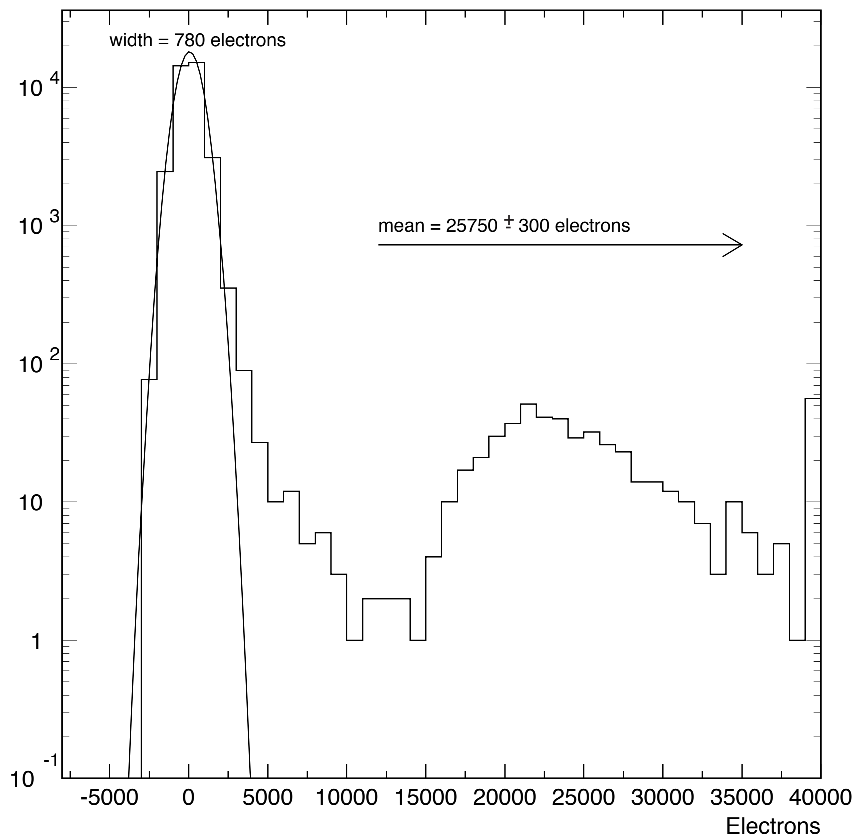
- Use AMPTEK 250F preamp, shapers with $\tau \simeq 1\mu$s and a digitizing oscilloscope to mockup expected electronics

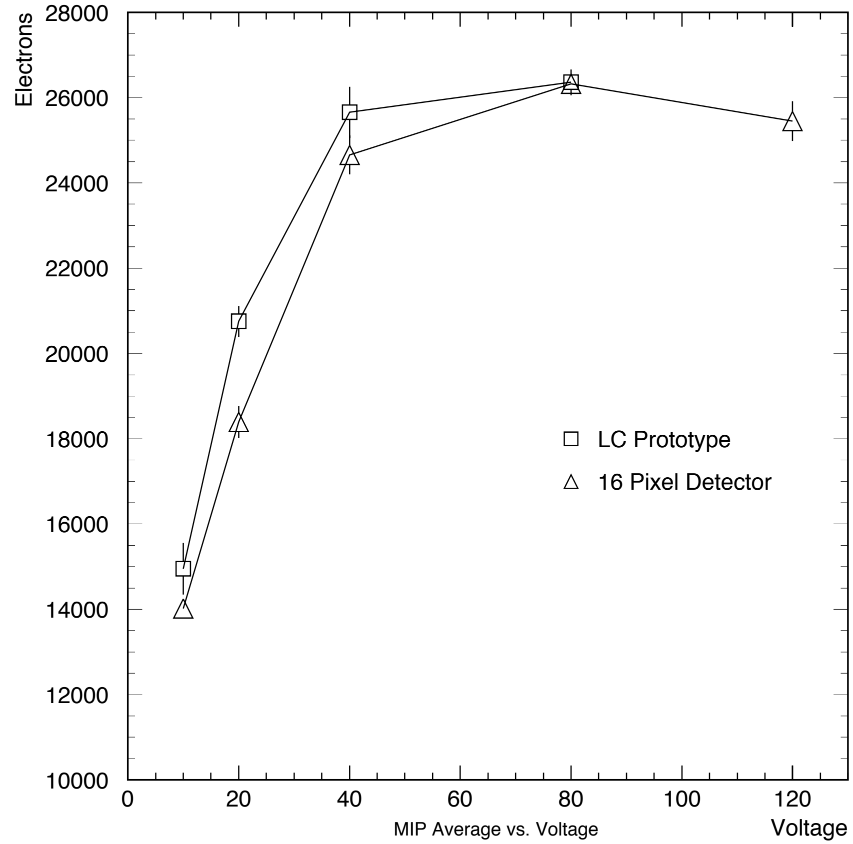
- PC board with 1 cm $\times$ 1 cm silicon pad detector used for cosmic trigger visible under chuck



Response of detectors to Cosmics
(Single 5mm pixel)
Simulate LC electronics
(noise somewhat better)

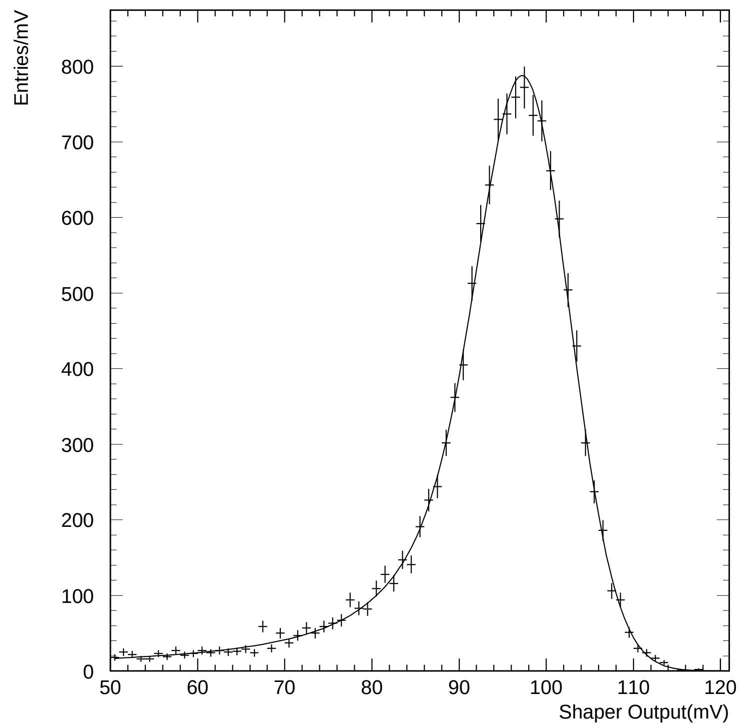






Errors do not include ∼ 10% calibration uncertainty (no source calibration)

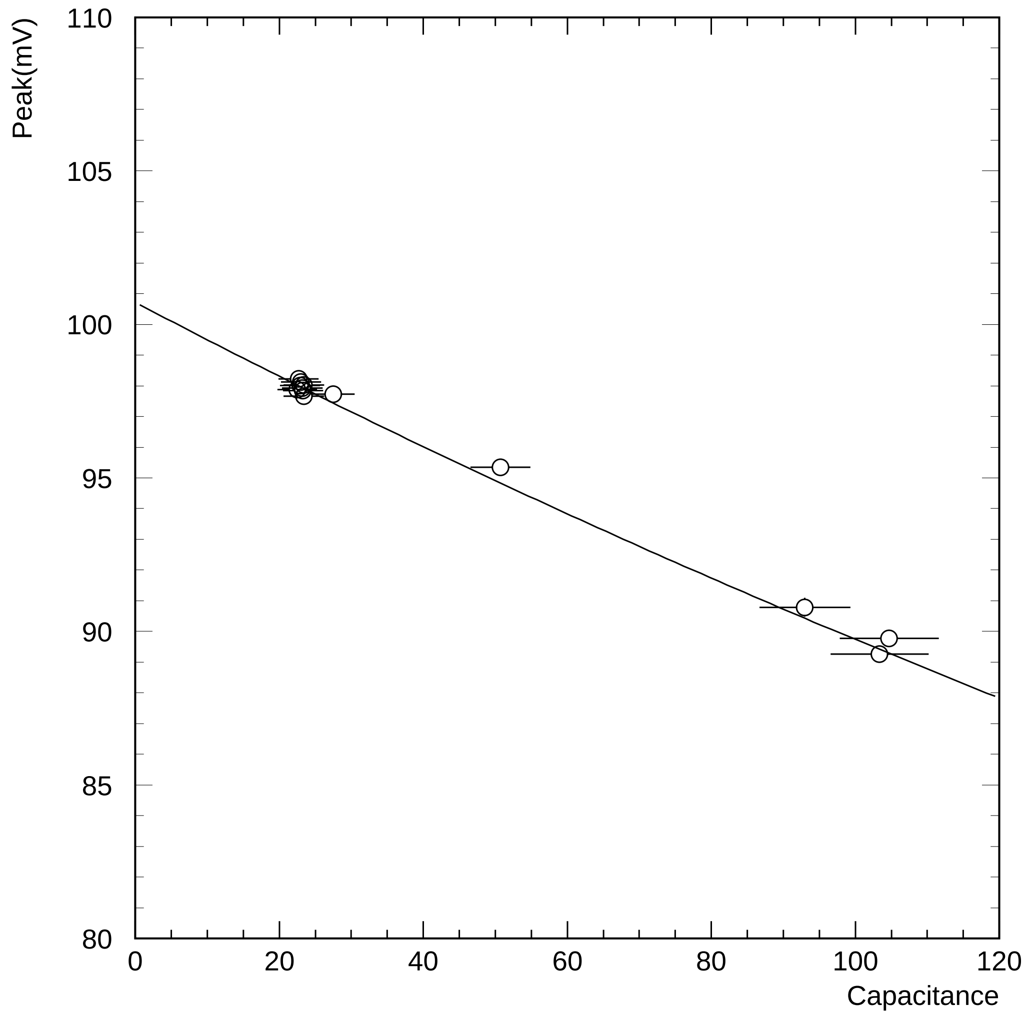
Response of Detectors to 60KeV Gamma's from Am^{241}



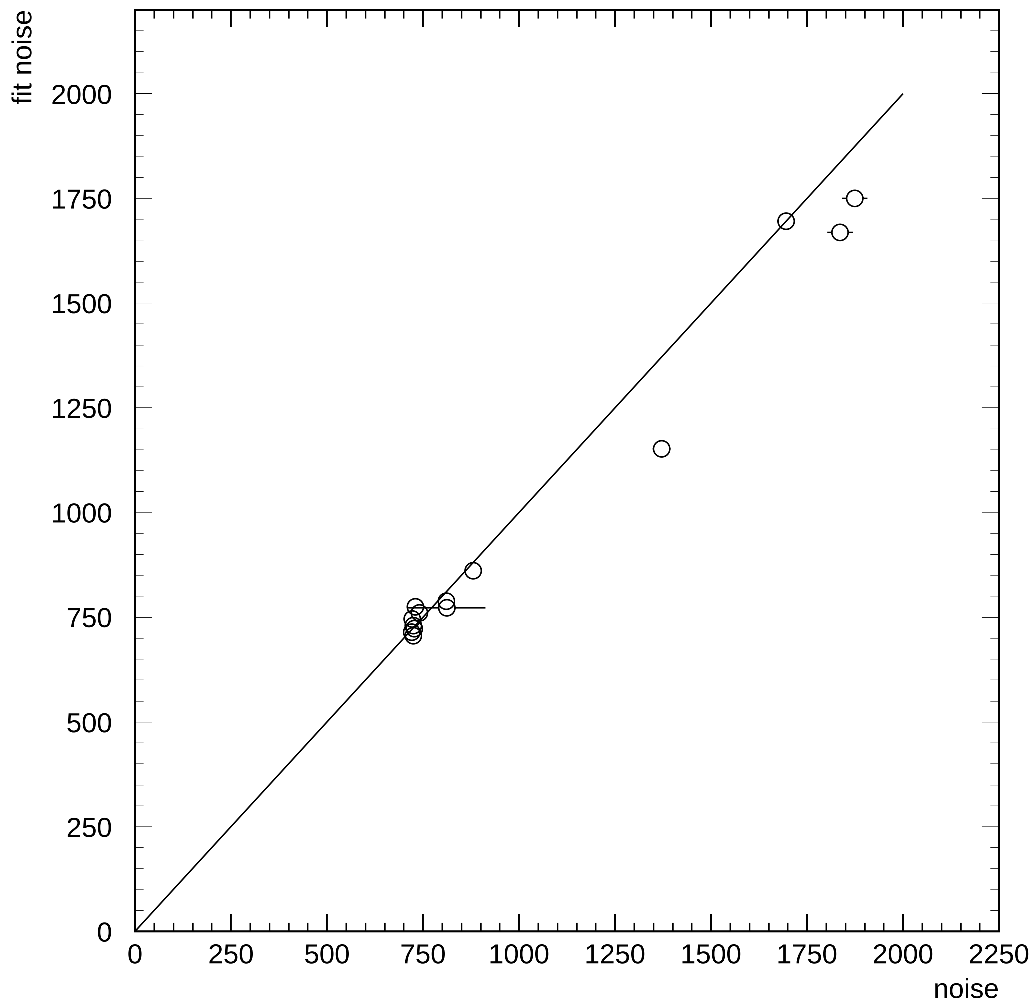
Possible $\sim$ 1% wafer-wafer calibration?

Width of distributions corresponds to $\sim$ 1000 electrons noise. Pixels under test are on outer edge of wafer – includes larger series resistance contribution than cosmic data.

Mean value versus capacitance



Slope is determined by "dynamic" capacitance of our laboratory electronics $C_{dyn} \sim 790$pF



Noise is consistent with expectation from capacitance and series resistance

Crosstalk

• **Positive** crosstalk is a function of the dynamic capacitance, C_{dyn} of the electronics and the typical trace–pixel capacitance C_{coup}, ideally

$$X_{talk} = \frac{C_{coup}}{C_{dyn}} << 1\%$$

(A few channels with parallel traces in region b will have larger cross talk)

• **Negative** crosstalk comes from finite bypass capacitance of bias side.

• With no bypass and all pixels depleted this would be $\frac{1}{1024}$
• In lab this ratio is about $\frac{1}{2000}$ for 10nF bypass capacitor

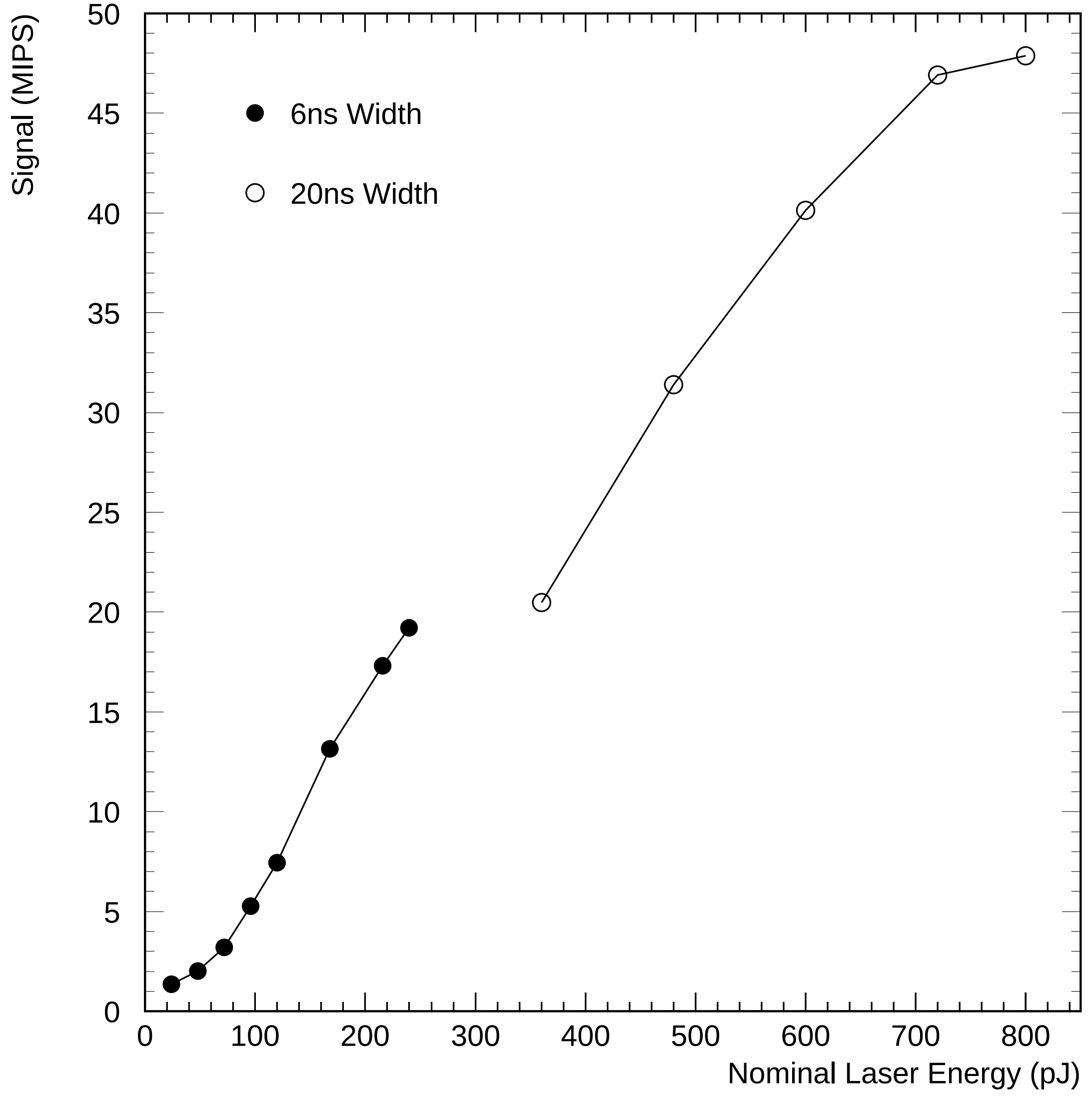
• All crosstalk observed with lab electronics is much below the 1% level – quantitative analysis underway.

Laser Studies

$\lambda = 1064\,\mathrm{nm}$

IR penetrates into wafer

Allows controlled study of large and small pulses



Conclusions

- A narrow gap silicon–tungsten detector for LC physics is attractive
- First round of prototype silicon detectors perform as expected
- Detectors can be produced with workable values of stray capacitance and series resistance
  $\Rightarrow$ some minor changes needed for cold design
- Detailed model of noise and crosstalk will shortly be available for Monte Carlo simulations

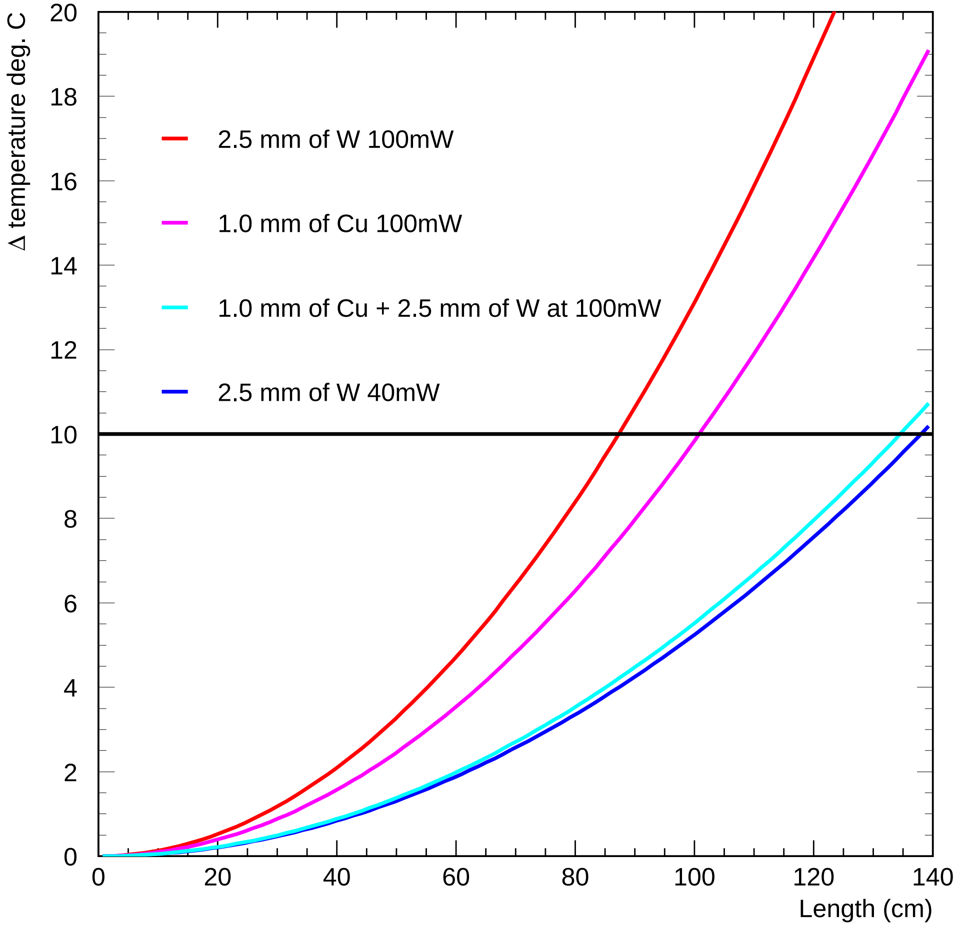
Backup

Can we get the heat out?

Back of the envelope calculation of change in temperature:

- Thermal Conductivity of W alloy 120W/(K-m)
- Thermal Conductivity of Cu 400W/(K-m)

Need to reduce heat to below 100mW/wafer.



Other more radical alternatives

- Polyimide (kapton) can be used instead of SiO_2 as insulator for traces
- Oxide thickness to 5μm possible.
- Minumum trace with probably 10μm
- Could reduce stray capacitances by a factor of 2 or more

Hamamatsu does not currently provide metal-on-polyimide products, but we could increase the thickness of the wafer and the SiO_2.

SINTEF (Norway) may be producing detectors based on 6 inch wafers with metal-on-polyimide within the next year. (Possible collaboration with Brookhaven to produce masks.)