DHCAL Prototype Construction

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Snowmass Workshop August 14 – 27, 2005

Digital Hadron Calorimeter

Fact Particle Flow Algorithms improve energy resolution compared to calorimeter measurement alone

Assumption Confusion term is the dominant contribution to jet energy resolution

Particles in jets	Fraction of energy	Measured with	Resolution [σ^2]
Charged	65 %	Tracker	Negligible
Photons	25 %	ECAL with 15%/√E	$0.07^2\ E_{jet}$
Neutral Hadrons	10 %	ECAL + HCAL with 50%/√E	$0.16^2\ E_{jet}$
Confusion	Required for 30%/√E		**$\leq 0.24^2\ E_{jet}$**

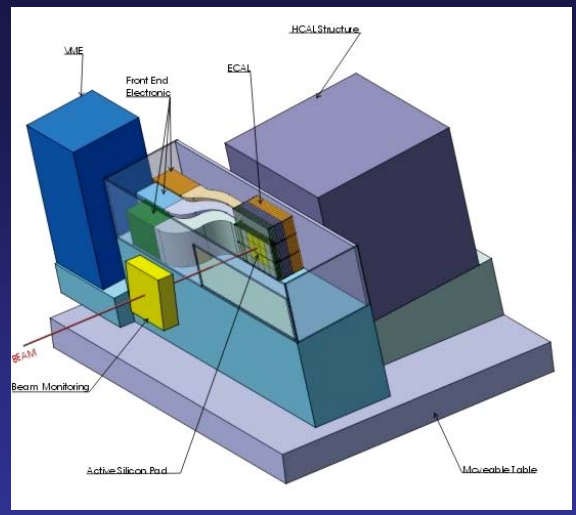
} 18%/√E

Minimize confusion term Maximize segmentation of calorimeter readout

High segmentation 1 – bit resolution on readout preserves energy resolution for hadrons

Technical implementation Resistive Plate Chambers (RPCs)
Gas Electron Multipliers (GEMs)

DHCAL R&D Goal



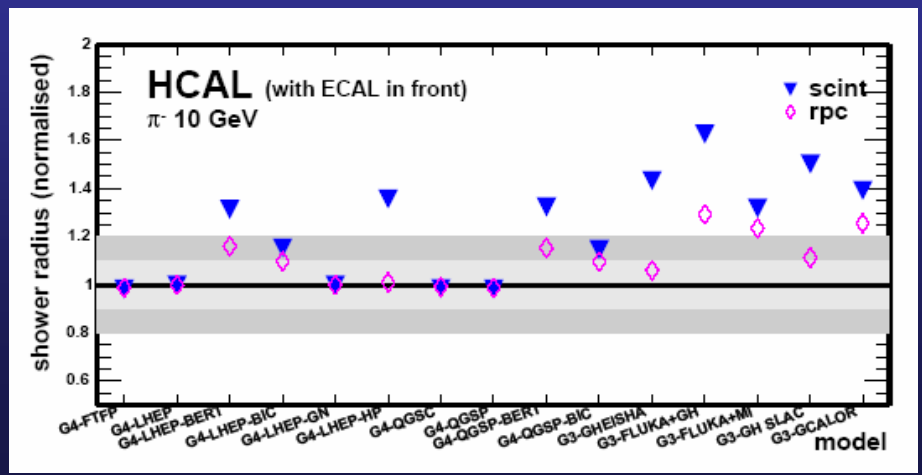
Prototype section

1 m^3 (to contain most of hadronic showers)
40 layers with 20 mm steel plates as absorber
Lateral readout segmentation: 1 cm^2
Longitudinal readout segmentation: layer-by-layer
Gas Electron Multipliers (GEMs) and Resistive Plate Chambers (RPCs) evaluated

Motivation for construction and beam tests

Validate RPC approach (technique and physics)
Validate concept of the electronic readout
Measure hadronic showers with unprecedented resolution
Validate MC simulation of hadronic showers
Compare with results from Analog HCAL

Comparison of hadron shower simulation codes by G Mavromanolakis



Choices for HCAL active media

	Scintillator	GEMs	RPCs
Technology	Proven (SiPM?)	Relatively new	Relatively old
Electronic readout	Analog (multi-bit) or Semi-digital (few-bit)	Digital (single-bit)	Digital (single-bit)
Thickness (total)	~ 8mm	~8 mm	~ 8 mm
Segmentation	3 x 3 cm^2	1 x 1 cm^2	1 x 1 cm^2
Pad multiplicity for MIPs	Small cross talk	Measured at 1.27	Measured at 1.6
Sensitivity to neutrons (low energy)	Yes	Negligible	Negligible
Recharging time	Fast	Fast?	Slow (20 ms/cm^2)
Reliability	Proven	Sensitive	Proven (glass)
Calibration	Challenge	Depends on efficiency	Not a concern (high efficiency)
Assembly	Labor intensive	Relatively straight forward	Simple
Cost	Not cheap (SiPM?)	Expensive foils	Cheap

?

Entries in ▭ are concerns/possible problems/limitations

Status of DHCAL Active Detectors

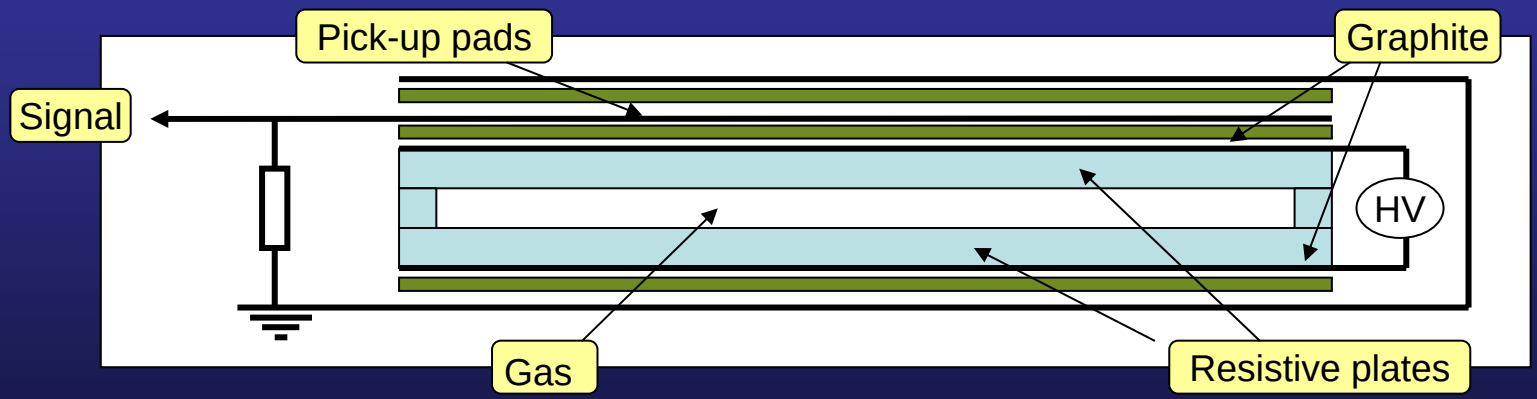
Measurement	RPC Russia	RPC US	GEM
Signal characterization	yes	yes	yes
HV dependence	yes	yes	ongoing
Single pad efficiencies	yes	yes	yes
Geometrical efficiency	yes	yes	no
Tests with different gases	yes	yes	yes
Mechanical properties	?	yes	no
Multipad efficiencies	yes	yes	ongoing
Hit multiplicities	yes	yes	yes
Noise rates	yes	yes	ongoing
Rate capability	yes	yes	no
Tests in 5 T field	yes	no	no
Tests in particle beams	yes	planned	planned
Long term tests	ongoing	ongoing	ongoing
Design of larger chamber	yes	ongoing	ongoing

Virtually all R&D completed

Catching up

Default RPC chamber designs

Layer	Russia	US
Resistive layer anode	Anode readout pads	1÷50 MΩ/□
Glass thickness in [mm]	0.55	1.1
Gas gap in [mm]	1.2	1.2
Glass thickness in [mm]	0.85	1.1
Resistive layer cathode	~1 MΩ/□	1÷50 MΩ/□



Electronic Readout System for Prototype Section

400,000 readout channels

Conceptual Design of Readout System

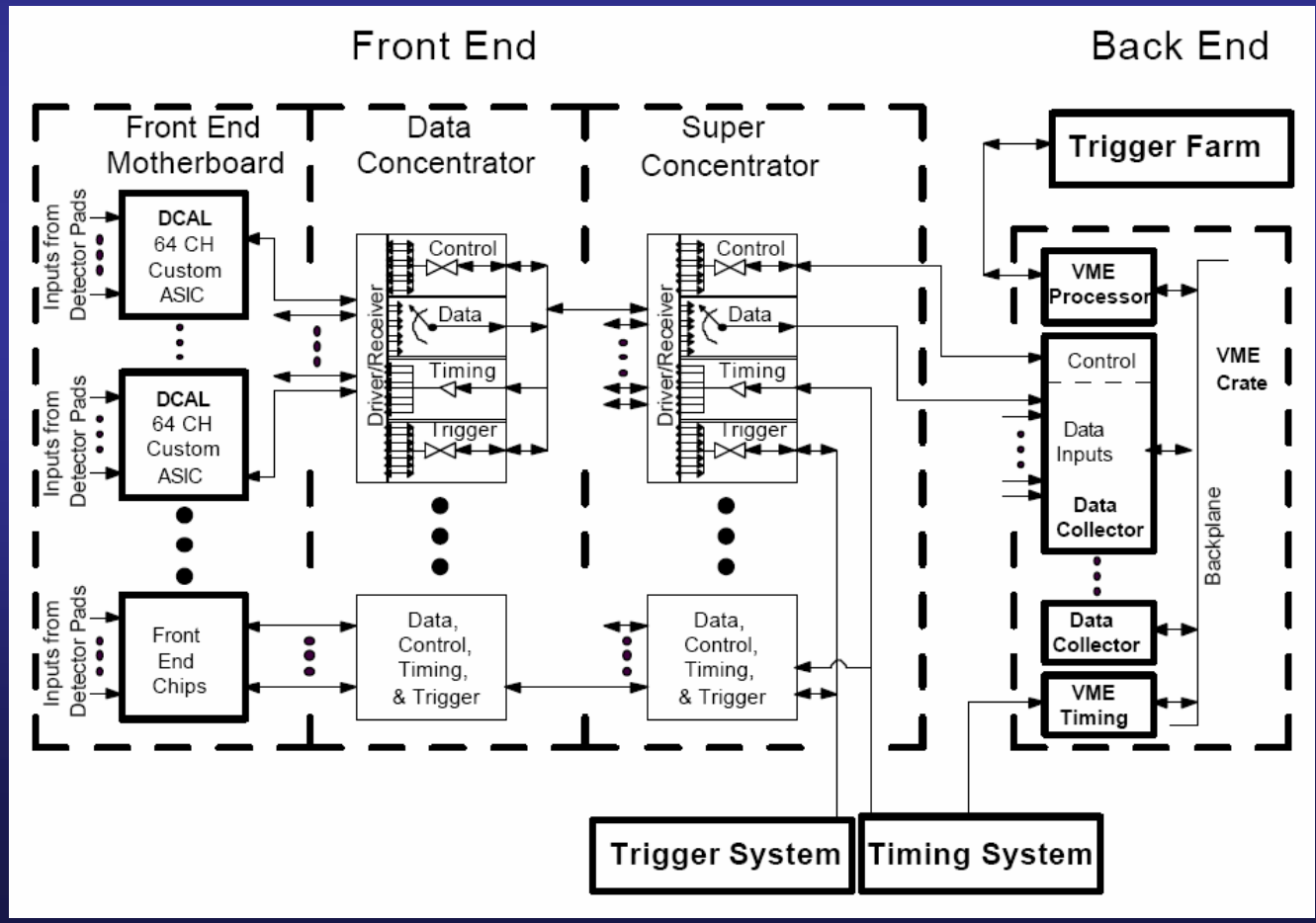
I Front-end ASIC and motherboard

II Data concentrator

III Super Concentrator

IV VME data collection

V Trigger and timing system



Specification of system

Document almost ready

To be released later this month

Contains all details of system

Basis for design work
Currently 57 pages

Document written by Gary Drake

Conceptual Design of the Readout System for the Linear Collider Digital HCAL Prototype Detector

John Dawson, Gary Drake, José Repond, Lei Xia
Argonne National Laboratory

John Butler, Menakshi Narain
Boston University

Jim Hoff, Abder Mekonani, Raymond Yarema
Fermi National Accelerator Laboratory

Edwin Nobeck, Yasar Onel
University of Iowa

Andy White, Jaehoon Yu
University of Texas - Arlington

Version 1.10
July 25, 2005

Multiplexing

Component	#/chamber	#/plane	#/channels/unit	Total # of units
Planes	0.333	1	9216	40
Chambers	1	3	3072	120
DCAL ASIC	24	144	**64**	5760
FE motherboards	2	6	1536	240
Data concentrators	4	12	**768**	480
Super concentrators	0.667	2	**4608**	80
Data collectors	-	0.166	**55,296**	7
VEM crates	-		**387,072**	1

Common development for RPC and GEM based Digital Hadron Calorimeter

Parameter	RPCs	GEMS
Type	Avalanche	(Gas)
Geometry	1cm x 1 cm Pads	1 cm x 1 cm Pads
Capacitance	10-100 pF	10-100 pF
Smallest Signal	~100 fC	~5 fC
Pulse Width	~5 nS	~3 nS
Rise Time	~2 nS	?
Largest Signal	~10 pC	~100 fC
Noise Rates	~0.1 Hz	?
Env. Noise Susceptibility	Low	Low

Front-end ASIC…

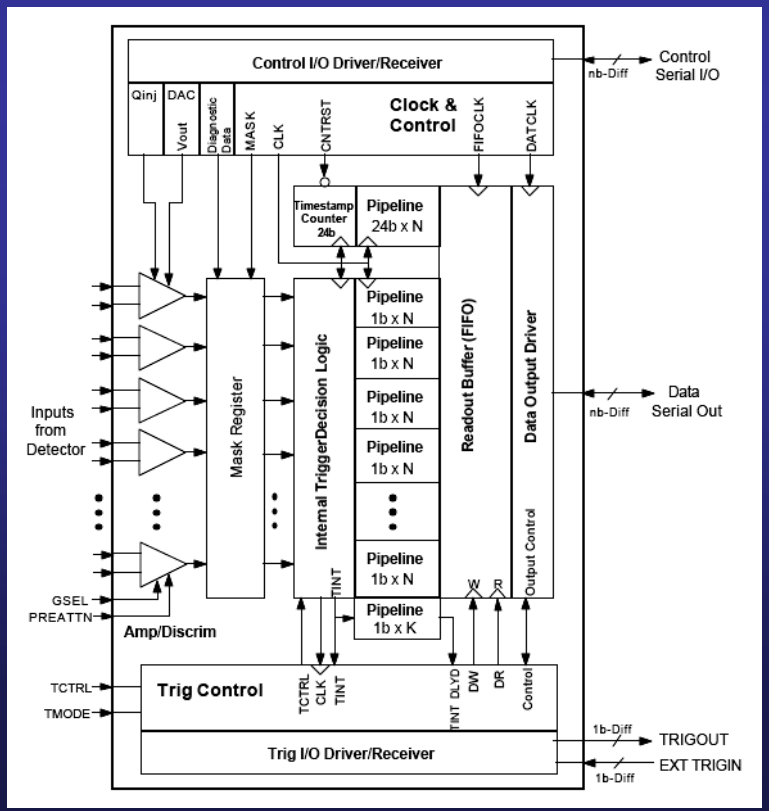
64 inputs with choice of input gains

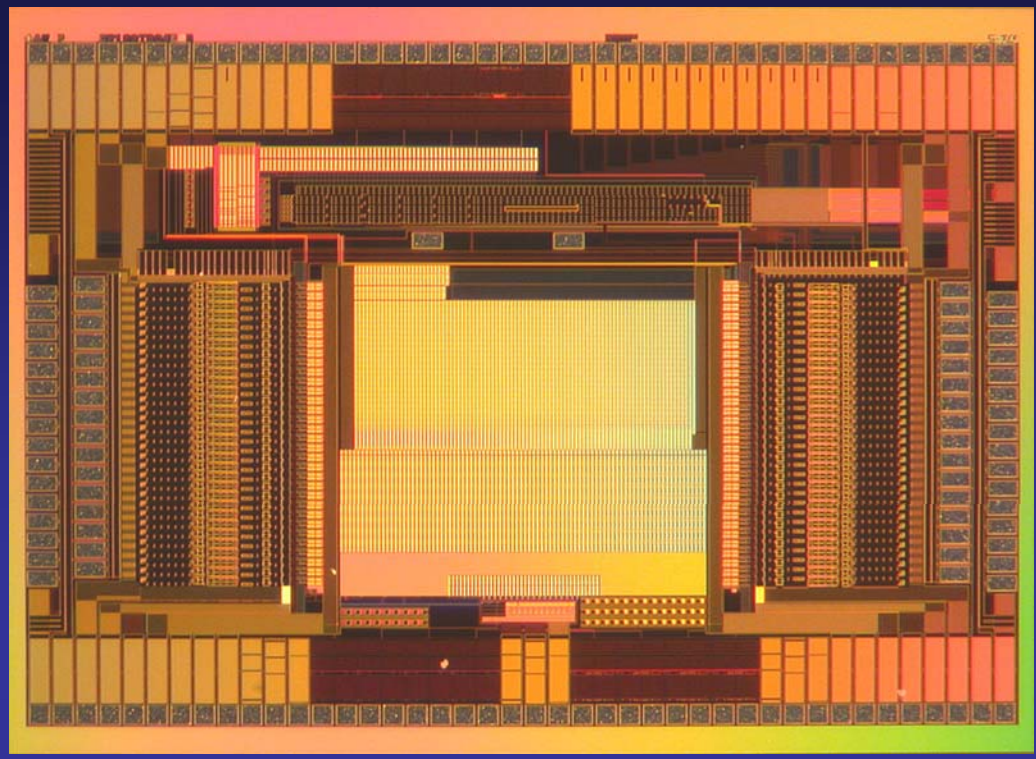
RPCs (streamer and avalanche), GEMs…

Triggerless or triggered operation

100 ns clock cycle

Output: hit pattern and time stamp





Design work at FNAL

Abderrezak Mekkaoui
James Hoff
Ray Yarema

Design work started in June, 2004

Prototype run submitted on March 18th 2005

40 unpackaged chips in hand

Tests started: so far looks good

Cooling…

Chip consumes about 300 mW (measured)

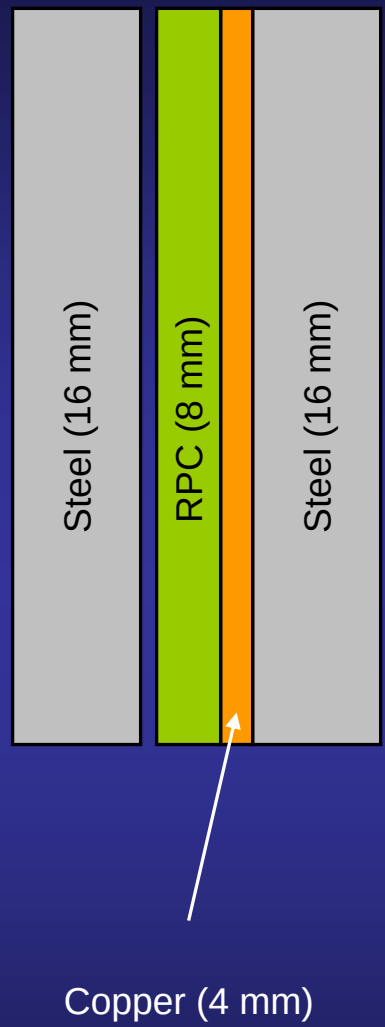
144 chips/plane → 50 W/plane

Thermal conductivity of steel not sufficient to dispose of heat

Copper factor of 10 better than steel

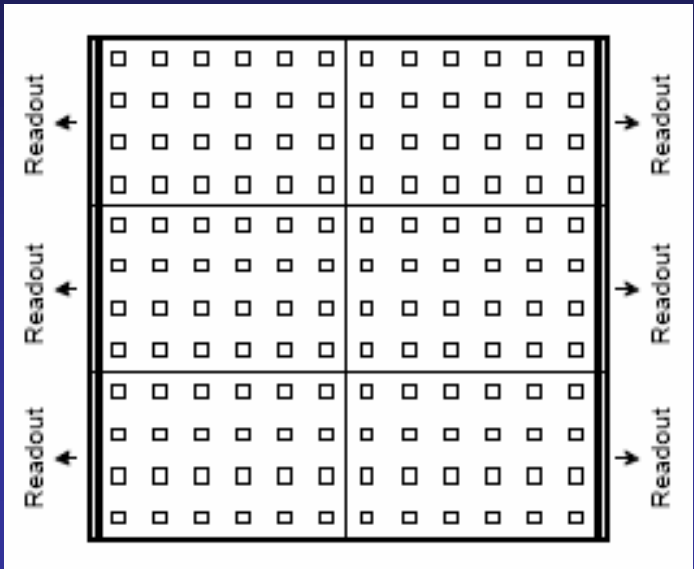
Consider replacing 4 mm support plates with copper plates

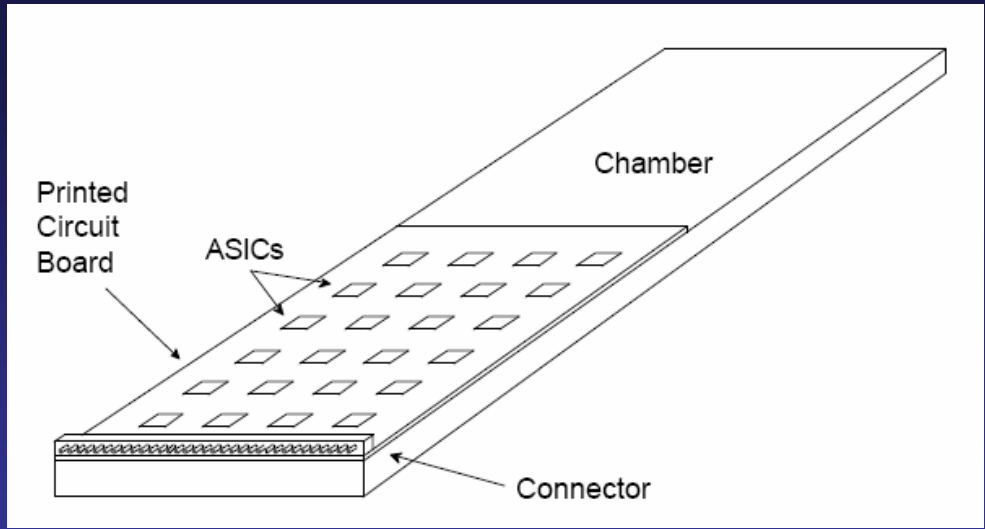
Cost?
Magnetic properties not relevant for testbeam
Properties for EM and HAD showers similar



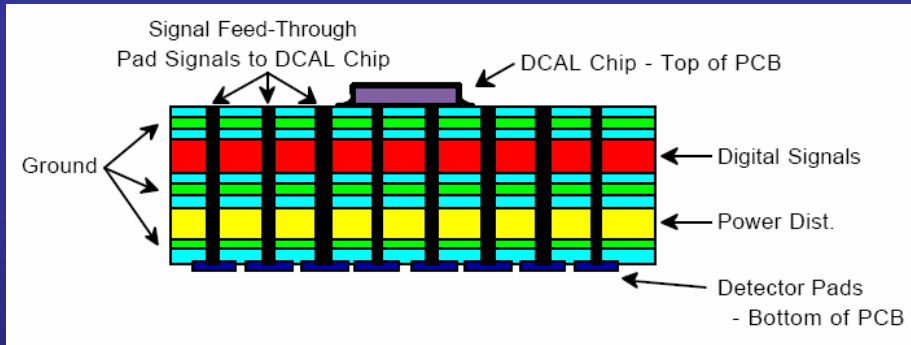
Material	A/Z	λ_I [cm]	X_0 [cm]	λ_I/X_0	$t_{passive} \equiv 4\lambda_I$ [cm]	Number of layers	t_{active}/ layer [mm]
Fe	56/26	16.8	1.8	9.3	67	38	8.7
Cu	64/29	15.1	1.4	10.8	42	60	9.5

Front-end boards…





2 boards/chamber or 6 boards/plane
8 layer boards
Overall thickness < 3 mm



Functionality

Houses ASICs (24)
Provides readout pads for RPCs
Routes signals to ASICs
Distributes power and ground to ASICs
Distributes clocks and control signals to ASCIs
Routes output signals (LVDS) to receivers

} Analog signals

} Slow control

} Digital signals

Design challenge

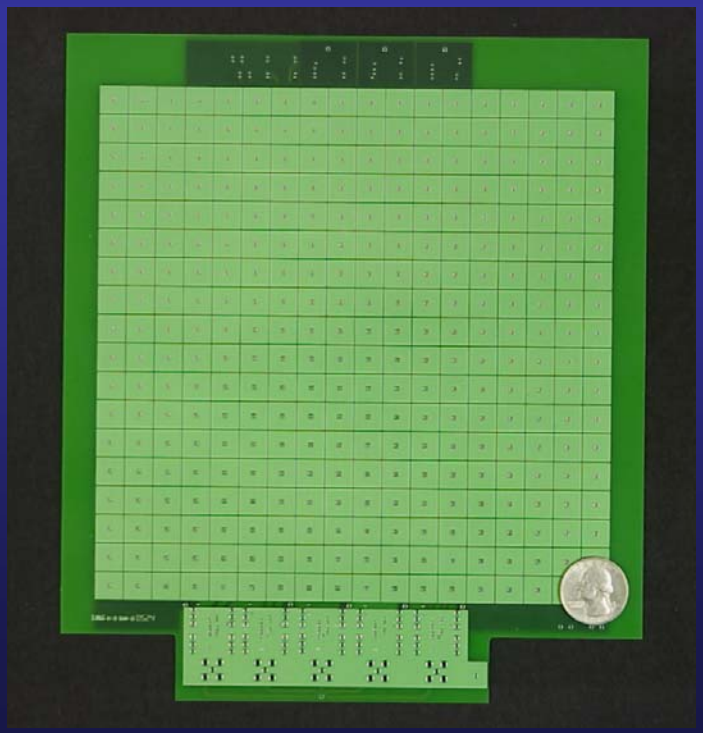
Digital → analog crosstalk…

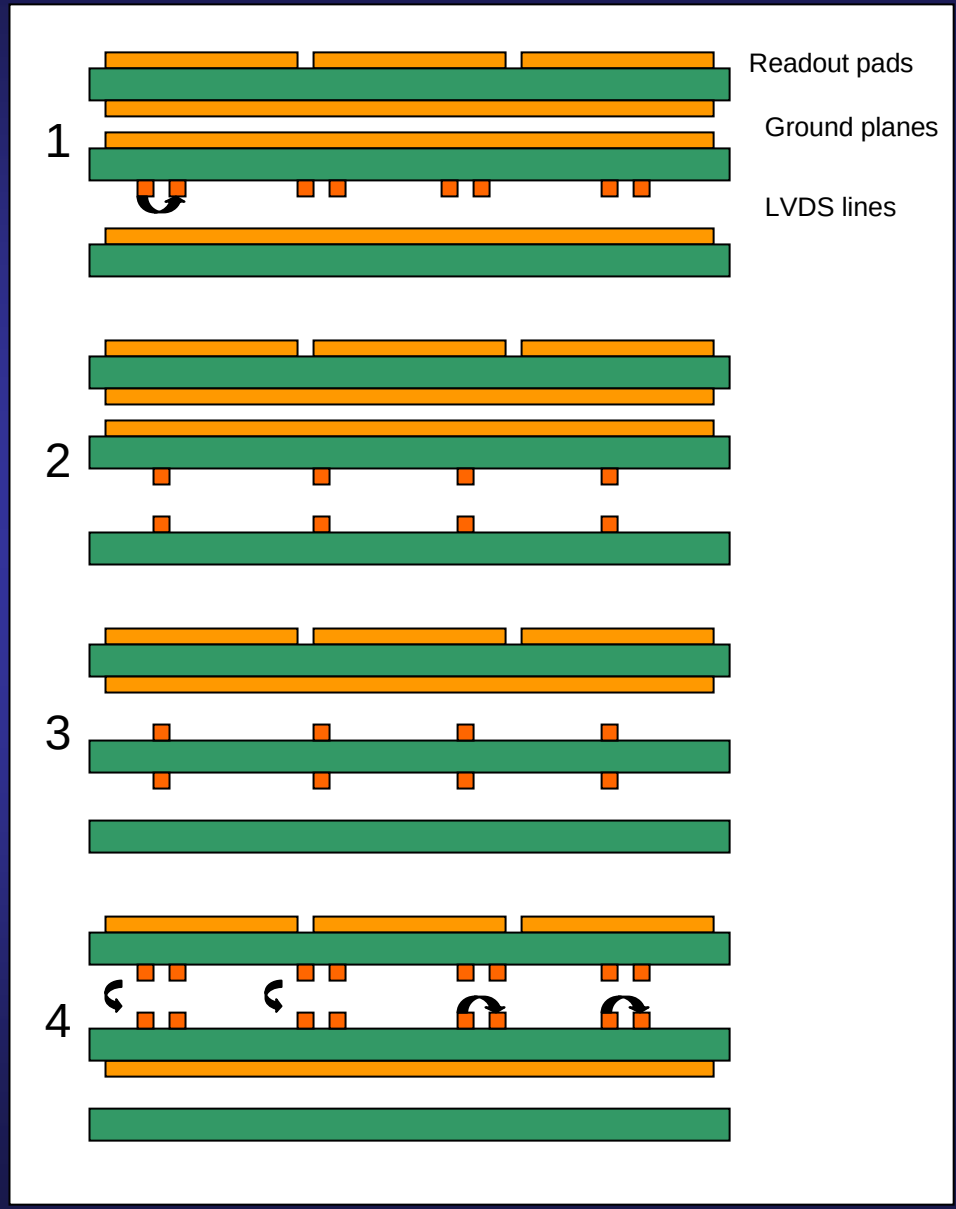
Measurements with test board

LVDS signals routed close to pads

- 4 different configurations
- Each with 4 different distances to the center of the pads

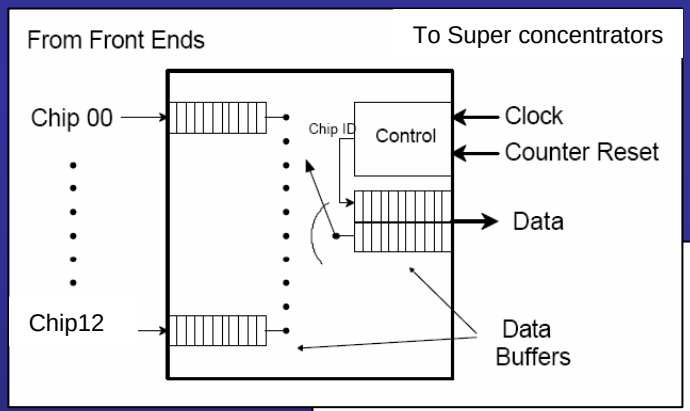
First results encouraging, more tests needed…

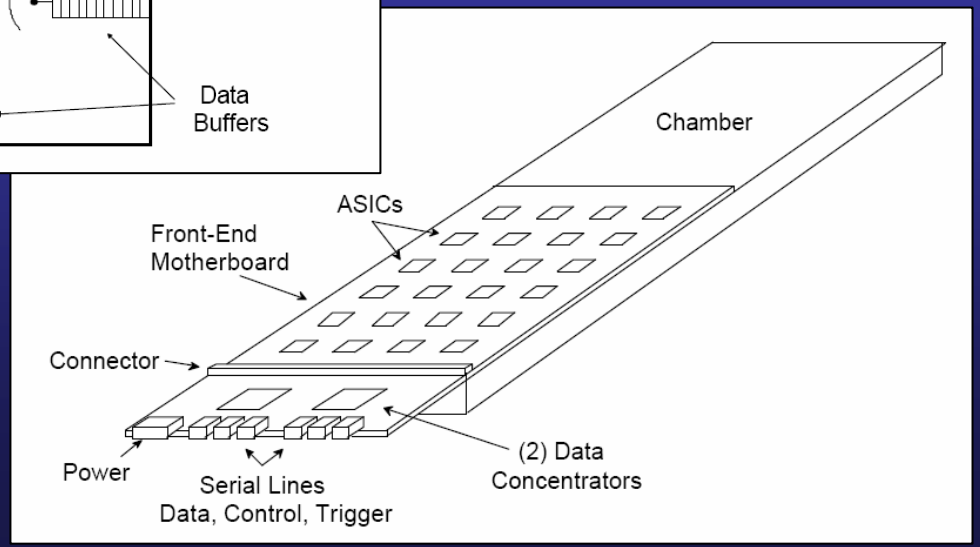


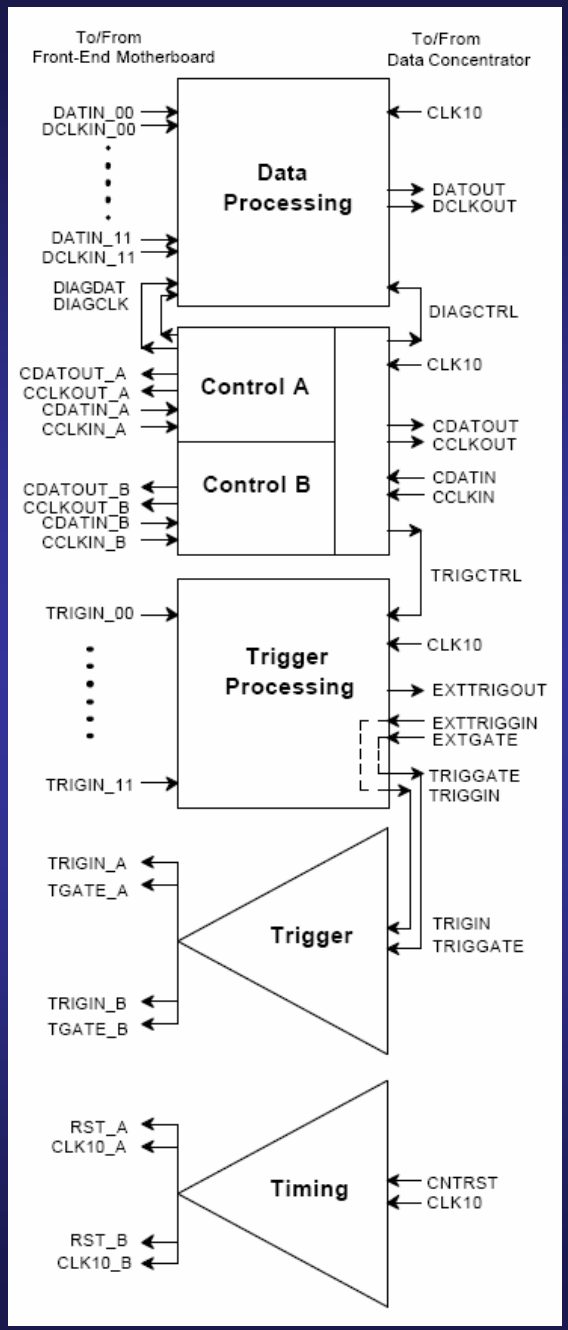


Data concentrators…

Read out 12 ASICs (serial lines)
Located on sides of section
Can buffer events
Distribution of trigger and timing
(bus connection)
Essentially FPGAs
All transmissions in LVDS







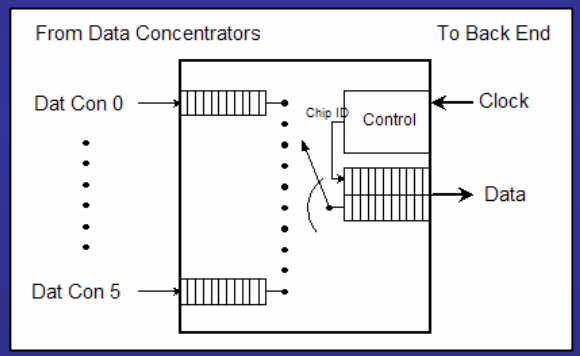
Super concentrators…

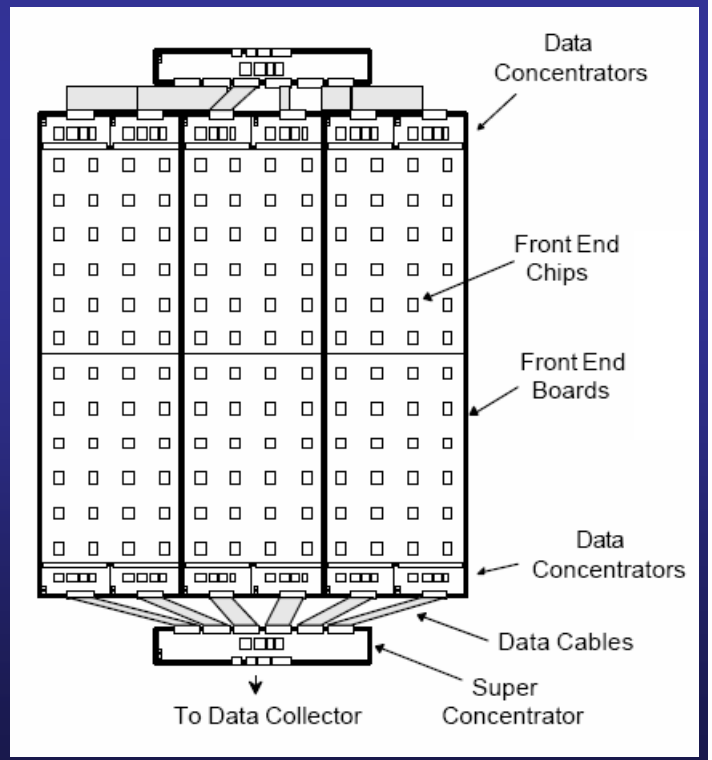
Introduced by urge to reduce cost (VME)

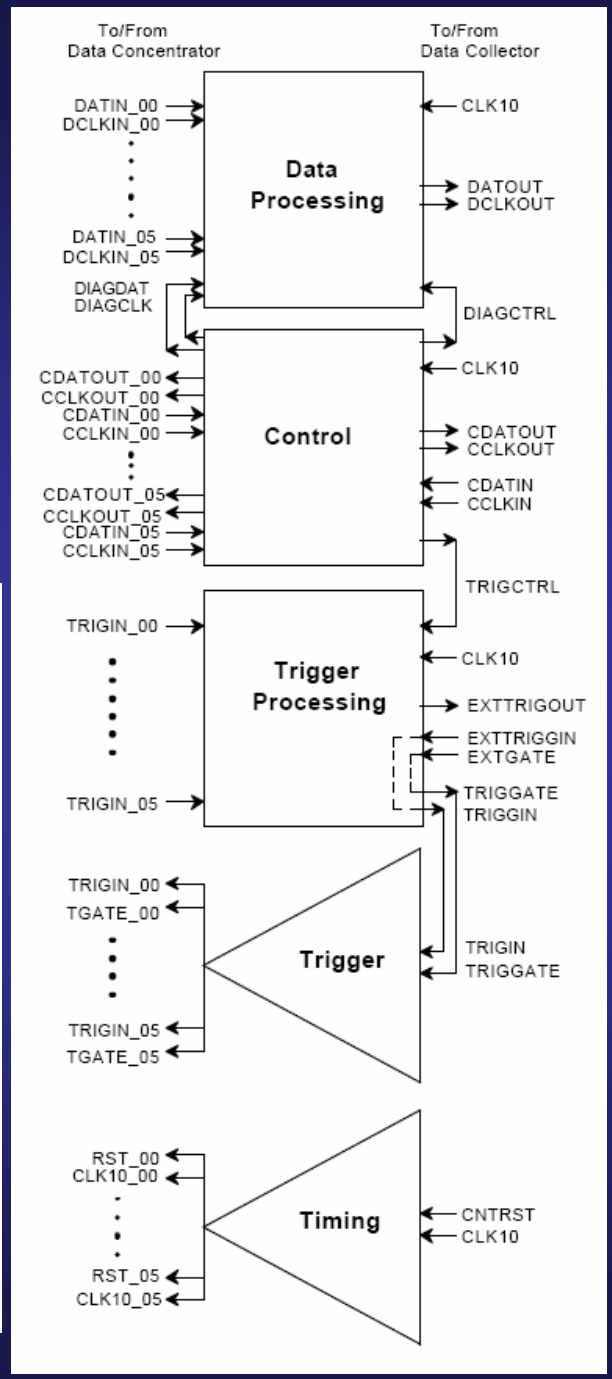
Reads out 6 data concentrators

Located on side of module

Similar design to data concentrator





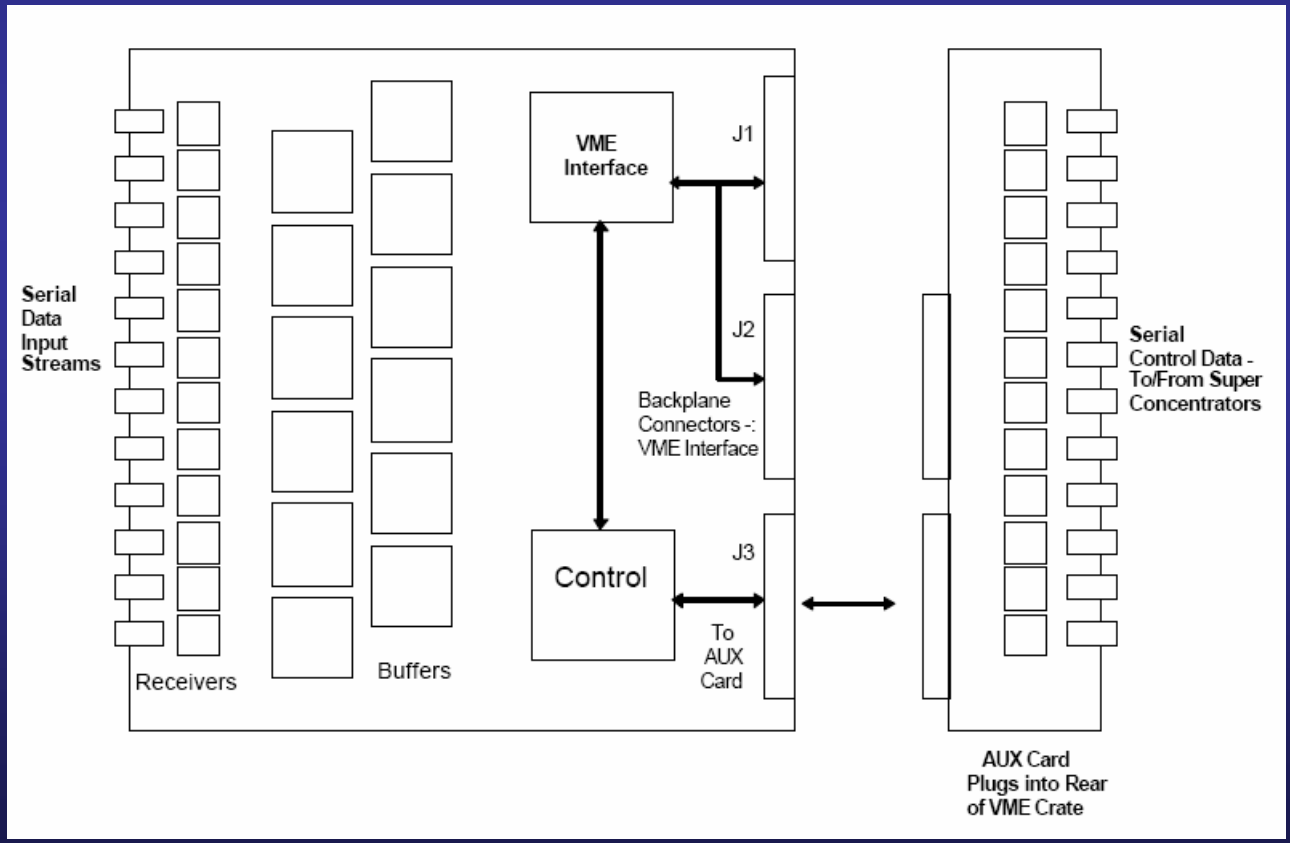


Data collector…

VME based system

Each card reads out 12 super concentrators

Need only 7 cards and 1 VME crate



Work by Lei Xia

Study of rates…

Simulation of response of 1 m^3 prototype section to 50 GeV π^+

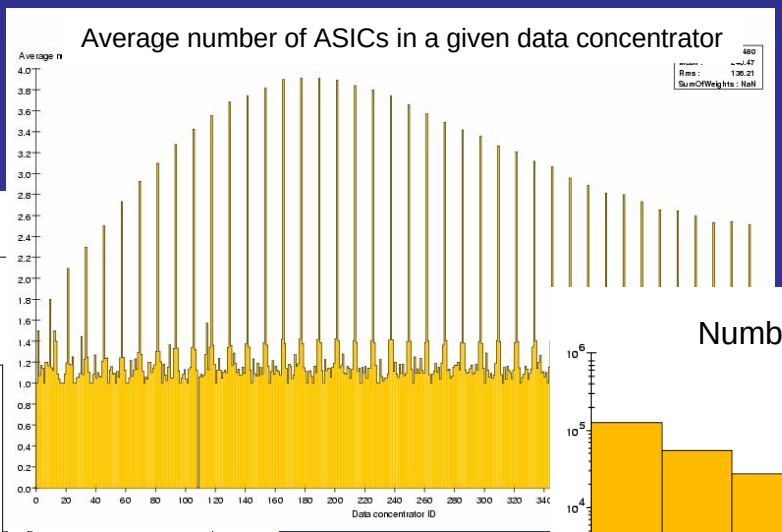
Study of number of data rates in different components of readout system

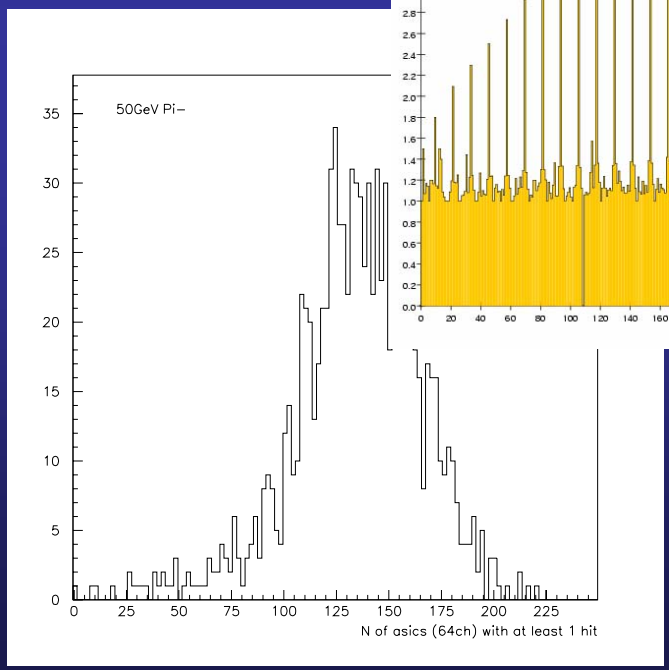
System capable of handling ~10x more data than expected

Examples…

Readout speed 10 Mb/sec

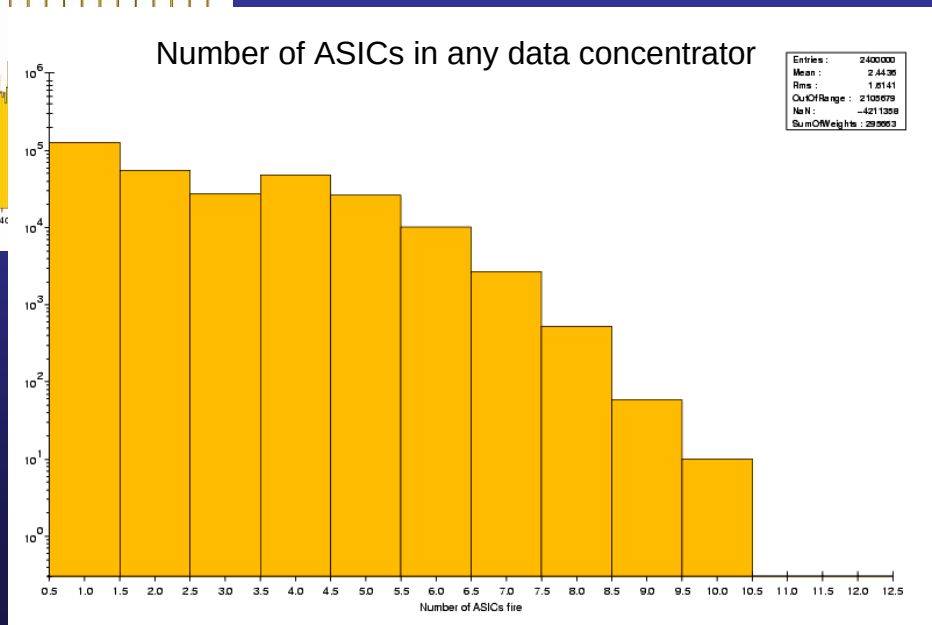
Average number of ASICs in a given data concentrator





Number of ASICs in a given event

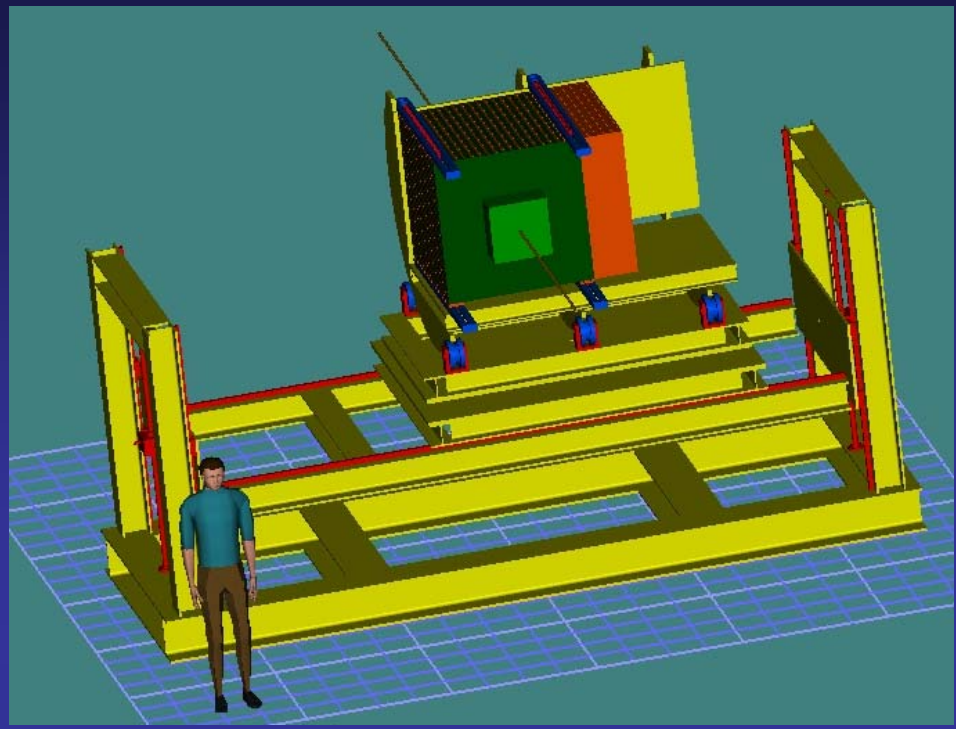
Number of ASICs in any data concentrator



List of electronics subtasks

1	Overall engineering and design	**ANL**
2	ASIC engineering and design	**FNAL**
3	ASIC testing Test board design Test board production Measurements	ANL **FNAL**
4	Front-end PC board engineering and design prototyping and testing	**ANL** **FNAL**
5	Data concentrator engineering and design prototyping and testing	ANL Chicago
6	Data super concentrator engineering and design prototyping and testing	ANL Chicago
7	Data collector engineering and design prototyping and testing	ANL Boston
8	DAQ system: VME processor and programming	**Washington**
9	Timing and trigger system engineering and design prototyping and testing	**UTA**
10	High voltage system	**Iowa**
11	Gas mixing and distribution system	**Iowa**

Mechanical Structure



CALICE builds versatile structure

Absorber 20 mm **Steel** → 1 X_0 sampling
40 layers → 4 λ_I at 90^0

Recent simulation studies indicate that Tungsten with

Thickness of 0.7 cm → 2 X_0 sampling
58 layers → 4 λ_I at 90^0

might result in better PFA performance and safe cost

Questions

a) Do we need to test a Tungsten prototype
b) If yes, can we re-use the CALICE structure
c) What is the optimum sampling depth for W

Cost estimate (M&S only)…

Item	Cost
Resistive Plate Chambers	$20,000
Front-End ASIC	$225,000
Front-end Readout Boards	$50,000
Data Concentrator Boards	$85,000
Data Collector System	$60,000
Power Supplies, Optical Fibers, HV…	$60,000
Grand total	

$200,500

Not yet updated to reflect latest developments

$500,000 + 50% contingency

Item	Cost
GEMs	$200,000
Front-End ASIC	$75,000
Front-end Readout Boards	$50,000
Remaining systems from RPCs	$0
Additional for GEMs	

$325,000 + 50% contingency

Recent Proposals to Funding Agencies…

Agency	Institutes	Request	Award
LDRD (ANL directorate) used for manpower mostly	ANL	400,000	?
LCRD (DOE)	ANL, Boston, Chicago, Iowa	105,000	38,000
LCRD (DOE)	UTA, Washington	105,170	35,500
U of C Collaborative Grants	ANL, Chicago	100,000	0
US-Japan	ANL (LBNL, Oregon, SLAC…)	50,000	0
MRI 3 calorimeter prototypes	ANL, Oregon, UTA	964,000	0

Time scales

2005	Russia	Equip 1 m^2 with Minsk-based readout (32 x32 channels)
	US	Develop and test design of larger chambers
	GEMs	Cosmic ray studies with stacks of GEMs
	GEMs	Initiate long foil production and testing
	US	Prototype ASICs: finalize design
	US	Specify remainder of readout system (released soon)
	US	Design and prototype all subsystems
2006		Produce chambers
		Produce ASICs
		Produce other subsystems
2007		Move to test beam
		Take data
2008		Take data
		Design LC hadron calorimeter

Only possible if funded

Tune Hadron Simulation