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Development of the Continuous Acquisition Pixel (CAP) sensor for High Luminosity Lepton Colliders

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A future higher luminosity B-factory detector and concept study detectors for the planned International Linear Collider require precision vertex reconstruction while coping with high track densities and radiation exposures. Compared with current silicon strip and hybrid pixels, a significant reduction in the overall detector material thickness is needed to achieve the desired vertex resolution. Considerable progress in the development of thin CMOS-based Monolithic Active Pixel Sensors (MAPS) in recent years makes them a viable technology option and feasibility studies are being actively pursued. The most serious concerns are their radiation hardness and their readout speed. To address these, several prototypes denoted as the Continuous Acquisition Pixel (CAP) sensors have been developed and tested. The latest of the CAP sensor prototypes is CAP3, designed in the TSMC 0.25μm process with a 5-deep Correlated Double Sample (CDS) pair pipeline in each pixel. A setup with several CAP3 sensors is under evaluation to assess the performance of a full scale pixel read-out system running at realistic read-out speed. Given the similarity in the occupancy numbers and hit throughput requirements, per unit area, between a Belle vertex detector upgrade and the requirements for a future ILC pixel detector, this effort can be considered a small-scale functioning prototype for such a future system.

1. INTRODUCTION

It has long been known that the vertexing performance of a silicon tracker could be improved by incorporating a fine granularity pixel detector in its innermost layer. Hybrid pixel detectors are the baseline for the experiments [1] under construction at the LHC collider at CERN. Their technology is well established and they provide a detector with high rate handling capability and pixel level hit treatment. In the case of a B-factory, where the tracks have relatively low momenta and the resolution is limited by multiple scattering, preliminary studies [2] indicated that the most important aspects to improve the resolution are moving the vertex detector as close to the interaction point (IP) as possible and reducing the amount of material in each detector layer. The rather thick hybrid pixel detectors ($\sim 750\mu$m of silicon, $\sim 0.8\%$ rad. length for each pixel layer) are thus not suitable. Similar constraints on multiple-scattering also drive an ILC vertex detector away from a hybrid pixel solution. For the observation of time-dependent CP violation in the gold-plated $B \to J/\psi K_S$ mode with Belle [3], the $\sim 100\mu m$ vertexing resolution based on the Silicon strip Vertex Detector (SVD) [4] measurements was sufficient and the development of a B-factory

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specific pixel detector has not been aggressively pursued. As KEKB [5] has become the highest luminosity collider in the world, operating with sustained luminosities exceeding $10^{34} cm^{-2} s^{-1}$, radiation damage and high occupancy of the SVD have become major issues. New vertexing solutions are needed for the proposed Super B-factory upgrade [6], where the background is expected to increase 20-50 times. Monolithic Active Pixel Sensor (MAPS) [7] have indicated great initial promise to fully exploit the physics reach, as many interesting decay modes are background limited and better vertexing resolution is desired to suppress these backgrounds.

2. CONTINUOUS ACQUISITION PIXEL DEVELOPMENT

2.1. Prototype Evolution

The Continuous Acquisition Pixel (CAP) concept is illustrated in Fig. 1. Brevity of this document dictates simply referring to results from earlier generations of CAP pixel detectors presented previously [8, 9]. These promising results have been followed with the fabrication of a "full size" detector, as seen in Fig. 2. Crucial in these latter designs is the incorporation of a sampling pipeline within each pixel to provide temporal segmentation, which reduces occupancy. Performance studies of this pipeline operation are currently underway.

2.2. CAP Operation as ILC Prototype

As may be seen in a heads-up comparison of the Super B-factory and ILC operating environments in Table I, the requirements on the vertex detector are quite similar. We therefore plan to explore a variant of the CAP architecture specific to future ILC operation.

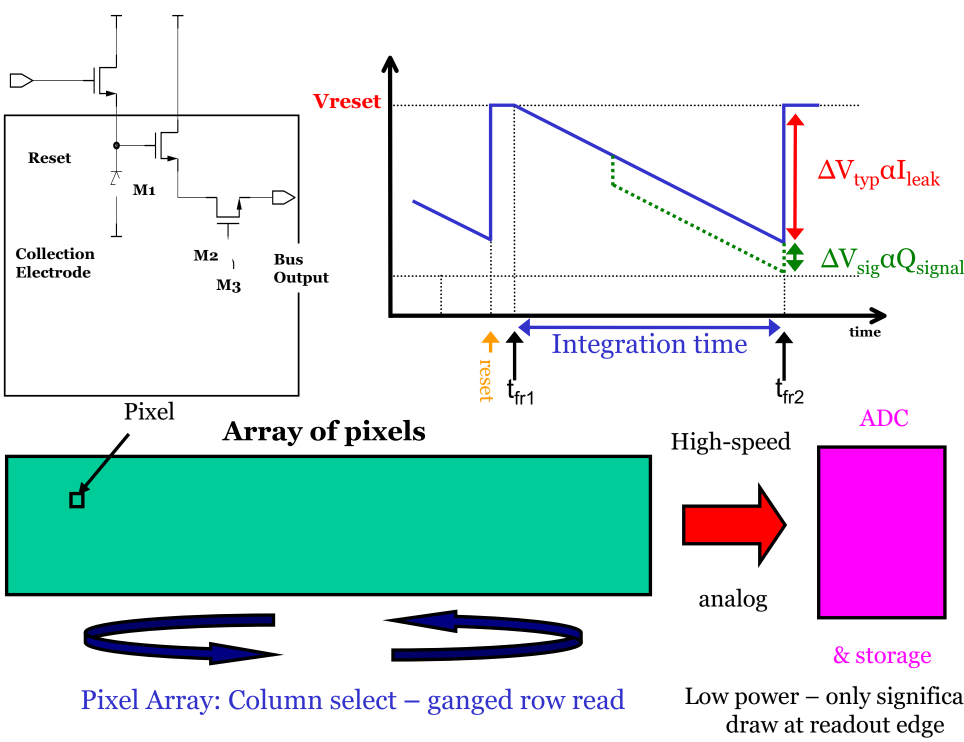

Figure 1: Basics of CAP operation: acquire samples from the standard Active Pixel Sensor cell as fast as possible – in later versions meaning by inserting sampling pipelines within each pixel.

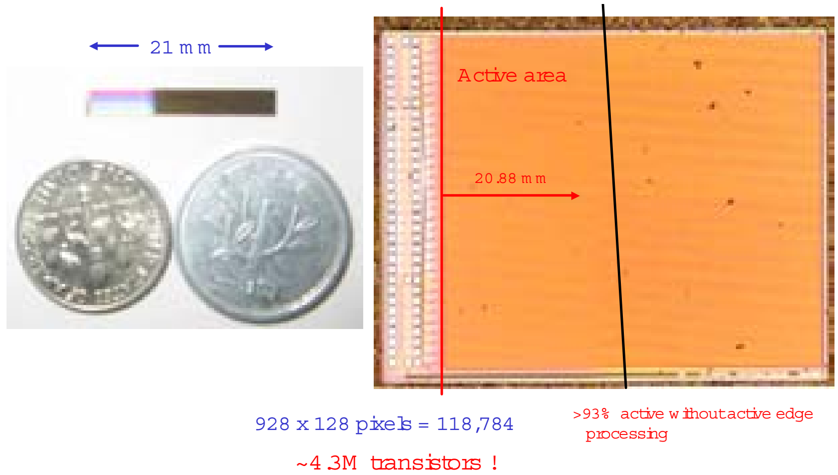

Figure 2: Photographs of the CAP3 die; at right, a zoomed-in view of the bonding pad array.

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Table I: Comparison of Super B-Factory and ILC vertex environments and subsequent demands on vertex detector performance.

Parameter	**ILC**	**Super-B**	Notes
Integration time	$25\mu s/1$ms	$\leq 10\mu s$	Belle (trigger dep.)
BX collision timing	300 (150) ns	2 ns	
# bunches/integ. time	75(150)/2.8k	1-5k	CPCCD or MAPS/DEPFET for ILC
Expected occupancy	$\sim 1\%$	$\sim 0.5 - 1\%$	Belle extrapolation
# pixel channels (Million)	100's to 1k	10-50	5 layers versus single
Duty cycle (high power)	few %	5-10%	within acceptance
Readout cycle	between trains	continuous	
Pixel readout rate (raw)	500/10 Gpix/s	200-1000 Gpix/s	Belle 10kHz trigger
Radiation requirements	0.5kGy/yr	few 10kGy/yr	NIEL not considered

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