Hadron Calorimetry

for the Linear Collider

(for DAQ Group/LCWS05)

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OUTLINE

- Brief look at Hcal configurations for the various detector concepts

- HCal implementation technologies

- Some numbers (channels, rates,...)

  (**CAUTION: work has been for Test Beam**!)

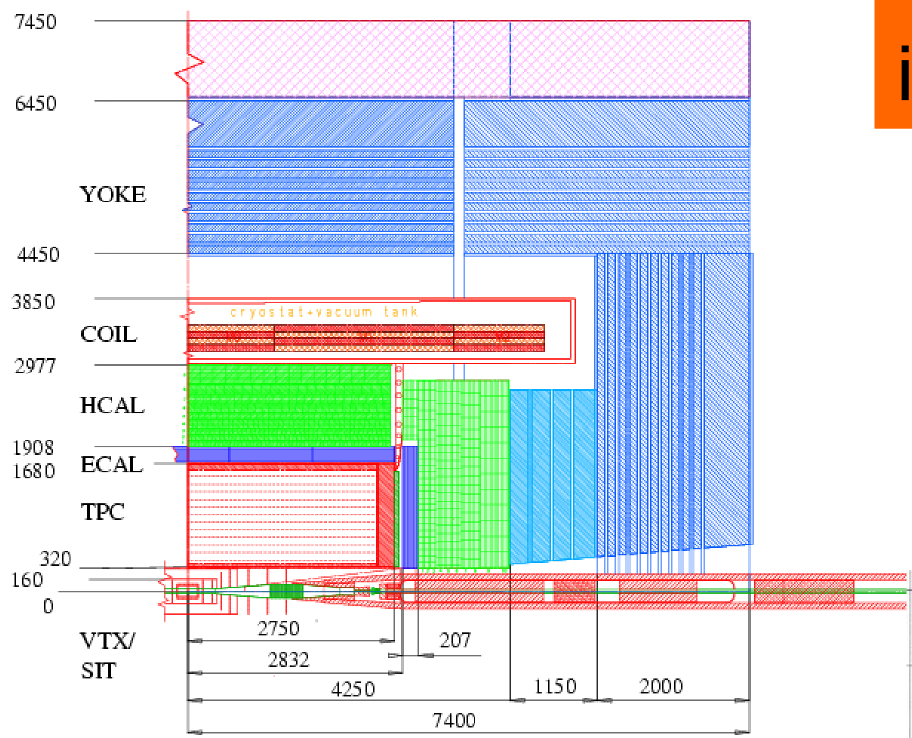
- Details of the RPC/GEM readout scheme

- Some more numbers...

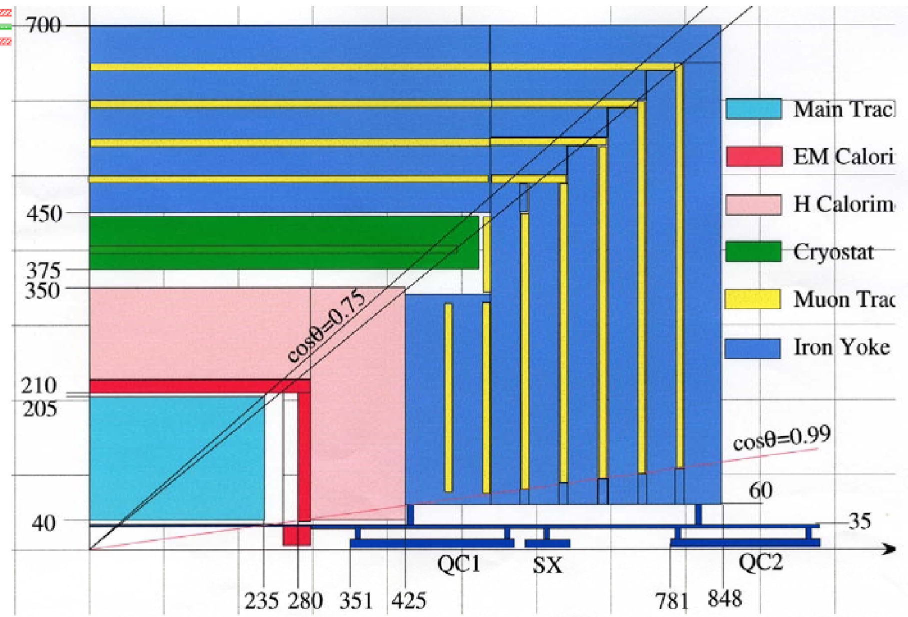
- Questions/issues for HCal/DAQ

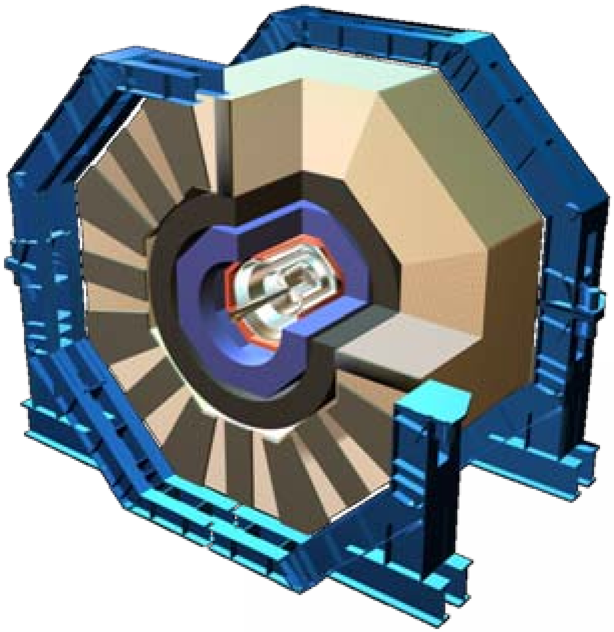
Large Detector

Detectors with large inner calorimeter radius



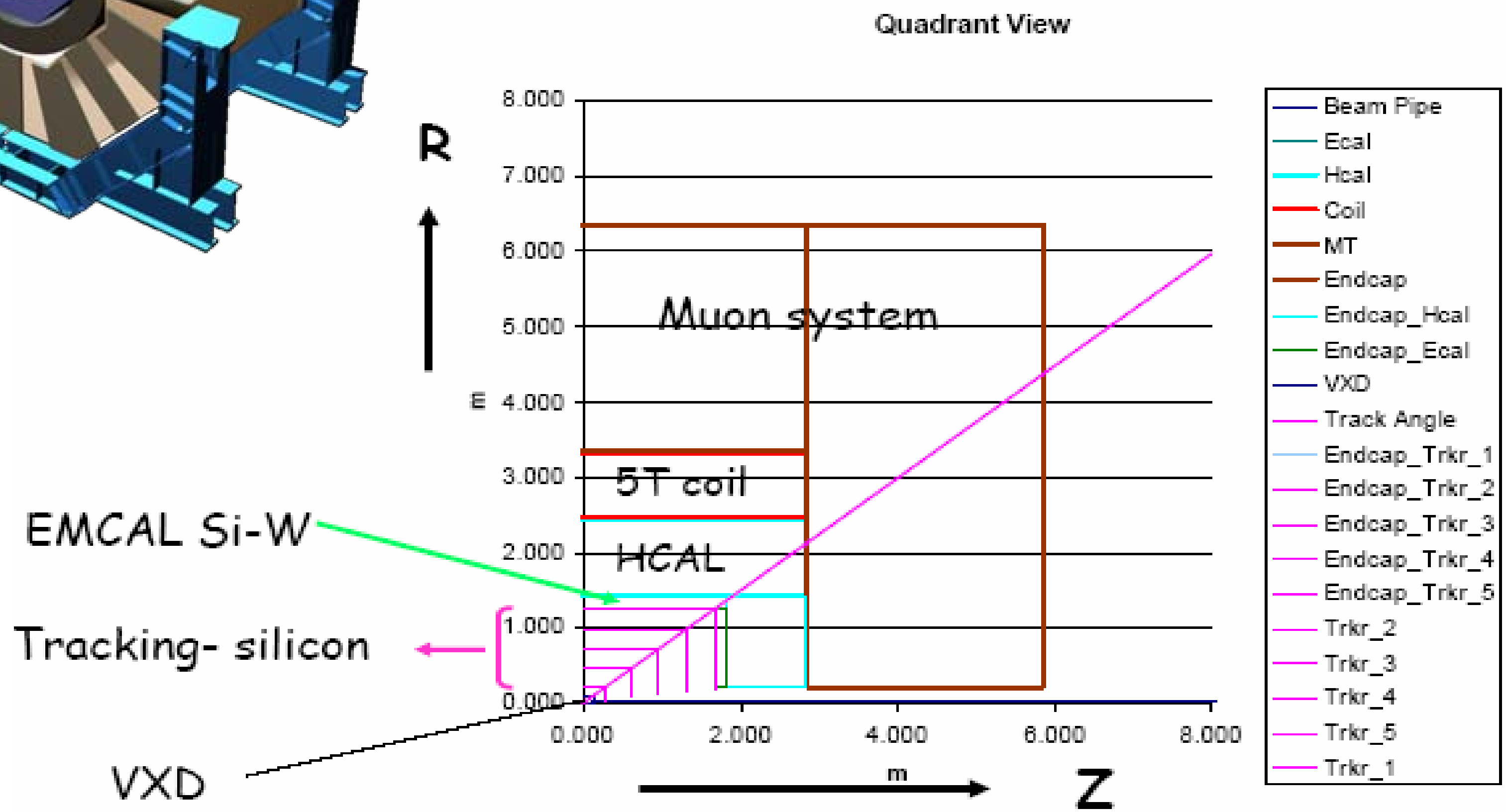
GLD





SiD

Compact detector



NOT A SMALL DETECTOR

HCAL Requirements – with DAQ notes

Physics requirements emphasize segmentation/granularity (transverse AND longitudinal) over intrinsic energy resolution.

- Depth $\geq 4\lambda$ (not including ECal ~ 1λ) + tail-catcher(?)

-Assuming PFlow:

- sufficient segmentation (#channels) to allow efficient charged particle tracking.

- for “digital” approach – sufficiently fine segmentation (#channels) to give linear energy vs. hits relation

- efficient MIP detection (threshold, cell size)

- intrinsic, single (neutral) hadron energy resolution must not degrade jet energy resolution.

Hadron Calorimetry

- General agreement on exploring the Particle Flow Algorithm(PFA) approach to achieve required jet energy resolution.

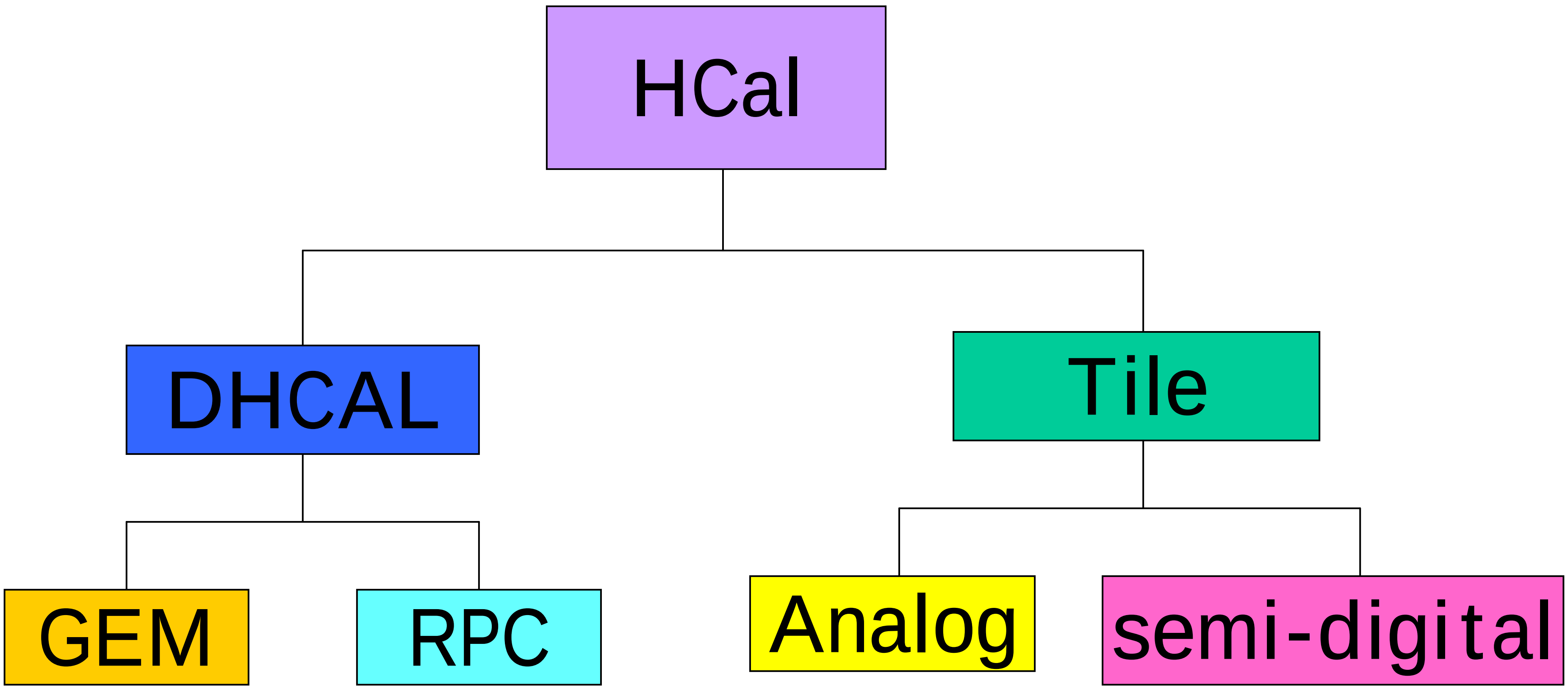
- PFA requirements translate into lateral segmentation of O(1 cm^2 -> 5 cm^2) and longitudinally O(30-40 layers).

?? Central question: what is the most effective way to implement the hardware for PFA??

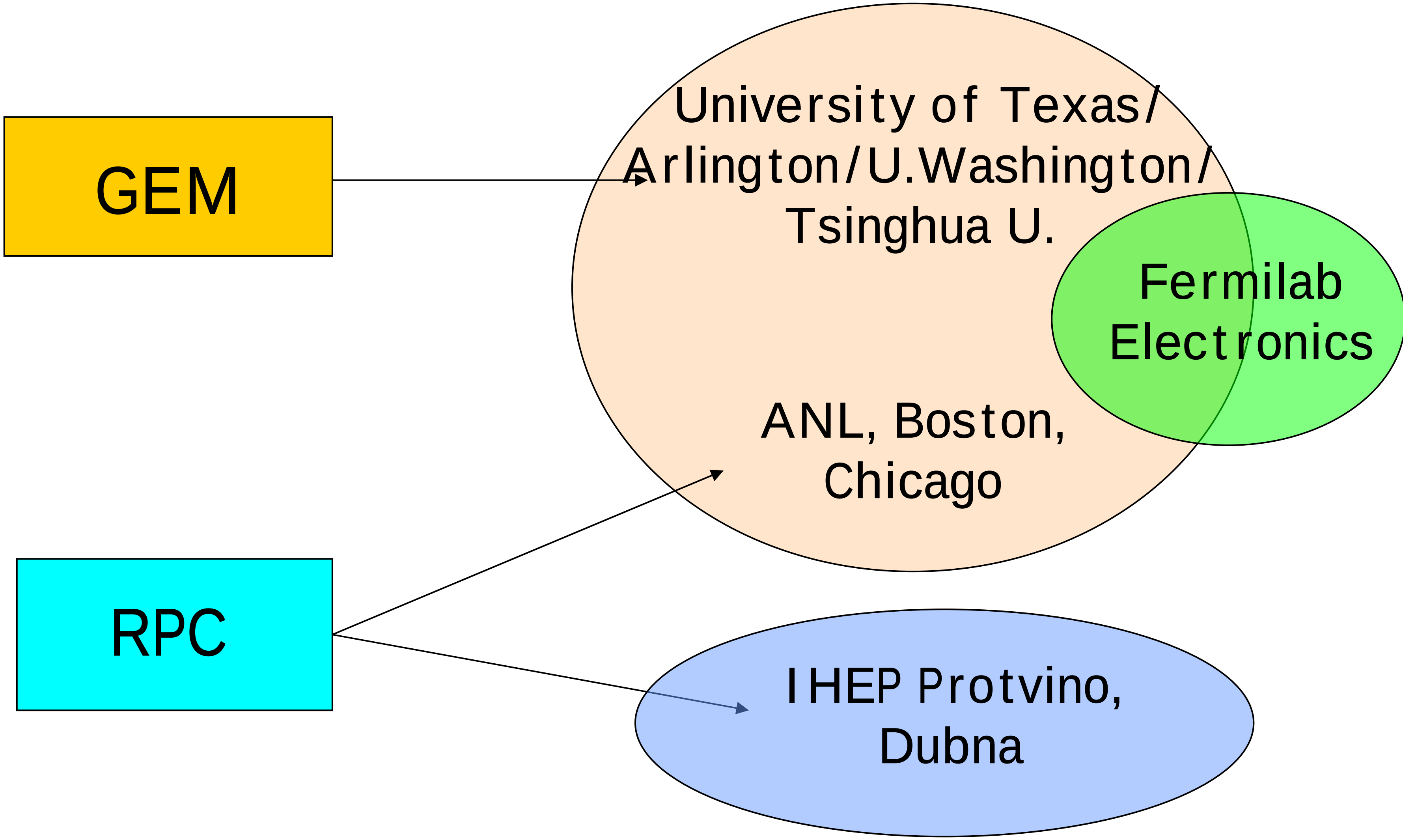
- Verification requires a combination of:

1) Test beam measurements
2) Monte Carlo verification at fine spatial resolution
3) PFA(s) development to demonstrate jet energy resolution.

Hadron Calorimetry



Digital Hadron Calorimetry



DHCAL – GEM-based

University of Texas at Arlington

- A flexible technology, easy to construct (non-demanding environment) and operate.

- Low voltage (~400V/foil) operation

- O(1 cm^2) cells easy to implement

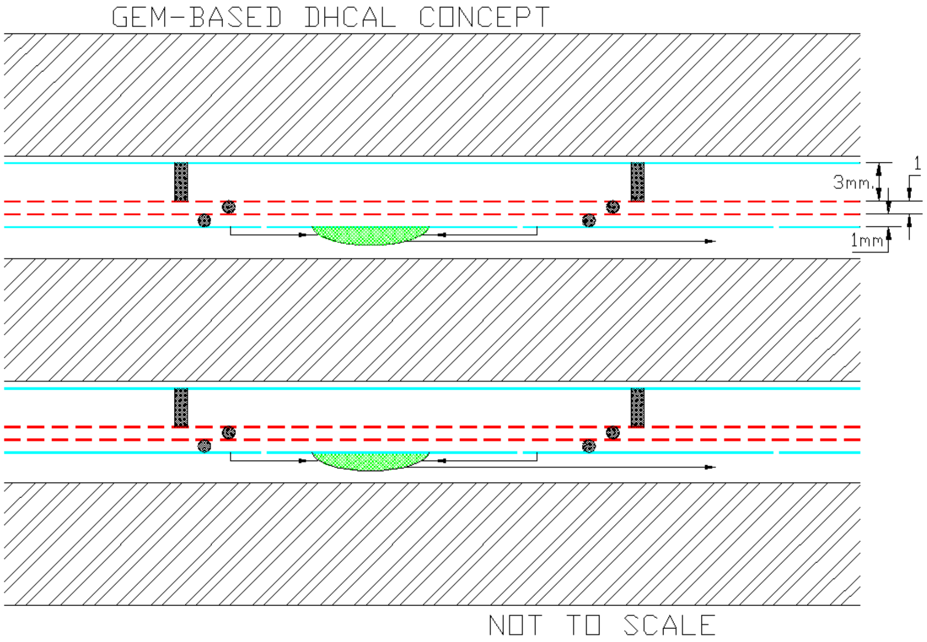
- Various small prototypes constructed to understand assembly procedures

- Prototypes tested with cosmics/source

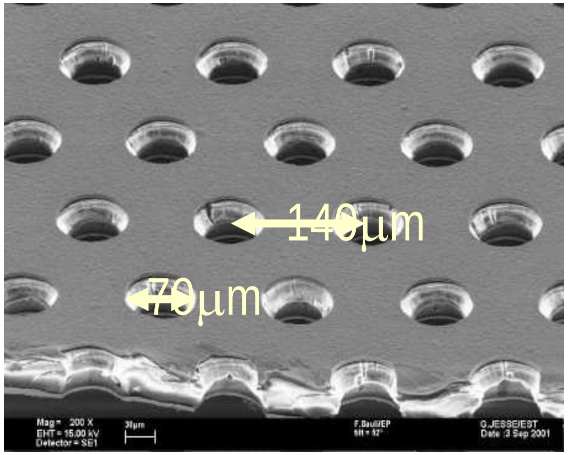
- Supplier(s) of GEM foils under consideration (3M Corporation in Texas)

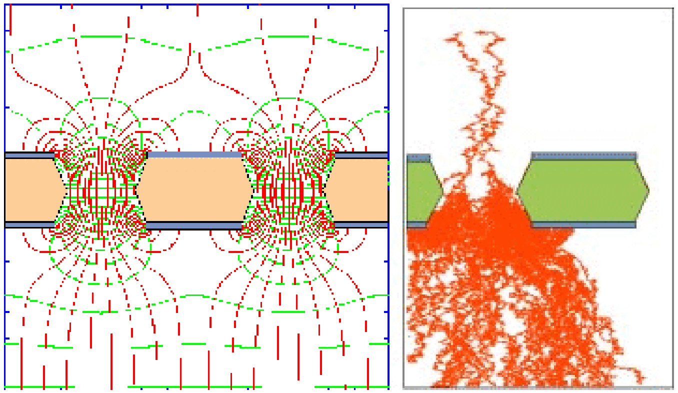
- Procedures for assembly of large scale mechanical prototypes of GEM active layers have been developed.

Design for DHCAL using GEM



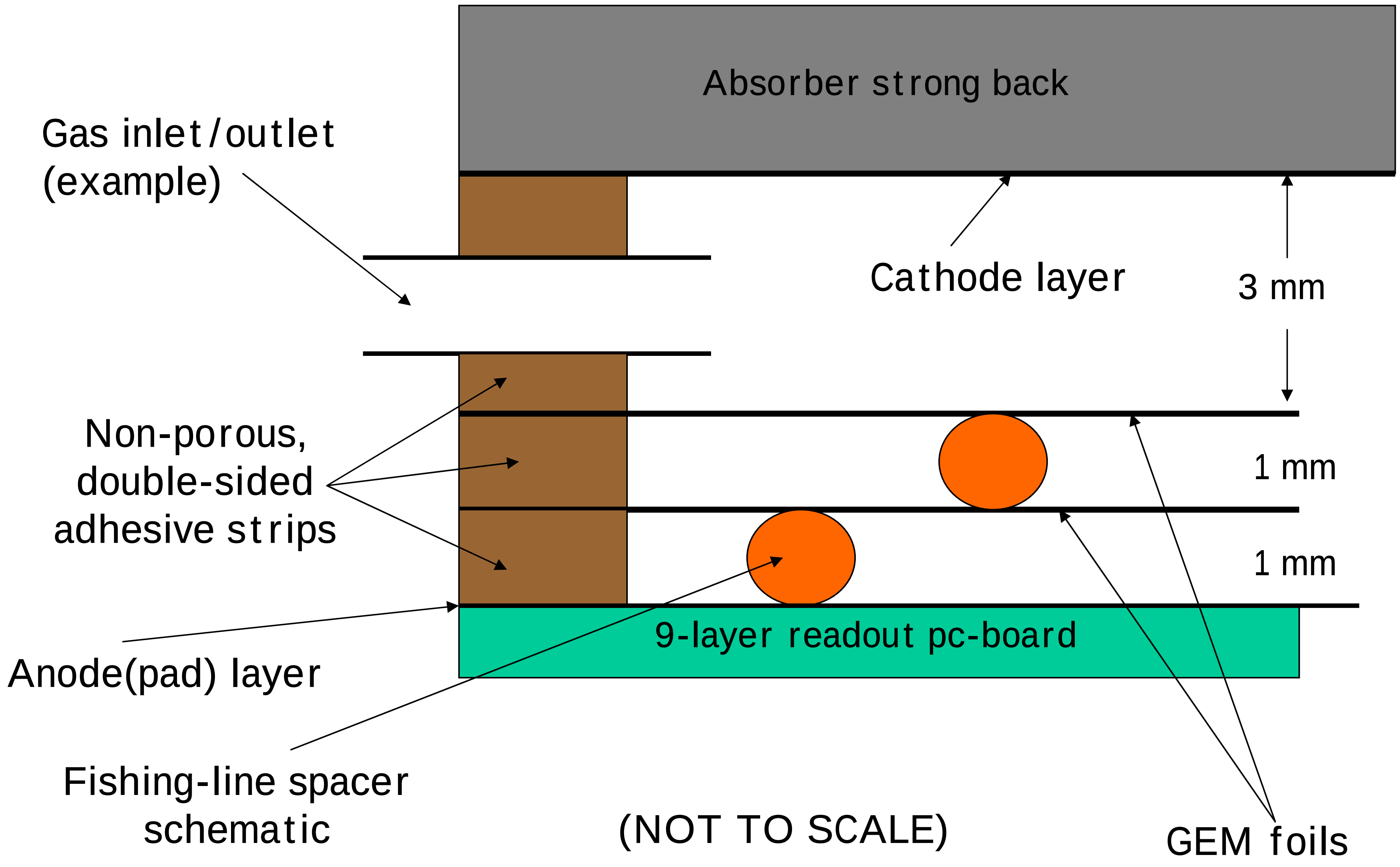
A.White (UTA) - 2001



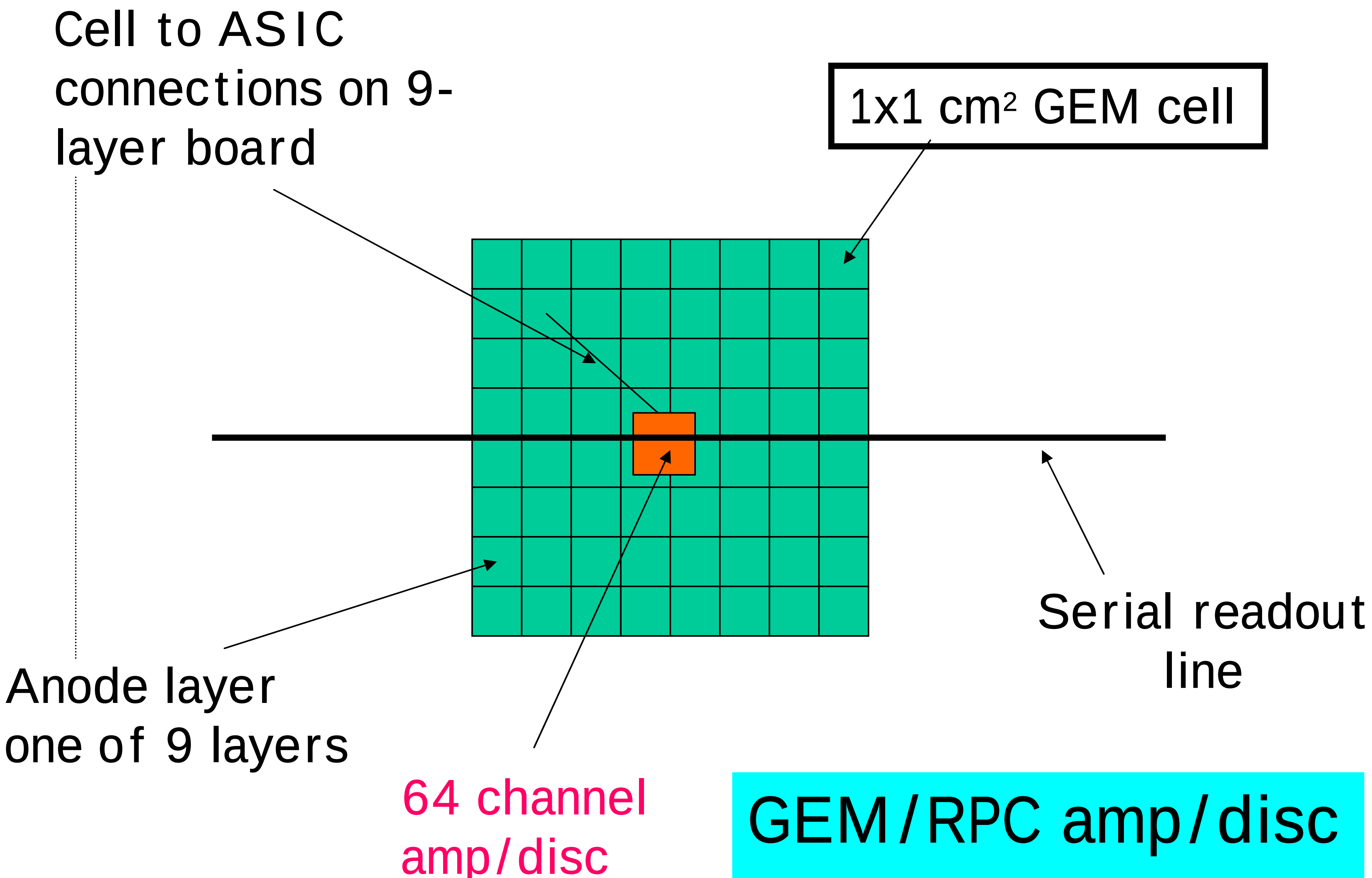


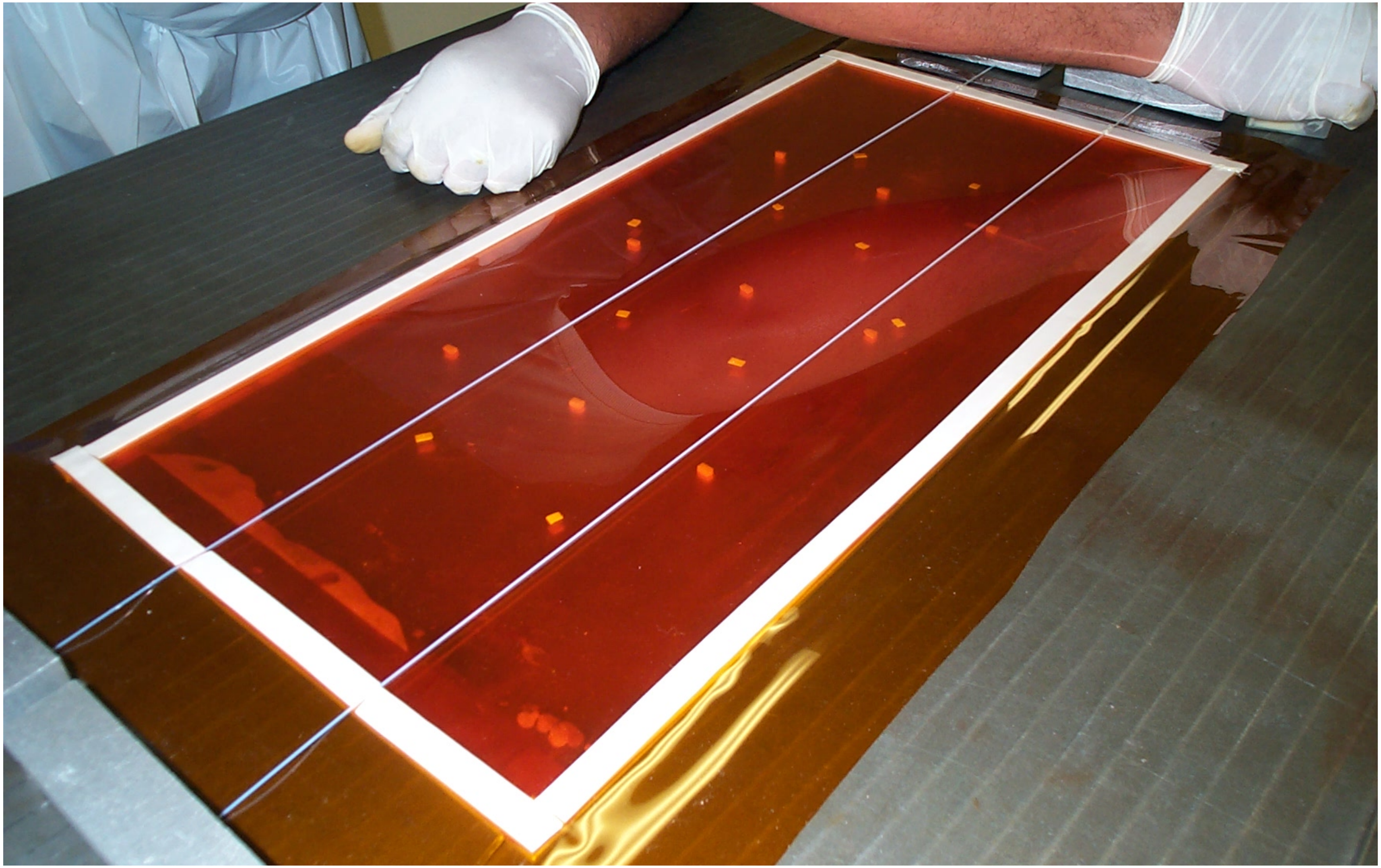
From CERN-open-2000-344, A. Sharma

Development of GEM sensitive layer



GEM/RPC amp/disc concept





An almost-complete mechanical double-GEM calorimeter layer

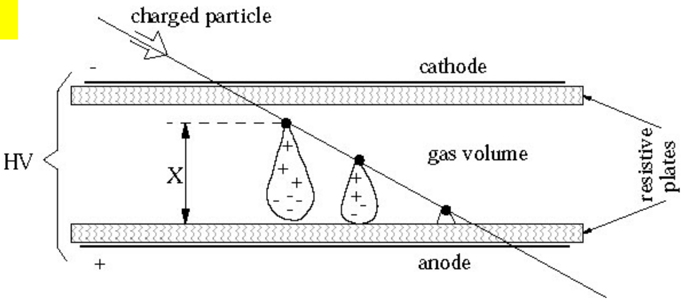
DHCAL – RPC-based

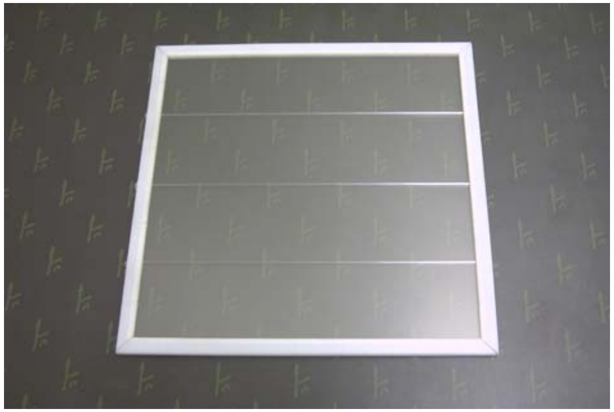
- Easy assembly techniques
- Mechanically robust layers.
- Large signal sizes (several pC's)
- High voltage operation - ~7-9 KV
- O(1 cm^2) cells easy to implement
- Using common RPC/GEM FE (also common readout scheme for Test Beam at Fermilab)

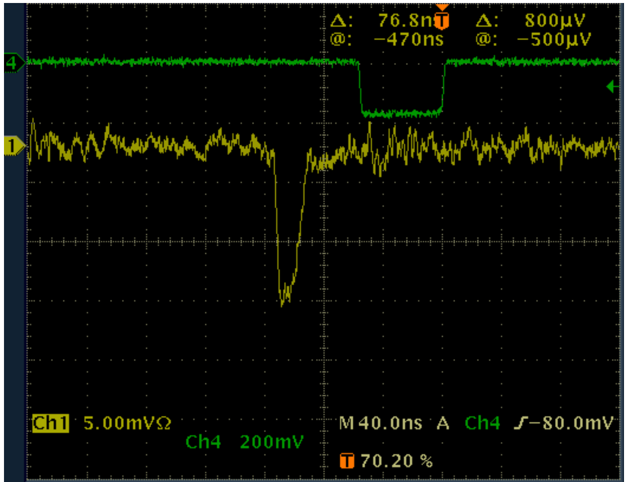
DHCAL – RPC-based

1) ANL, Boston, Chicago, Fermilab

- RPCs are simple detectors
  - Parallel resistive plates
  - Enclosed gas volume
  - Apply HV across gas volume, by resistive ink layer
  - External pad(s) to pick up signal
- Basic cosmic ray test setup
  - Single test pad + analog readout
    - Signal charge, efficiency, operational modes, etc.
  - Multiple readout pads + analog readout
    - Charge distribution on pads, efficiency, hit multiplicity
  - Multiple readout pads + digital readout
    - Efficiency, hit multiplicity, noise rates
    - Close to the running condition in a digital calorimeter

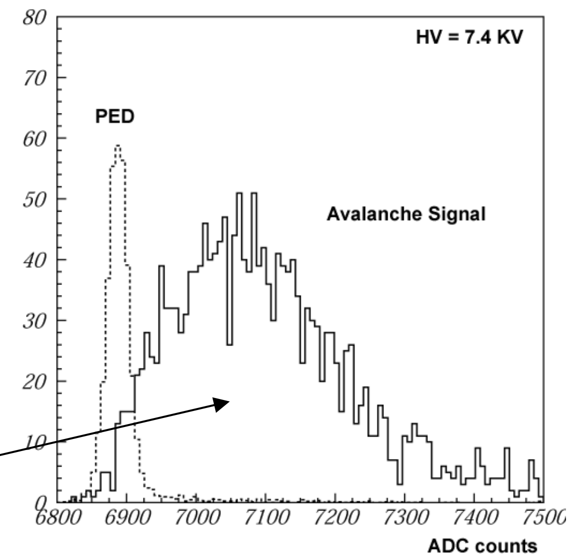


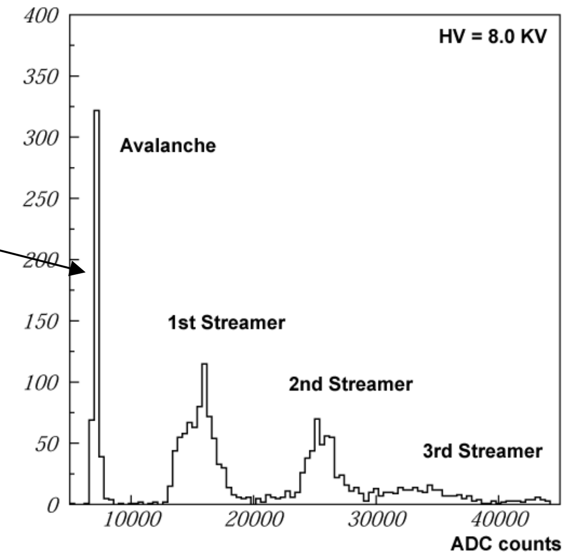




DHCAL – RPC-based

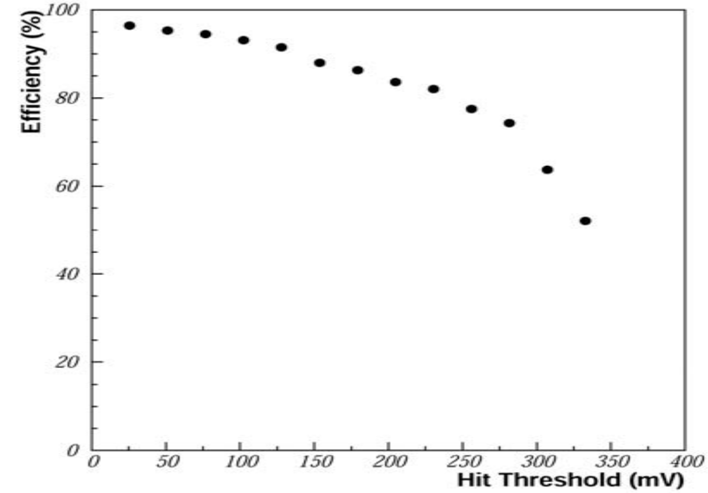
- Large single pad to cover whole chamber
- Trigger: cosmic ray ‘telescope’
  - Signal rate ~1Hz, trigger area ~10x10cm^2
- Analog readout: ‘RABBIT’ system (CDF)
  - Measure total charge of a signal
  - Charge resolution ~1.1fC/ADC bit, dynamic range ~ -6pC to ~ +60pC, very low noise level
  - Multi-channel readout
- Two modes of operation
  - Avalanche
    - Average signal charge: 0.2 – 10+ pc
    - Lower operating voltage
    - Typical efficiency ~99%
    - Very low noise level
    - Rate capability <1kHz/cm^2
  - Streamer
    - Average signal charge: 10 – 100+ pc
    - Higher operating voltage
    - Typical efficiency ~90%
    - Rate capability ~10Hz/cm^2
    - Multiple streamers

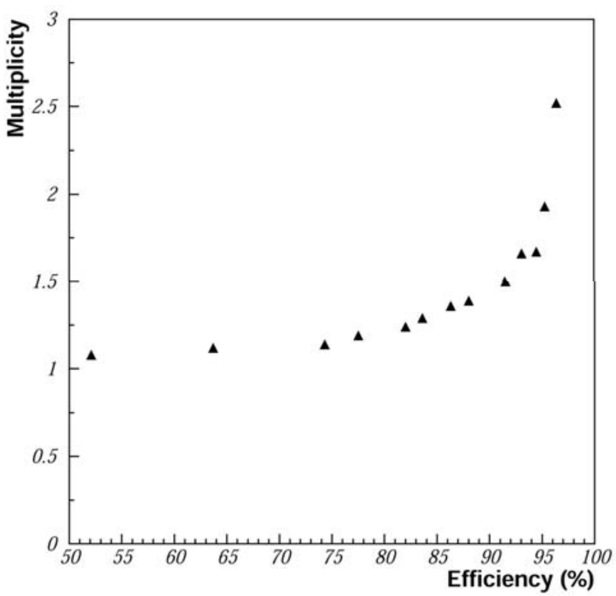


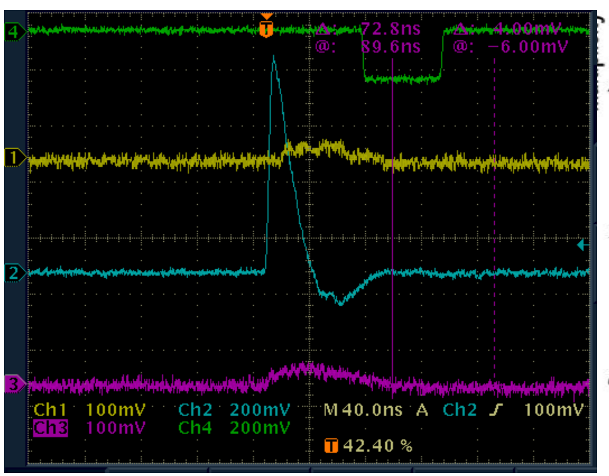


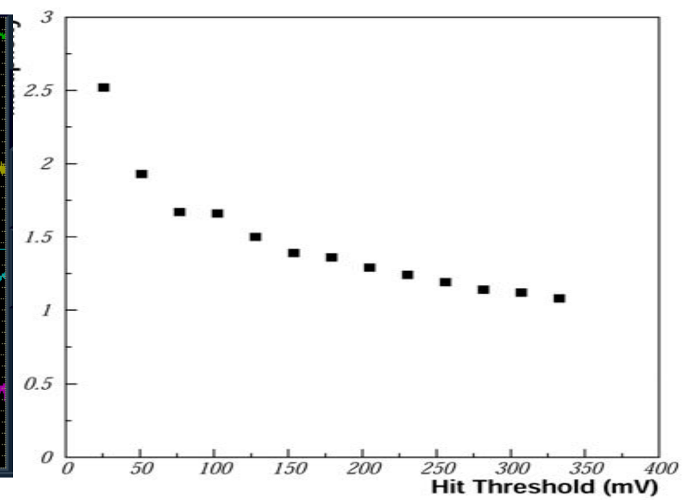
Multiple pads + digital readout: hit multiplicity with avalanche signal

- Test with 1-gap chamber, 8x8 pads, 6.8KV
  - Avalanche mode, eff ~ 97%
- Better hit multiplicity at higher threshold, at the cost of lower efficiency
- Number of pads seeing signal:
  - Most of events: 1 or 2 pads
  - Small fraction: 3 or 4
  - Almost none: 5 or more









Tile Calorimeter

Prague, DESY, Hamburg, ITEP, JINR, LPI, MEPhI, NIU, LAL, UK

- Combines well-known scintillator/wavelength shifting fiber technology with new photo-detector devices.

- Small tiles required for implementation of PFA.

- Explore analog and semi-digital approaches – optimize spatial and analog information use.

- Must verify simulation description of hadronic showers at high granularity.

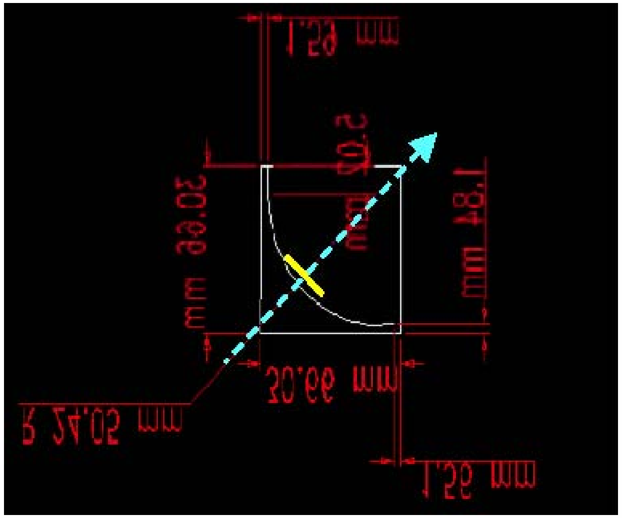
- Results from "minical" prototype

- Components for cubic-meter stack under construction

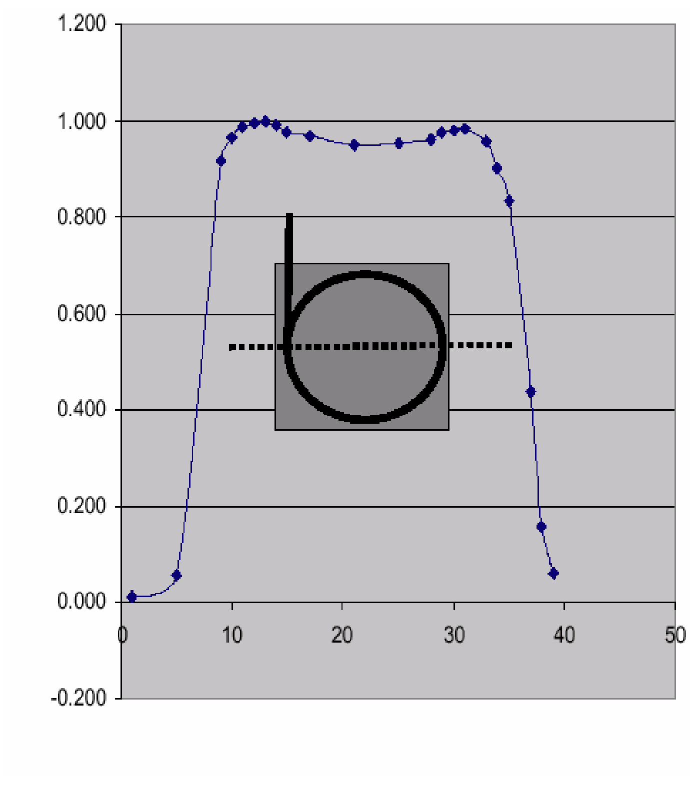
Tile HCal – Scintillator tile/fiber

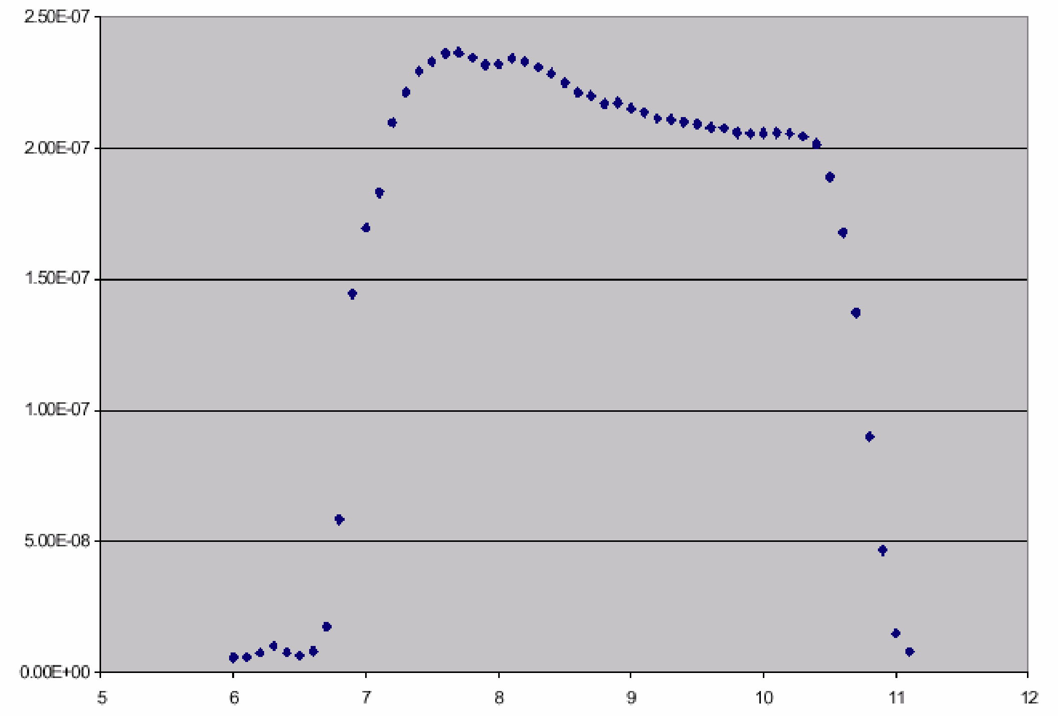
Vladimir scintillator
+ Kuraray Y11

“Rainbow groove”



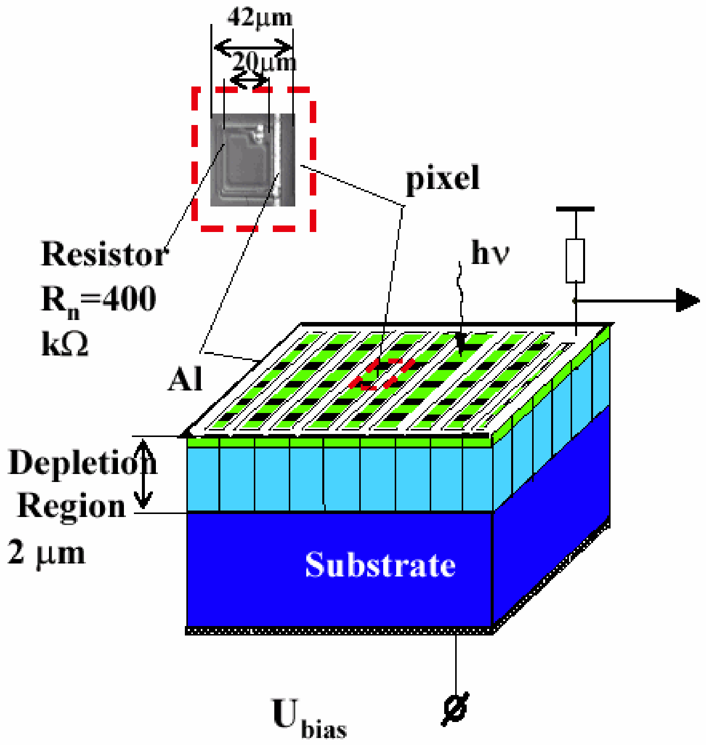
“Sigma” groove





Tile HCal – SiPM Photodetector

SiPM main characteristics



- Pixel size ~20-30µm
-

Electrical inter-pixel cross-talk minimized by:
- decoupling quenching resistor for each pixel
- boundaries between pixels to decouple them
 ➔ reduction of sensitive area and geometrical efficiency

• Optical inter-pixel cross -talk:
-due to photons from Geiger discharge initiated by one electron and collected on adjacent pixel

- Working point: $V_{Bias} = V_{breakdown} + \Delta V \sim 50\text{-}60$ V
$\Delta V \sim 3$V above breakdown voltage

Each pixel behaves as a Geiger counter with
$Q_{pixel} = \Delta V\, C_{pixel}$
with C_{pixel}~50fmF ➔ Q_{pixel}~150fmC=10^6e

Dynamic range ~ number of pixels (1024)
➔ saturation

HCal – Some numbers (approximate!)

Channel count

SiD/Digital HCal – cell size $1cm^2$

- R(inner) = 1.35m, R(outer) = 2.75m
- Average layer area ~$80m^2$
- 40 layers

-> O(40M channels) inc. endcaps

Large Detector/Tile-analog – cell size $9cm^2$

- 30 layers

-> O(2M channels – barrel)

HCal – Some numbers (approximate!)

Data size/event – for SiD/digital

- Readout: one FE-ASIC handles 64 channels

-> 40 x 10^6 channels/64 = 6 x 10^5 sectors

-> assume for a "busy" event ~10% of sectors have at least one cell hit

-> Each sector yields ~100 bits

-> Total data/event = 6 x 10^5 x 10% x 100 = 6 x 10^6 bits

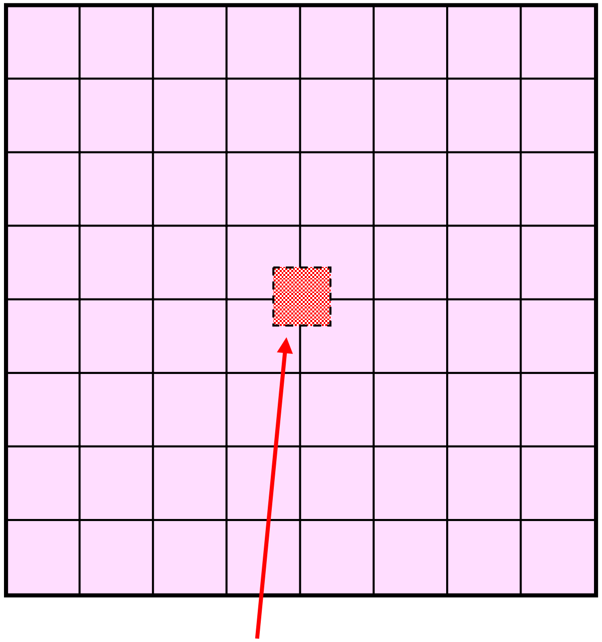
(no zero suppression)

N.B. M.Breidenbach (this morning) -> Cal. Data rate 5MB

Digital HCal readout scheme (test beam)

⇨ ***ASICs on Detector.***

8 x 8 RPC Cell Array
(Part of Single RPC Chamber)



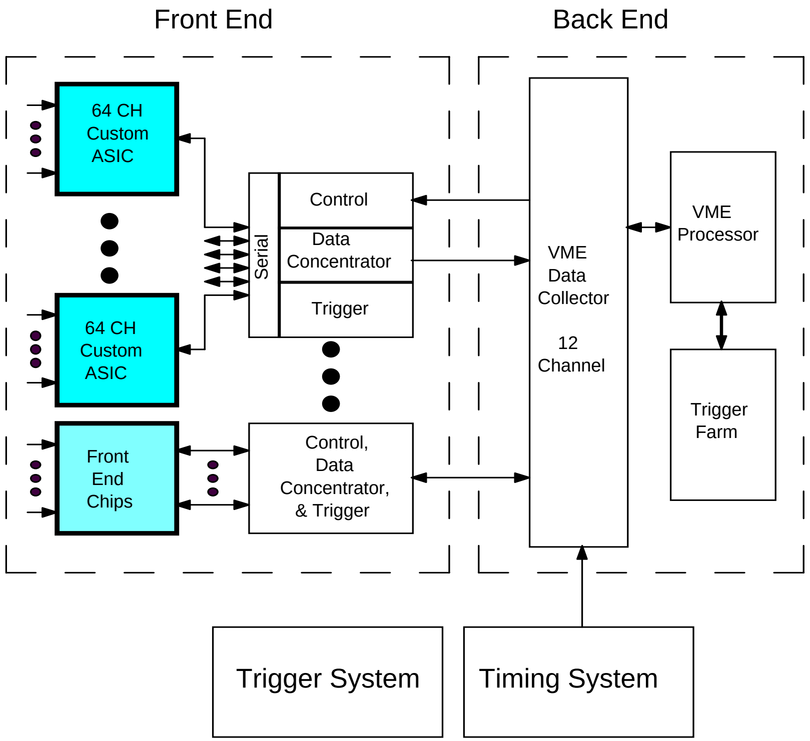
ASIC on Opposite Side of Pads

Pads on Bottom, ASIC on Top

Digital HCal readout scheme (test beam)

From Gary Drake/ANL

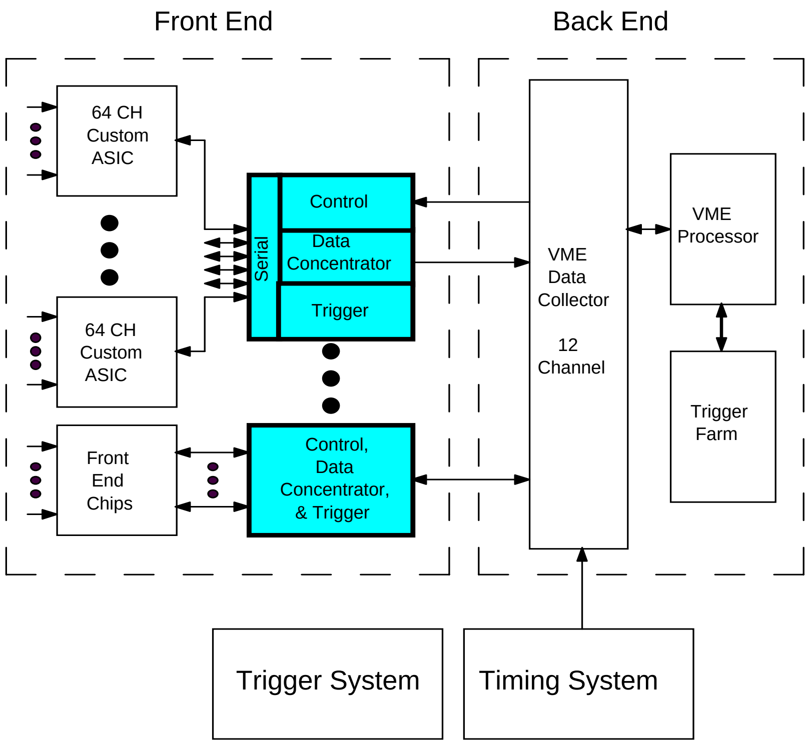
- Custom ASIC
  - Performs Functions:
    - Receive, Process, & Discriminate Detector Signals
    - Timestamp Hits, & Record Hit Pattern
    - Temporary Data Storage
    - Serial Data Transmission
  - Can Self-Trigger, or Use External Trigger
  - Services 64 Detector Channels
- Mother Board
  - Chips Reside on Chamber



First submission of ASIC next week

Digital HCal readout scheme (test beam)

- Data Concentrator:
  - Concatenate Serial Data Streams from Several Chips → Multiplexer
  - ***N*** Serial Lines In, 1 Serial Line Out
  - Drives Serial Line to Back End Read-Out Electronics
  - Handles Clock & Control Interface
  - Handles Trigger Interface

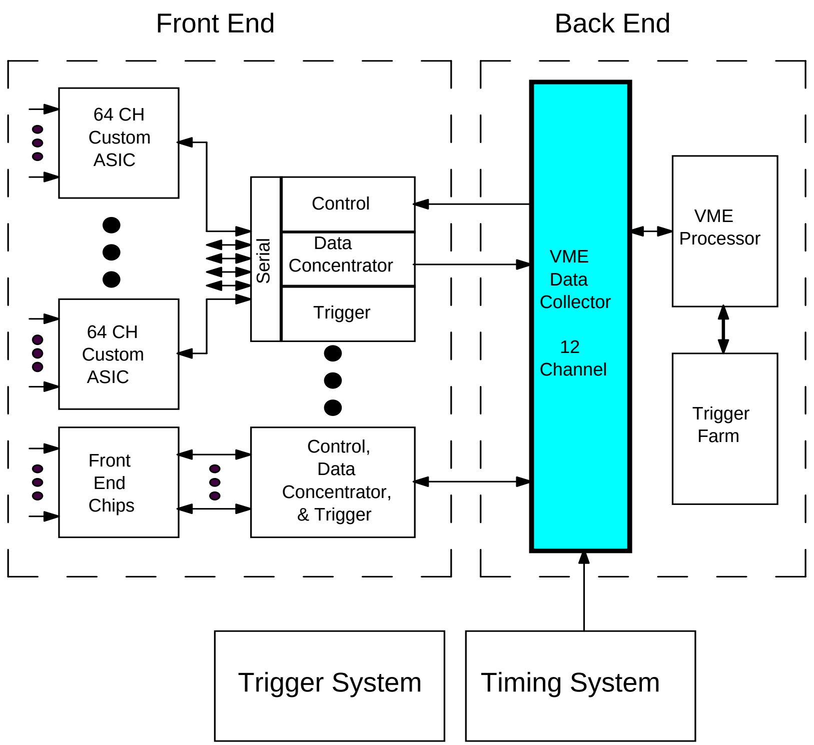


Digital HCal readout scheme (test beam)

– Data Collector:
- Receives Serial Data Streams from Several Data Concentrators
- Stores Data in Buffers
- Dual Buffers: Data Written into One While Processor Reads the Other

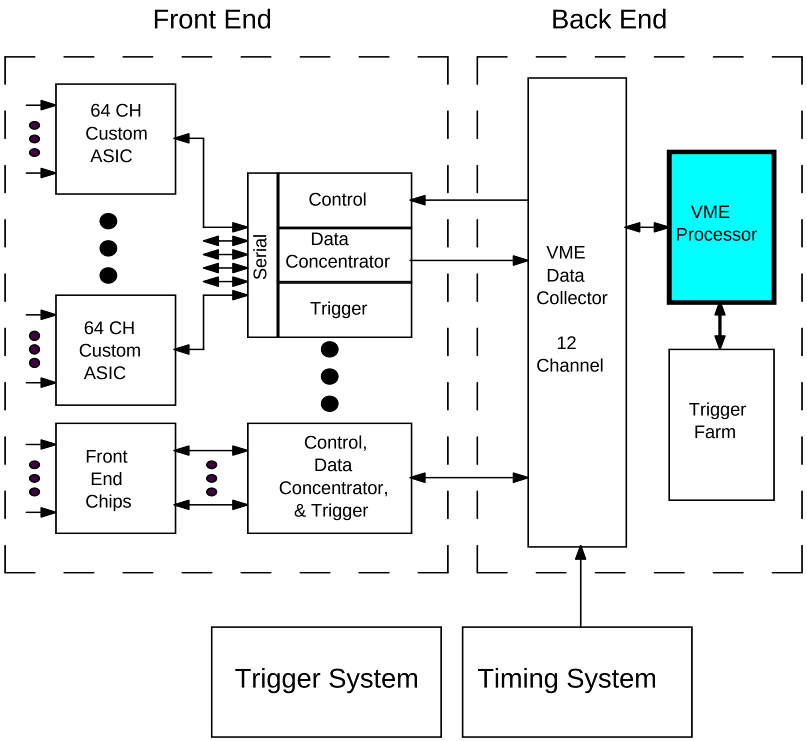
  → "Buffer Swaps"

  → No Deadtime



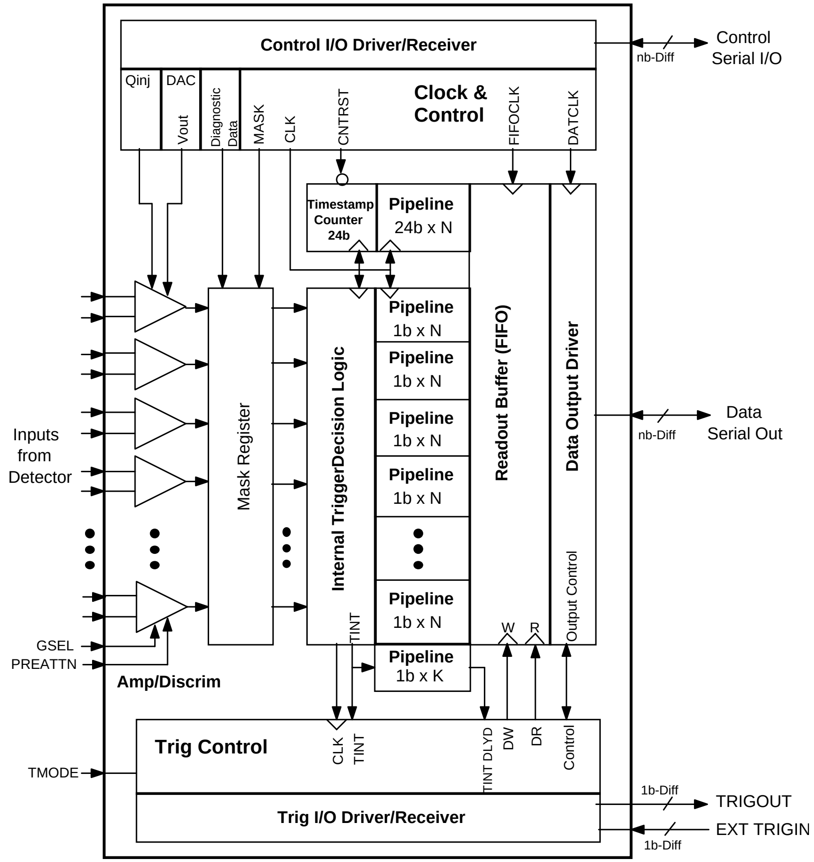
Digital HCal readout scheme (test beam)

– VME Processor:
- Buffer Swaps Coordinated by VME Timing Module using ISRs
- Read Data from All Data Collectors in VME Crate
- Forms Time Frames from Timestamps (~1 Sec)
- Sends Time Frames to Trigger Farm for Processing



Digital HCal readout scheme (test beam)

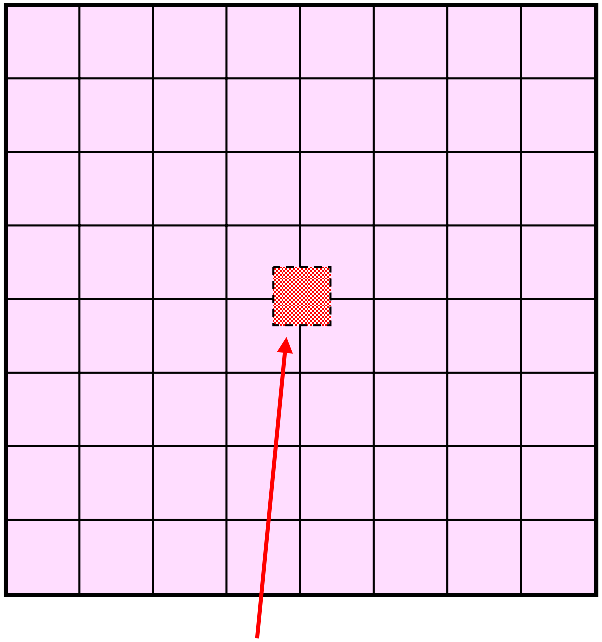
- **Front End Amplifier & Discriminator Senses Hits Above Threshold**
- **24-Bit Timestamp Counter Runs at 10 MHz**
- **Comparator States Clocked into Shift Register - Buffer for Trigger Decision**
- **Save States & Timestamp on Ext. Trig. or Self-Trigger**
- **Serial Data Output - 100 MHz, 88 Bits/Event, 1 uSec/Event**
- **Serial I/O – Separate Data, Control, & Trigger**
- **Services 64 CH**



Digital HCal readout scheme (test beam)

⇨ ***ASICs on Detector.***

8 x 8 RPC Cell Array
(Part of Single RPC Chamber)

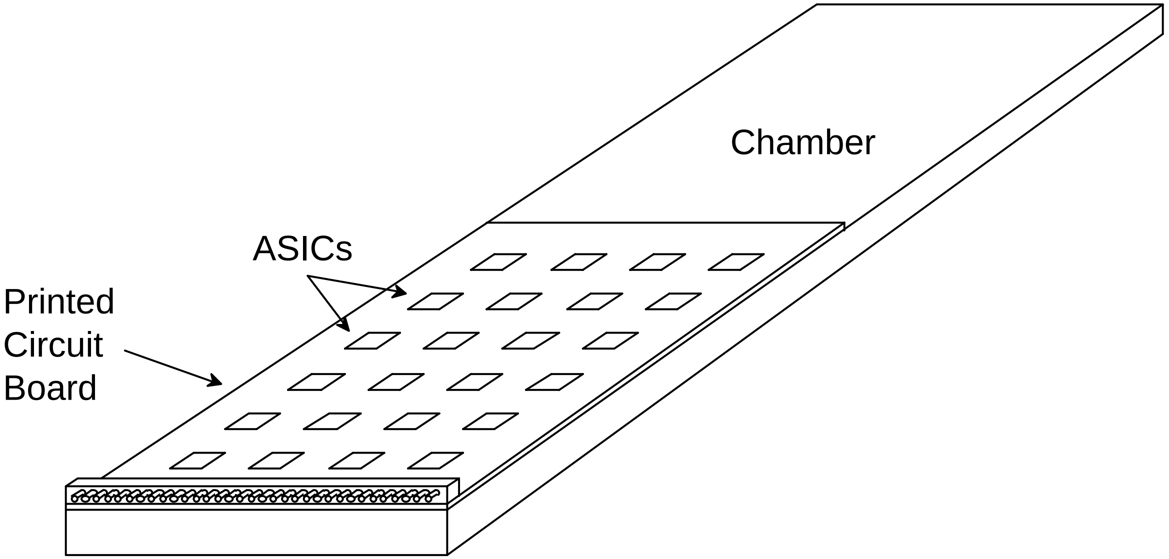


ASIC on Opposite Side of Pads

Pads on Bottom, ASIC on Top

Digital HCal readout scheme (test beam)

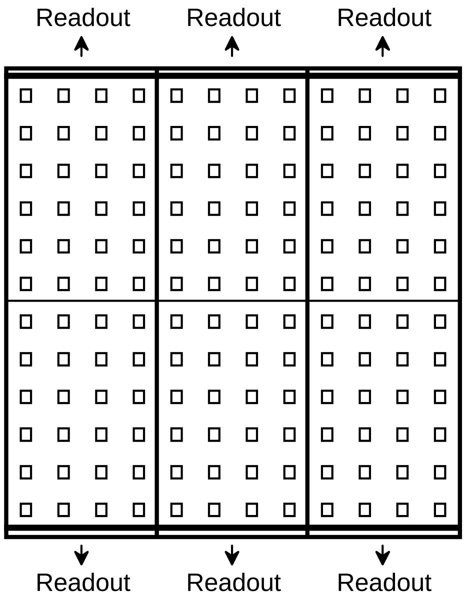
- **One PCB Contains 24 ASICs, Each Servicing an 8x8 Array of Pads**
- **Arrange Data Connectors on Outside Edge of Chamber**



Digital HCal readout scheme (test beam)

2 Front End Boards/Chamber
6 Front End Boards/Plane
24 ASICs/FE Board
144 ASICs/Plane
9216 Channels/Plane(test beam)

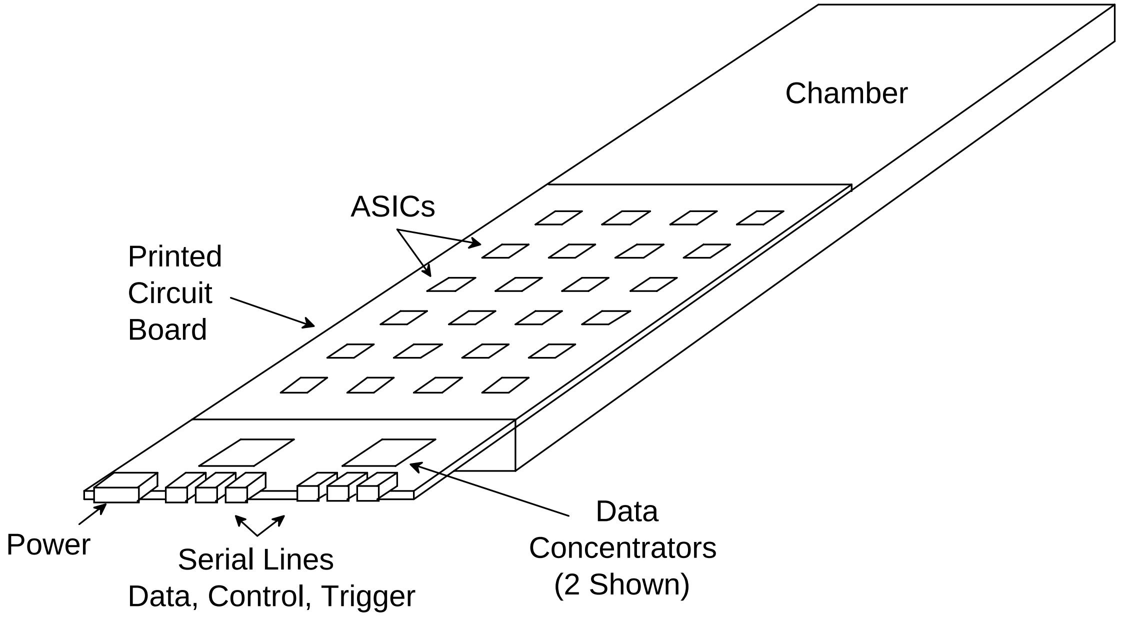
1m^3 stack of GEM/RPC has ~400,000 channels!



View of Plane

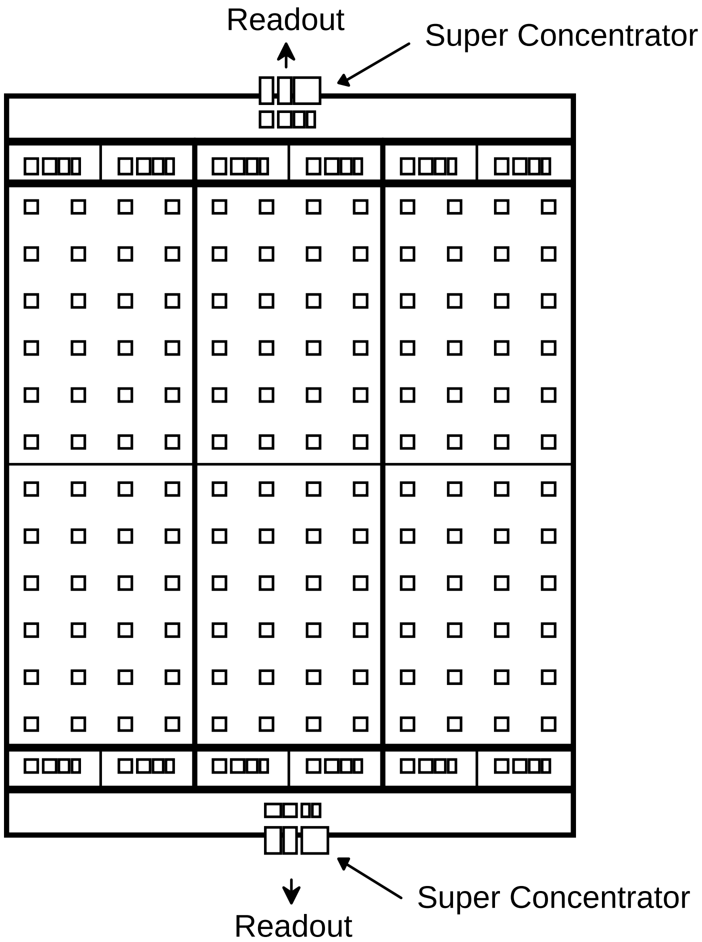
Digital HCal readout scheme (test beam)

- **Host for Data Concentrator Circuitry**
- **Plugs Into Front End Board**
- **Interface for Power Distribution**
- **Forms Integral Unit with Front End PC Board**
- **Plan: Each Data Concentrator Reads Out 12 Chips, or 768 Channels**



Digital HCal readout scheme (test beam)

- **Each Super Concentrator Reads Out 6 Data Conc., or 144 ASICs, or 4608 Channels**

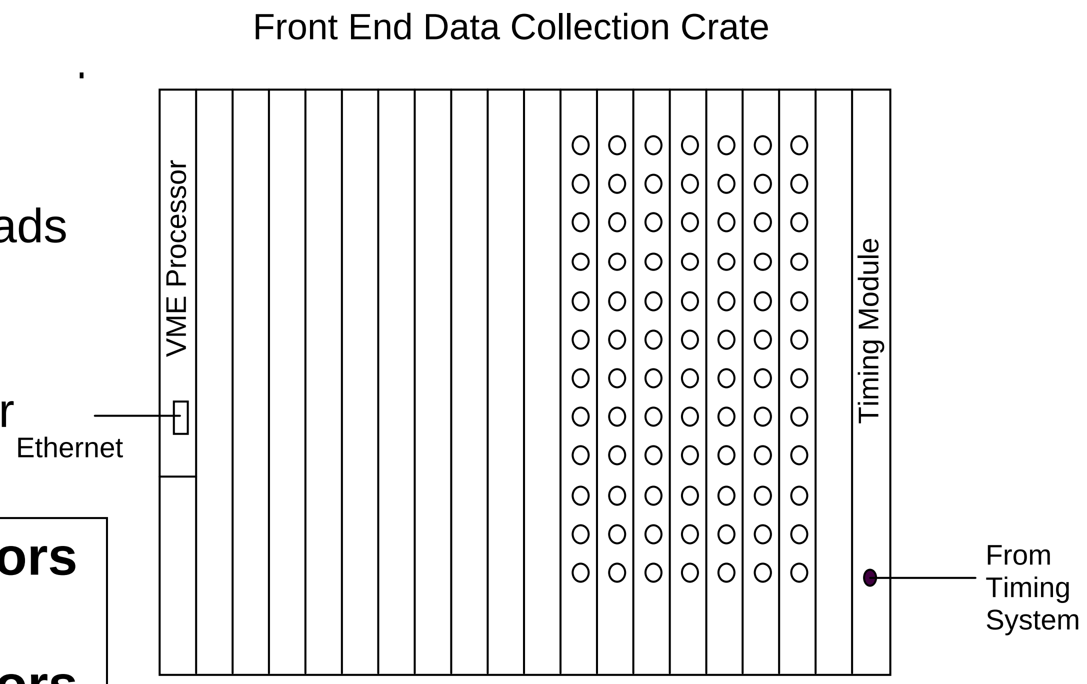


View of Plane

Digital HCal readout scheme (test beam)

– Data Collector (Cont.)
  - VME Crate Hosts Data Collectors
  - VME Processor Reads Data from Data Collectors
  - Data Sent to Trigger Farm over Ethrenet

2 Super Concentrators per Plane
12 Super Concentrators per Data Collector
6 Planes per Data Collector



⇨ ***With Super Concentrators, Need 1 Crate***

HCal – Some numbers (approximate!)

Data rate (SiD/digital test beam prototype):

- Serial data rate from FE = 100MHz
- ...so 100 bits @ 100MHz -> 1 μsec (all sectors in parallel
- then into data concentrator (for > 3 hits it is better to retain all 64 bits + time stamp rather than have individual time-stamped hits)
- ...but what about zero suppression?
- when sector information is merged, need to add geographical address information

HCal/DAQ Issues, Questions etc.

- Physics + background occupancy (#cells, #sectors) ?
- Detector/DAQ interface (VME processor for test beam)
- Readout strategies w.r.t. beam structure?
- Zero suppression/concatenation schemes?
- Data organization/structure – e.g for efficient EFlow
- Time/crossing stamping
- Ideas on global DAQ scheme(s)?? Too early??

Next steps? HCal/DAQ interaction?