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Front-End electronics developments for CALICE W-Si calorimeter

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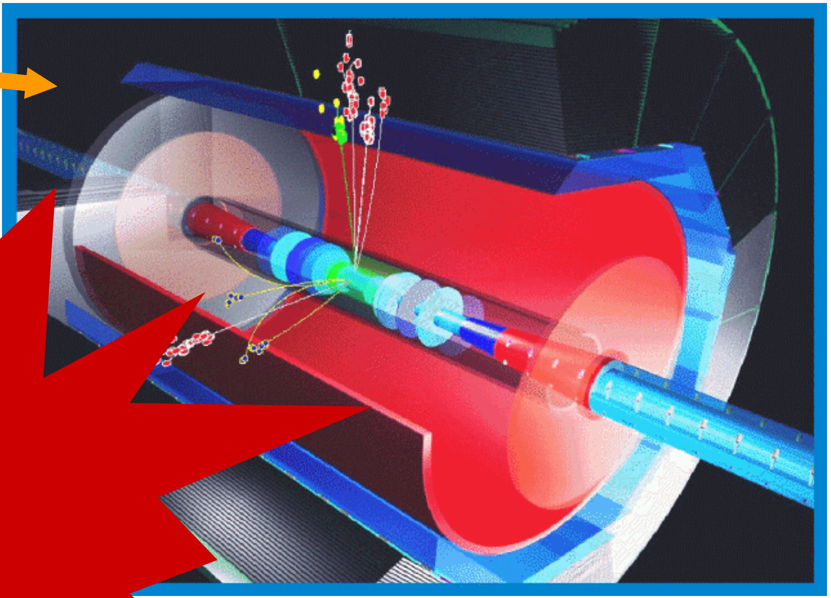
IN2P3/LAL Orsay & LPC Clermont

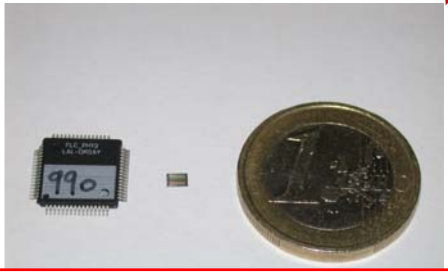
http::/www.lal.in2p3.fr/technique/se/flc

Introduction : FLC challenges for electronics

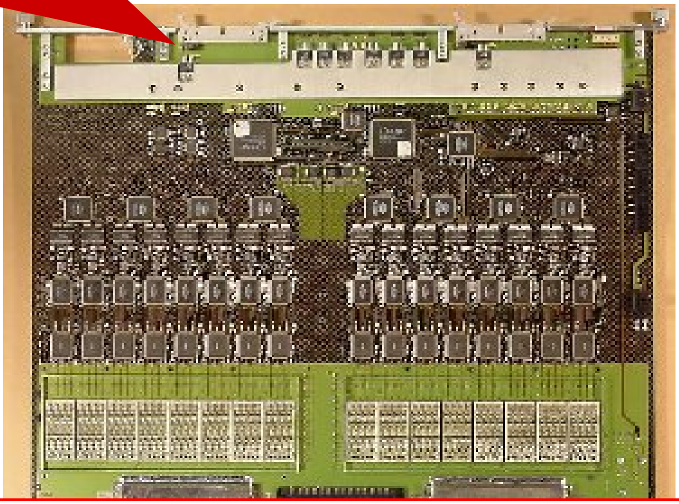
- **CALICE = W-Si Calorimeter**
  - Precision measurements : ~10%/√E
    - good linearity (‰ level)
    - Good inter-calibration (% level)
    - Low crosstalk (‰ level)
  - Large dynamic range (15 bits)
    - 0.1 MIP -> ~3 000 MI
  - Auto-trigger on MIP
    - Low noise << M
  - Hermeticity : no roo
    - High leve
    - **Ultra-low pow**
  - ~30 Mchannels
- **« Tracker electronics w**
  calorimetric performan e »



Low
POWER
is the
KEY issue

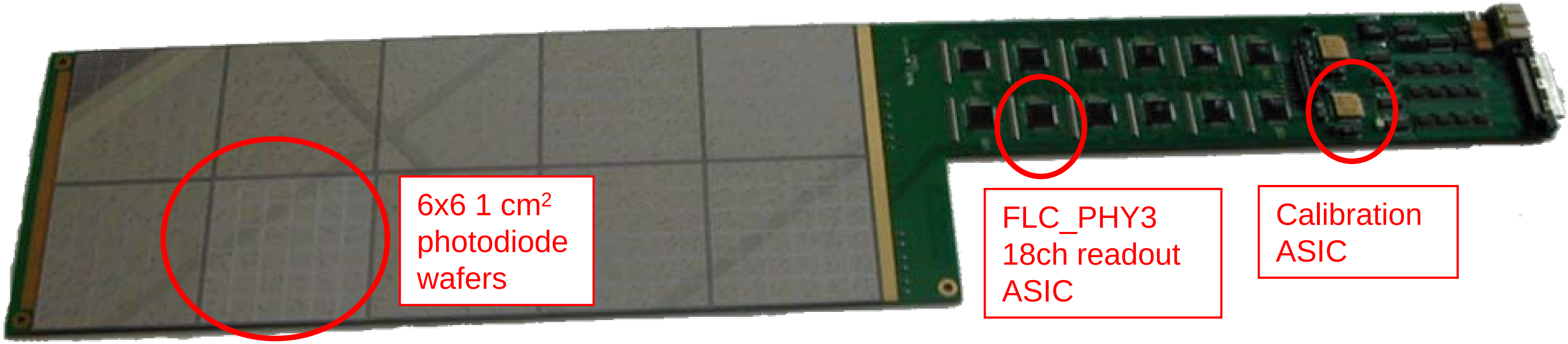


FLC_PHY3 18ch 10*10mm **5mW/ch**

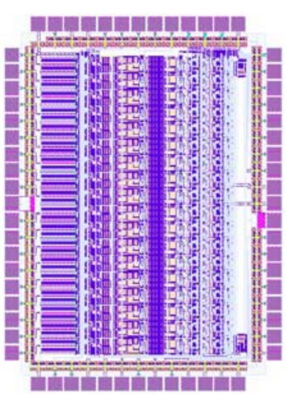


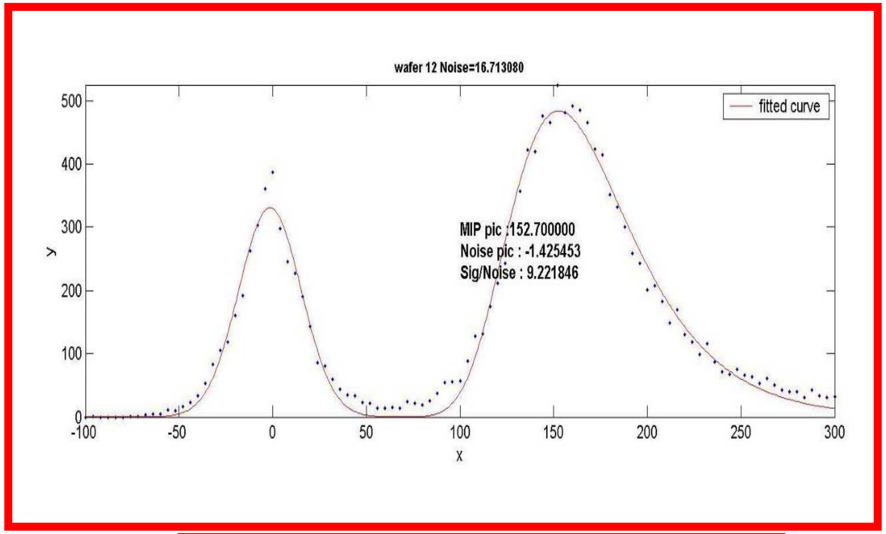
ATLAS LAr FEB 128ch 400*500mm **1 W/ch**

FLC W-Si front-end electronics : FLC_PHY3 ASIC



- **FLC_PHY3 in a nutshell** *[see talk by J. Fleury]*
  - Variable gain preamp : 0.3-5 V/pC
  - Bi-gain shaper G1-G10 t_p=200ns
  - Multiplexed analog output 5MHz
  - 18 channels, Pd = 100 mW total
  - ENC = 4000 e-
  - MIP/noise = 9
  - Emax = 1000 MIPS
  - 2000 chips produced
  - AMS 0.8µm BiCMOS
  - Yield : 80%

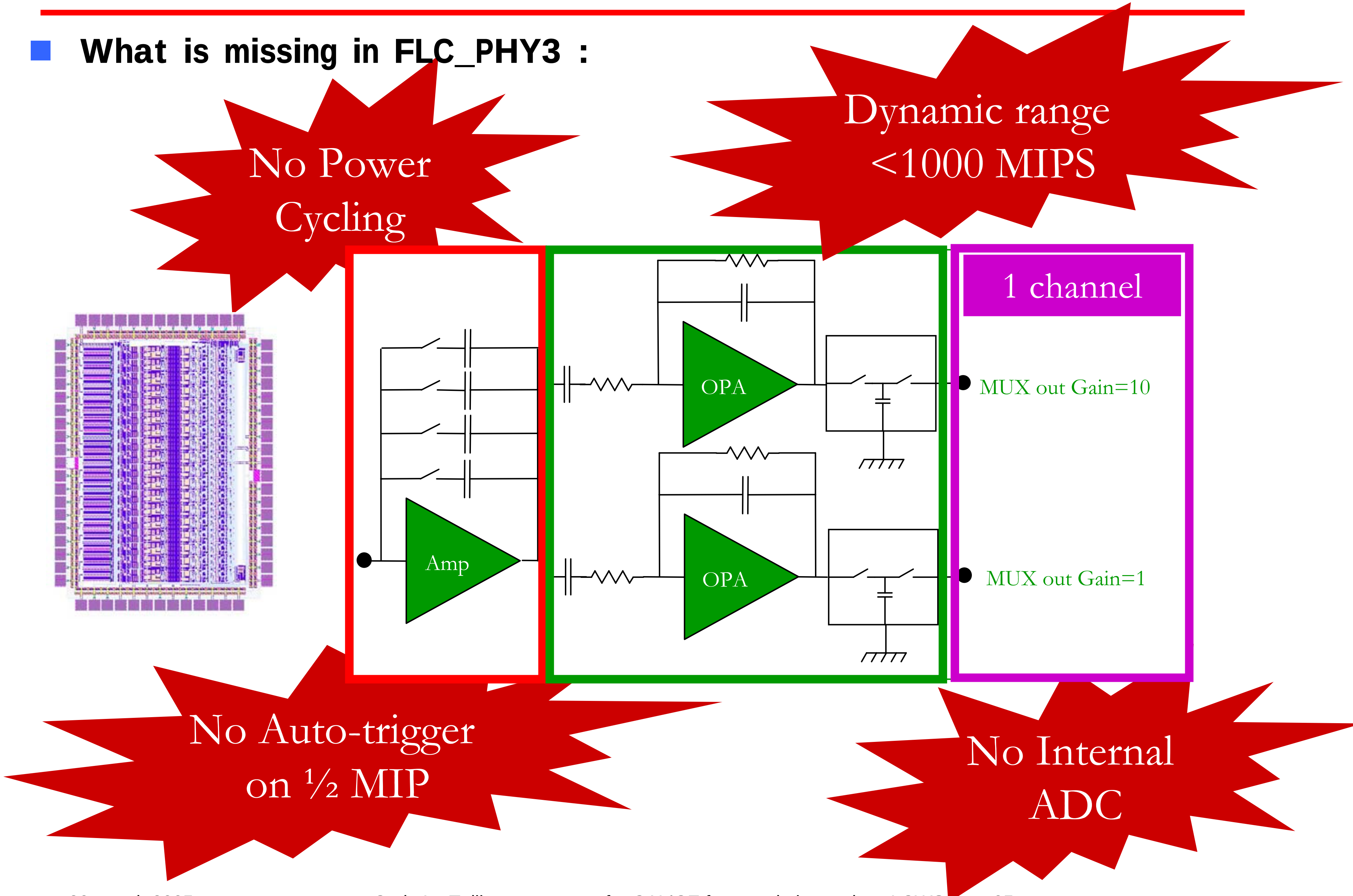




Noise and MIP on cosmic bench

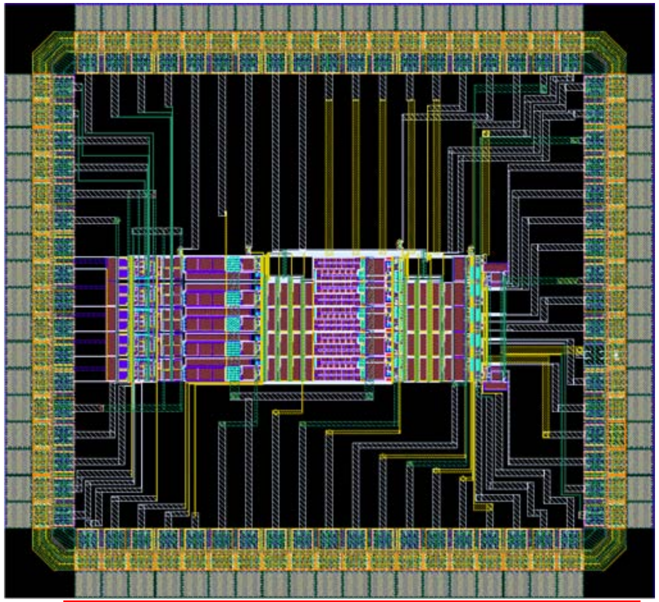
Towards module0 ASIC : FLC_TECH

- **What is missing in FLC_PHY3 :**

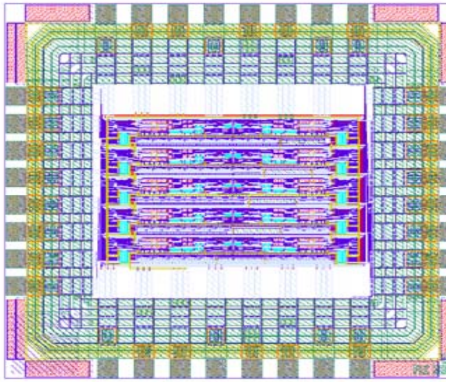


ASIC developments in 2004-2005

- **FLC_TECH1 : moving into SiGe 0.35µ**
  - 4ch preamp + shaper + power cycling
  - Testing power cycling
  - Submitted Apr 04, currently under test
- **FLCPHY4 : integrating the ADC**
  - FLC_PHY3 architecture basis
  - Power pulsing
  - No external components
  - Integrated ADC
  - To be submitted april 05
- **FLC_TECH2 : on-chip zero-suppress**
  - Prototype of module0 front-end electronics
  - Foreseen end 2005
- **ADCs**
  - Several ADC architectures being studied



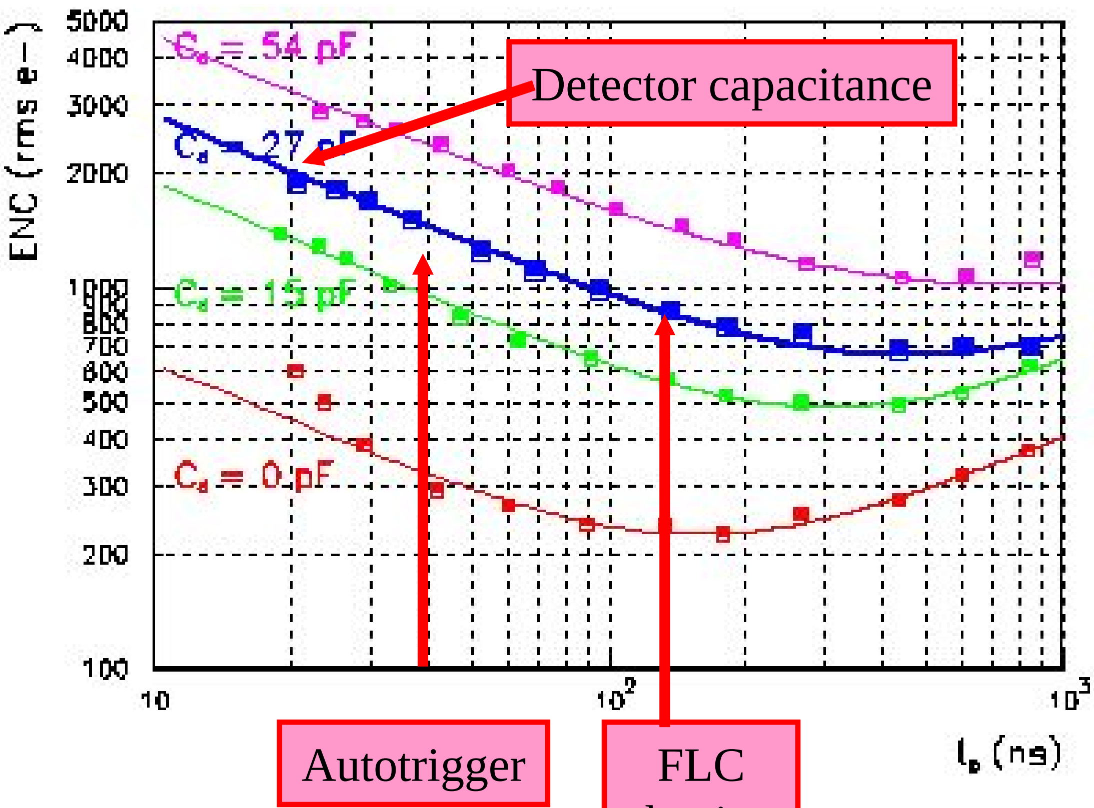
FLC_TECH1 layout AMS 0.35µ



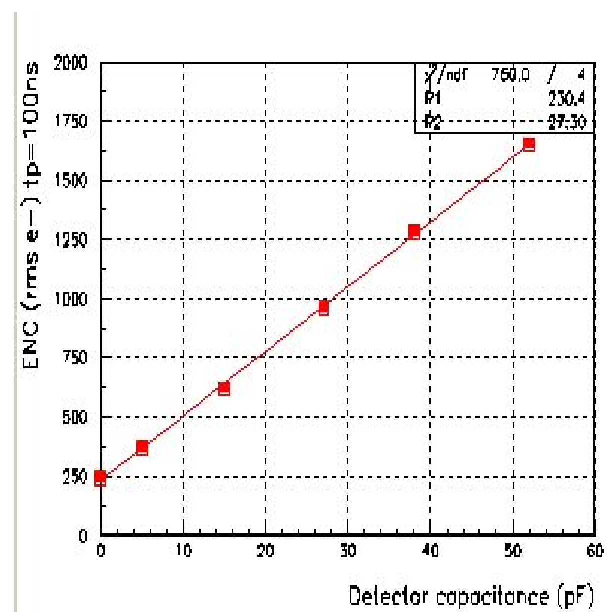
Pipeline ADC 0.35µ ©LPCC

FLC_TECH1 : noise performance

- **Moving to 0.35 µm SiGe AMS**
  - ENC = 1000 e- @ tp=100 ns & Cd=27pF
- **Target noise of ENC < MIP/10 = 4000 e- is (more than) achieved**



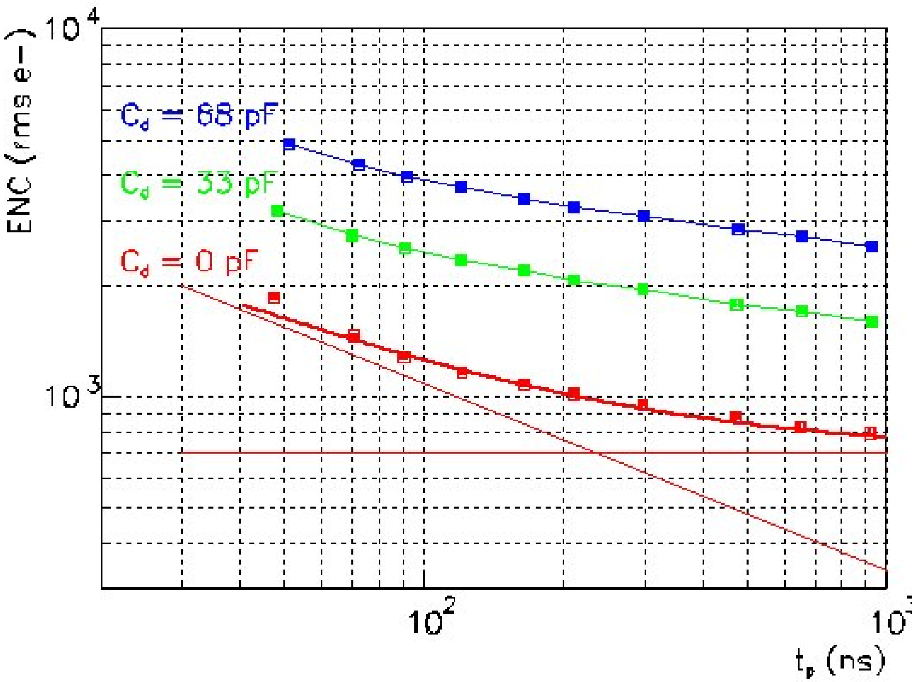
ENC vs shaping time FLC_TECH1



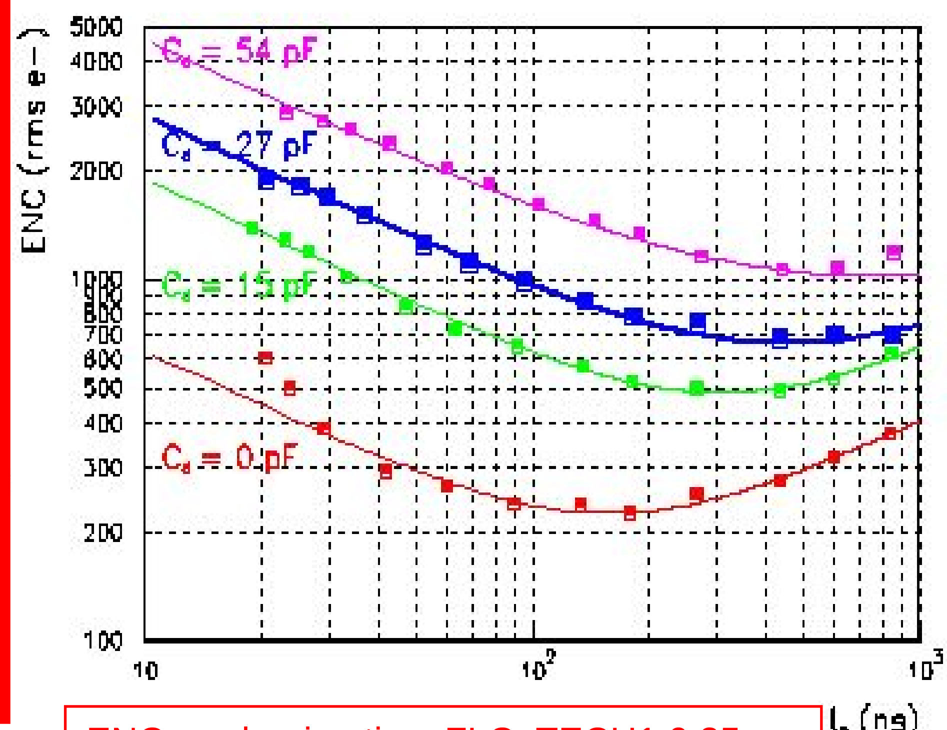
ENC vs Capacitance tp=100ns

FLC_TECH1 : noise performance

- **FLC_PHY3 : 0.8µm**
  - Series : e_n = 1.6nV/√Hz
  - C_{PA} = 10pF + 15pF test board
  - 1/f noise : 25e-/pF
  - Parallel : i_n = 40 fA/√Hz
- **FLC_TECH1 : 0.35µm**
  - Series : e_n = 1.4 nV/√Hz
  - C_{PA} = 7 pF
  - 1/f noise : 12 e-/pF
  - Parallel : i_n = 40 fA/√Hz



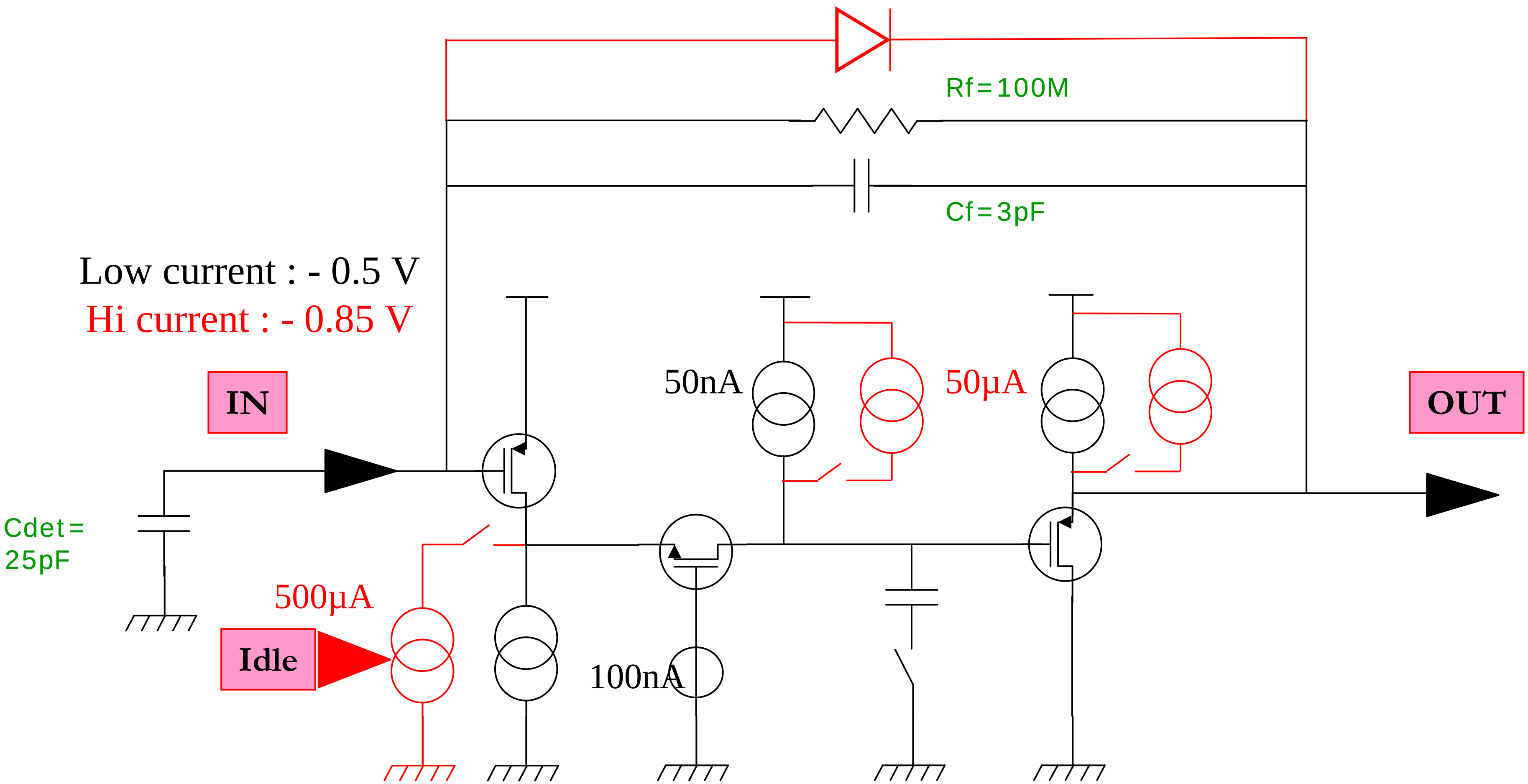
ENC vs shaping time FLC_PHY3 0.8µ



ENC vs shaping time FLC_TECH1 0.35µ

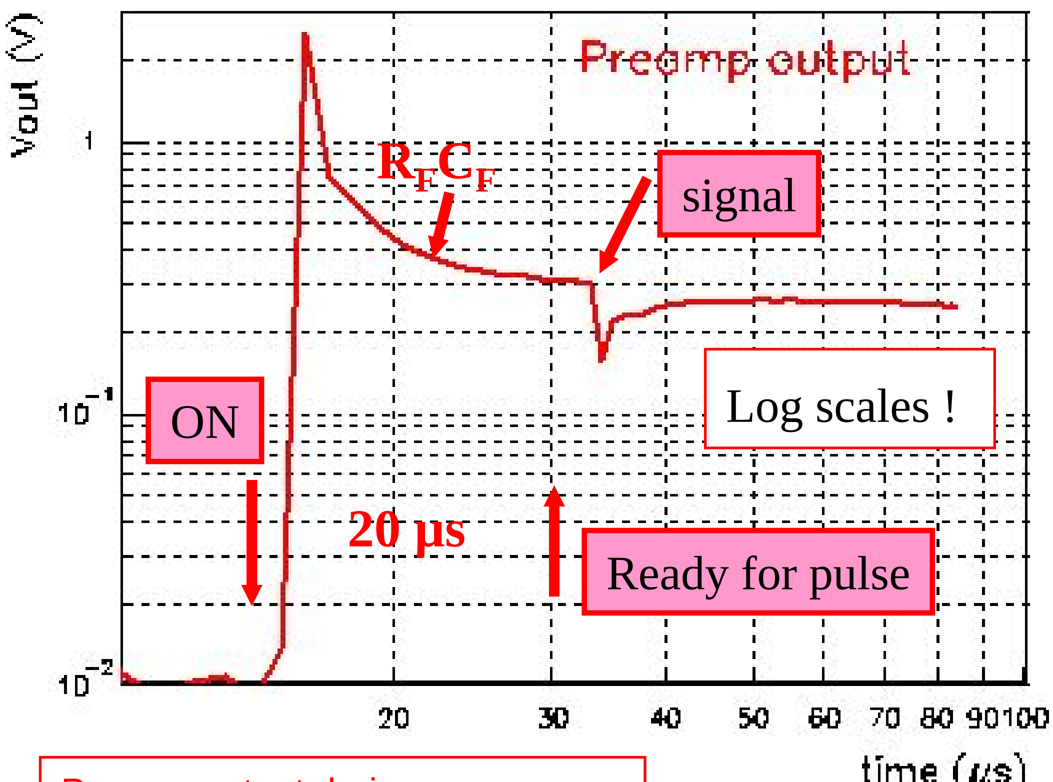
FLC_TECH1 : Power cycling design

- **Switching from idle current (i/1000) to nominal**
  - Change in operating point : V_{GS}(100nA) = 0.5 V -> V_{GS}(500 µA) = 0.85 V
  - Requires a large current i = Cdet dV/dt => antisaturation diode feedback

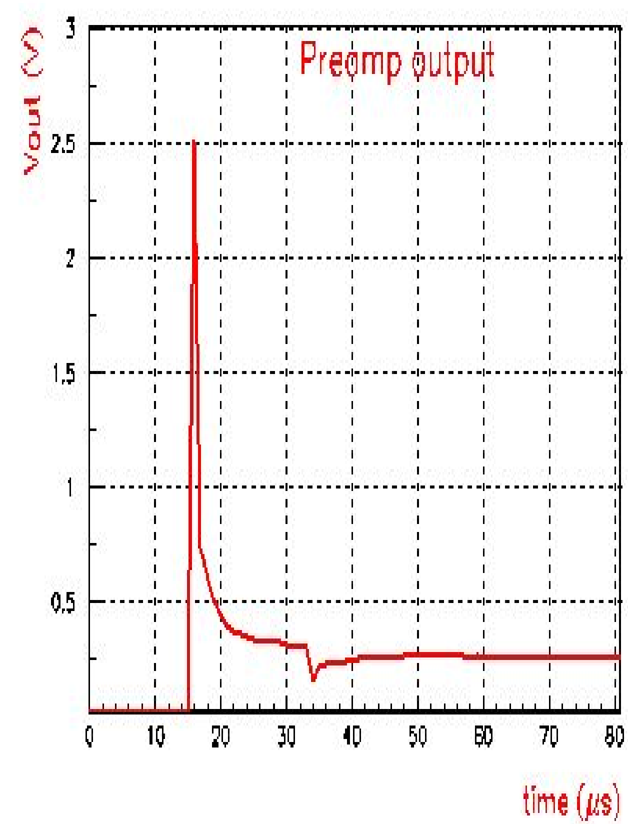


FLC_TECH1 : Power cycling results

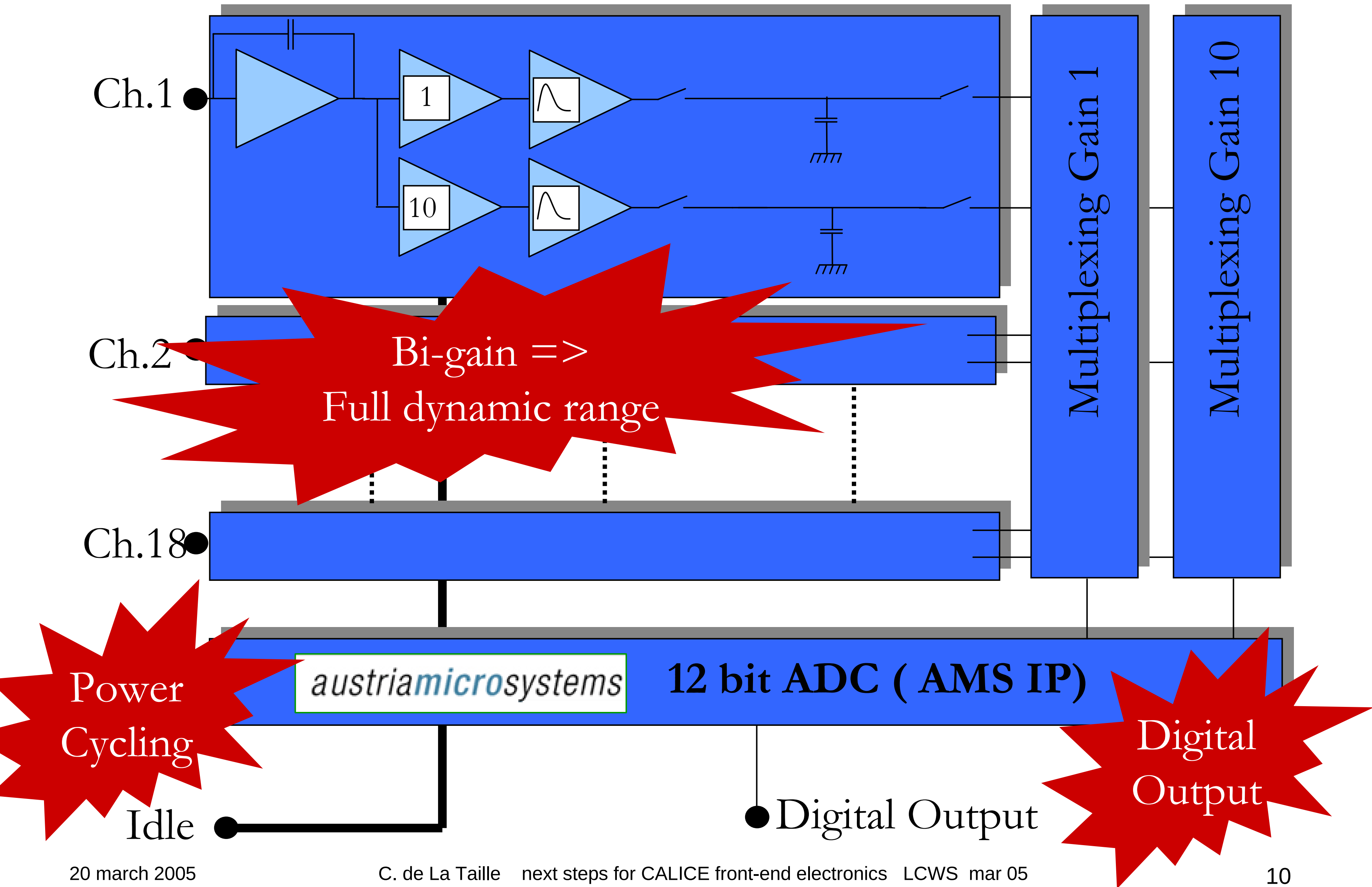
- **On-setting time < 20 µs**
  - Pulse amplitude and noise identical in pulsed mode than in steady mode
  - Allows to reduce power by 99% with beams 2ms/200ms
- **Target power of 100 µW/channel appears within reach**



Preamp output during power up

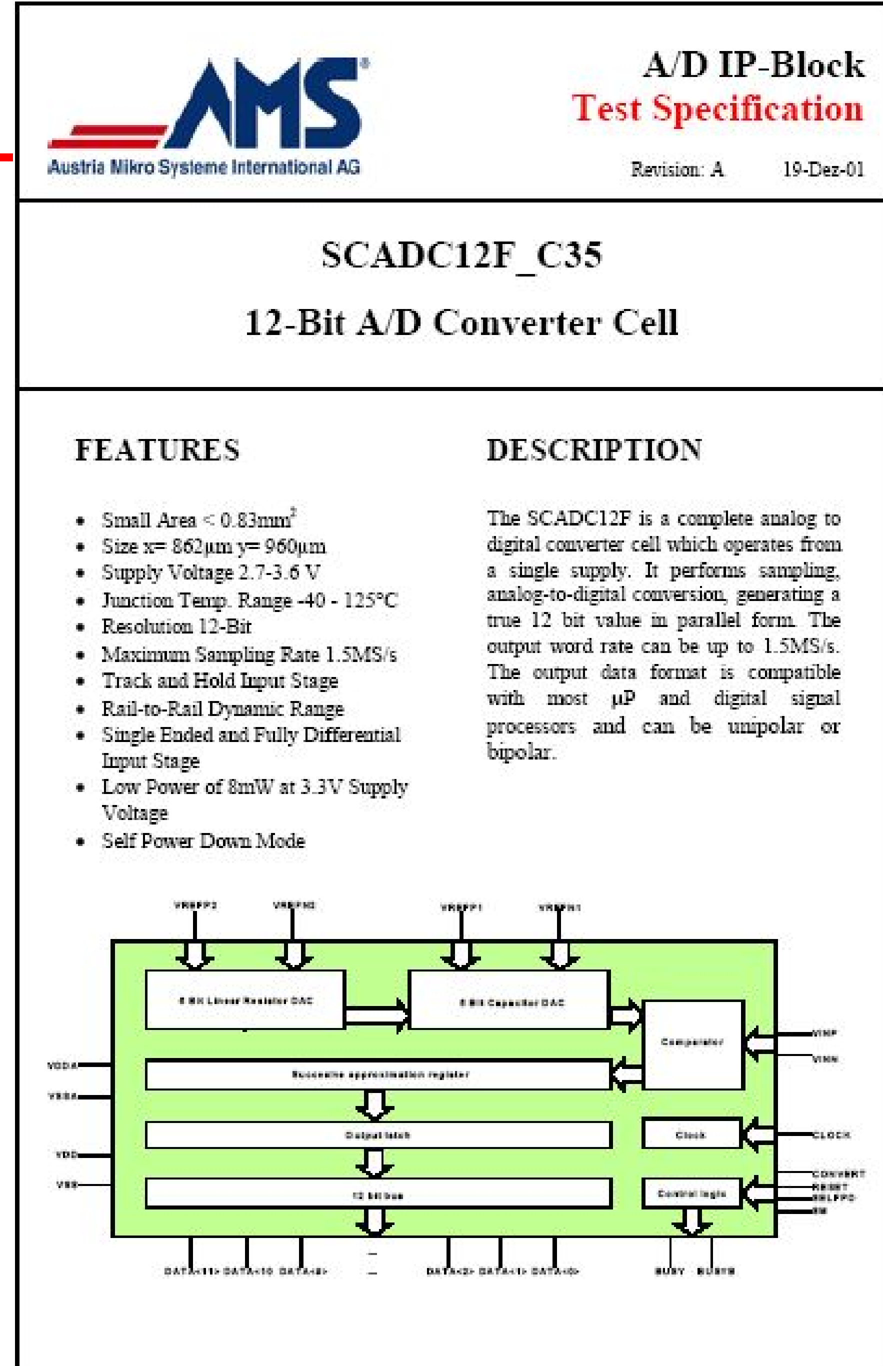


Next version : FLCPHY4



FLC_PHY4 design

- **Analog front-end :**
  - Same preamplifier as FLCTECH1
  - Extended dynamic range C_F->10pF
  - Shaper bi-gain G1-G10
  - Power pulsing
  - Differential Track&Hold + multiplexer
  - Internal bias
- **ADC : 12 bit 1MHz 8mW**
  - Commercial IP from AMS to start with
- **18 channels, Pd = 2mW + 8mW ADC**
  - To be submitted April 05 in AMS 0.35µ
- **What is still missing**
  - SCA
  - Zero suppress



AMS Austria Mikro Systeme International AG

A/D IP-Block
Test Specification

Revision: A 19-Dez-01

SCADC12F_C35

12-Bit A/D Converter Cell

FEATURES

- Small Area < 0.83mm^2
- Size x= 862µm y= 960µm
- Supply Voltage 2.7-3.6 V
- Junction Temp. Range -40 - 125°C
- Resolution 12-Bit
- Maximum Sampling Rate 1.5MS/s
- Track and Hold Input Stage
- Rail-to-Rail Dynamic Range
- Single Ended and Fully Differential Input Stage
- Low Power of 8mW at 3.3V Supply Voltage
- Self Power Down Mode

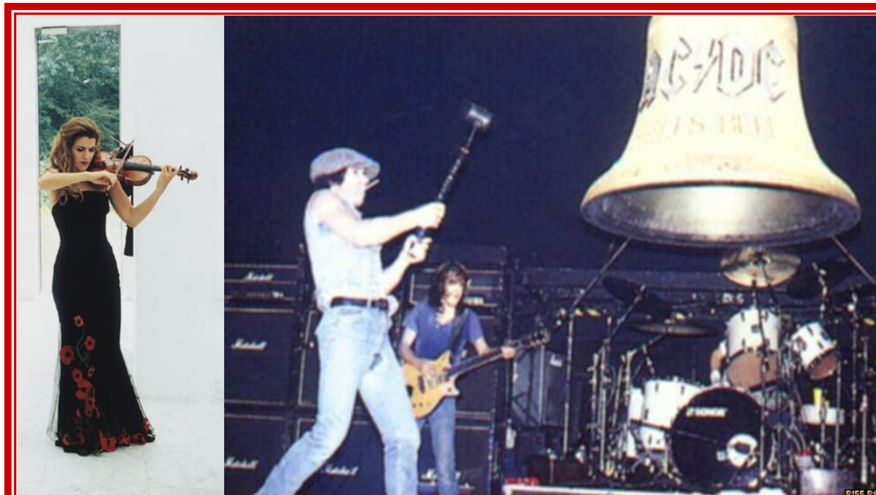
DESCRIPTION

The SCADC12F is a complete analog to digital converter cell which operates from a single supply. It performs sampling, analog-to-digital conversion, generating a true 12 bit value in parallel form. The output word rate can be up to 1.5MS/s. The output data format is compatible with most µP and digital signal processors and can be unipolar or bipolar.

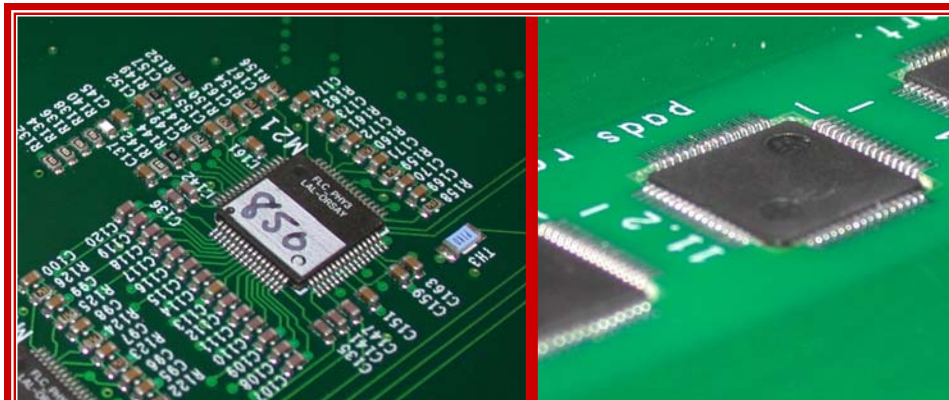
FLCPHY4 : main issues

Mixed signal :

High speed digital features & low noise amplifier on the same die.



Analog vs digital



No external component :

Reduce PCB thickness to 0.8mm
Need to internally decouple all biases and supplies.

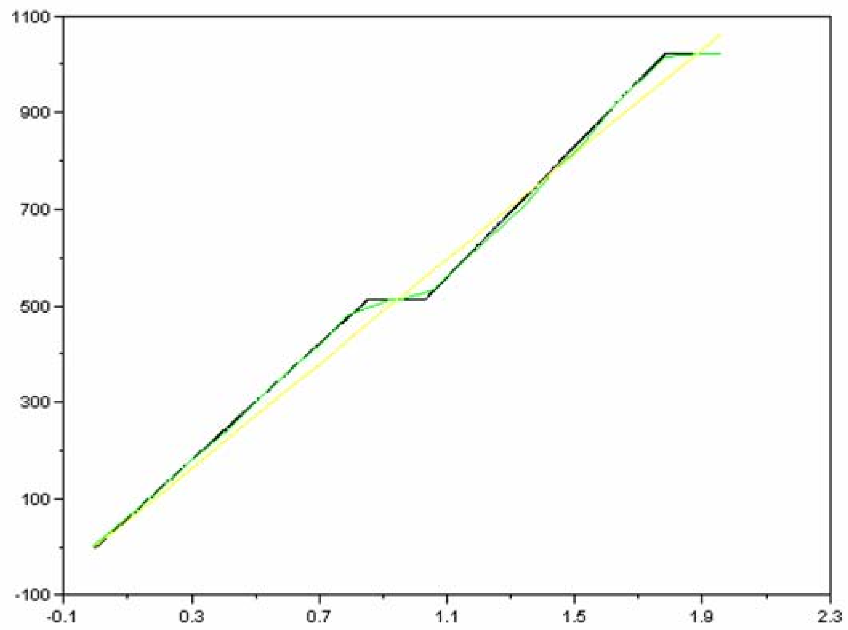
R&D on ADCs

- **Pipeline ADC**
  - 10bit 5MHz 8mW
  - Submitted in july 04
  - Status : under test
  - Non linearity needs to be fixed

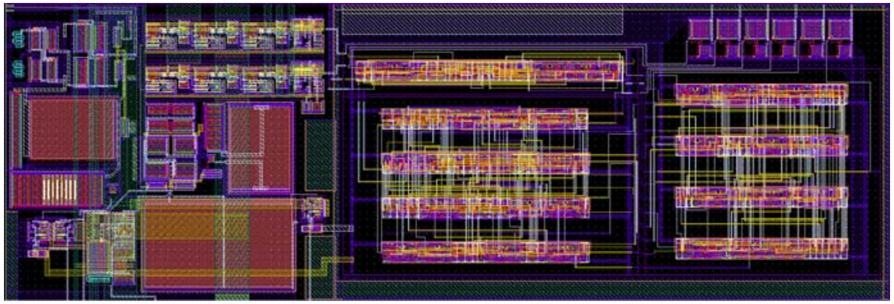
- **SAR ADC C/2C**
  - 10bits 1 MHz 1mW
  - Submitted in AMS 0.35µm
  - Status : Waiting to be tested

- **Wilkinson**
  - 12bit 10kHz 2.5mW
  - Submitted in dec 04

- **Still a long way to go…**



Measured linearity of Pipeline 10 bit ADC

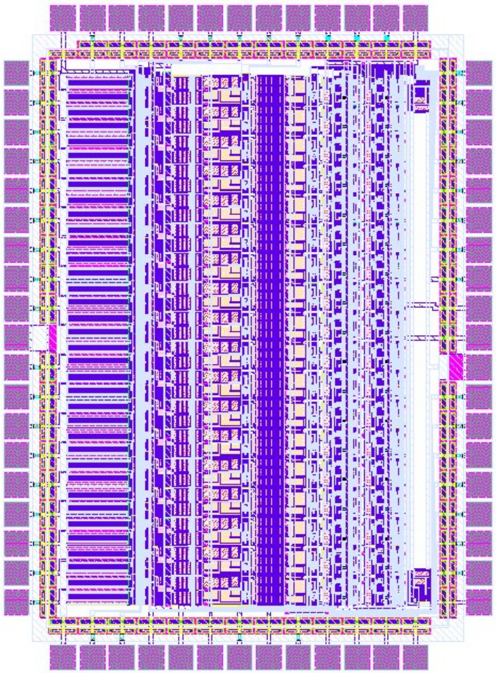


Layout of Wilkinson 12bit ADC

Conclusion

- **FLC_TECH1 in 0.35 µm**
  - 30 µW in pulsed mode
  - ENC = 1000e- @ Cd=27pF (measured)

- **FLC_PHY4 in 0.35 µm**
  - Similar to FLC_PHY3 (18ch)
  - Will integrate a 12 bit ADC
  - Will allow Power pulsing
  - Will cover the 0.05-3000 MIP dynamic range
  - Will have no external components
  - Can be tested with test beam prototype
  - Will be submitted in April 05

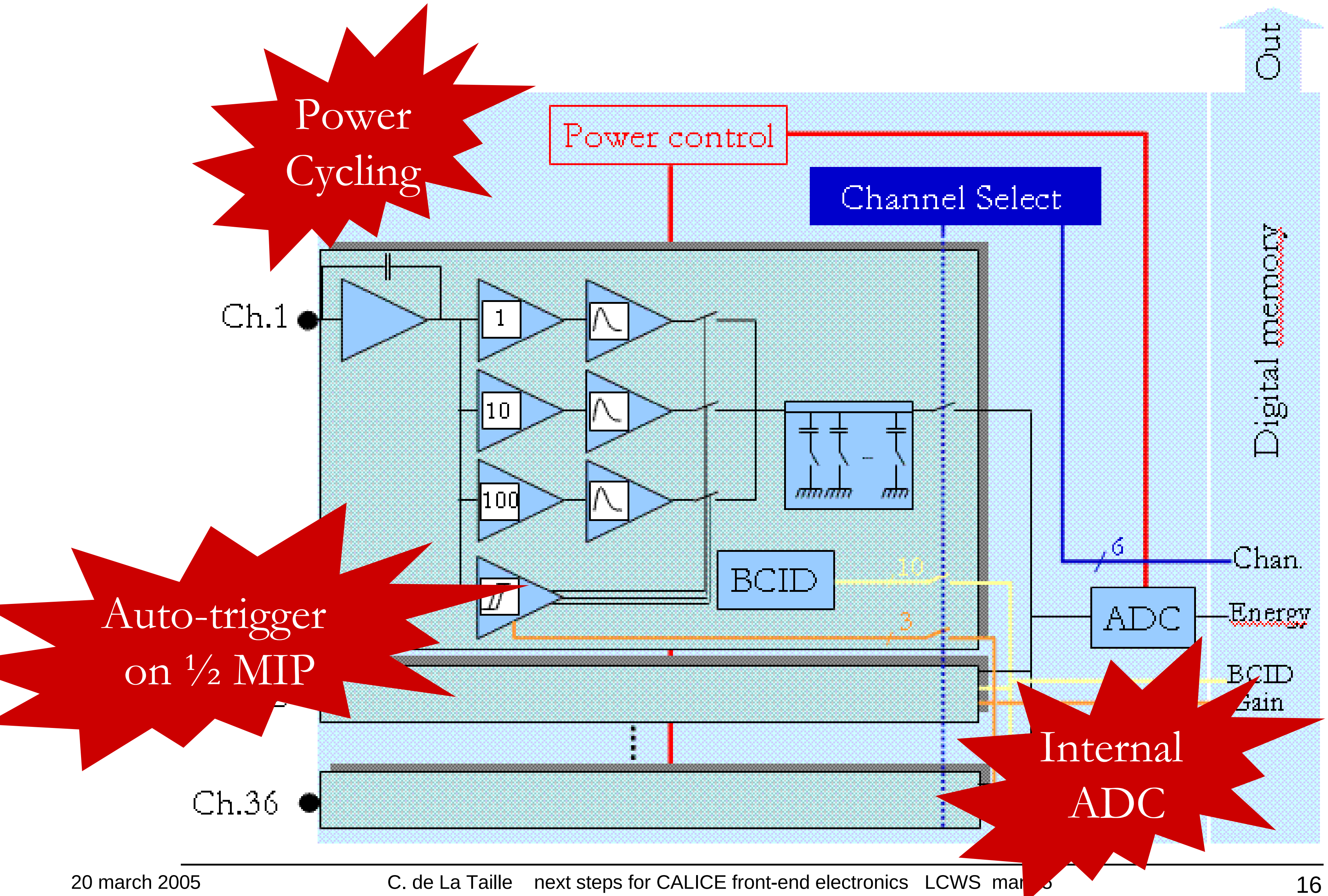


- **The key issue of low power (100 µW/channel) now looks under control**

- **Now ready to design module 0 front-end electronics**

Backup slides

ECAL Front-End ASIC



R&D on ADCs : pipeline

10 bits low power high speed pipeline ADC

LPC Clermond-Ferrand, Fr

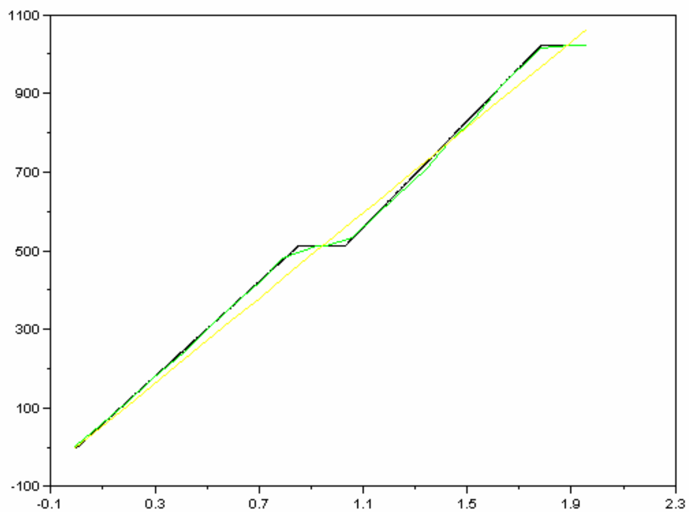
- -Gerard Bohner
- -Pascal Gay
- -Jacques Lecoq
- -Samuel Manen

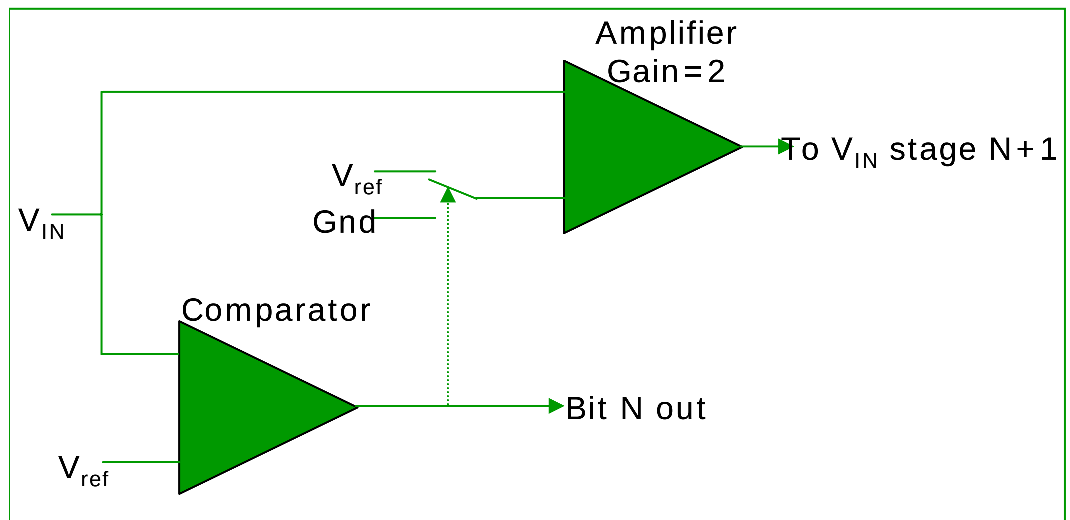
Performance

- -10 bit
- -up to 5MS/s (Clk @ 50 MHz)
- -Consumption around 10mW

Status

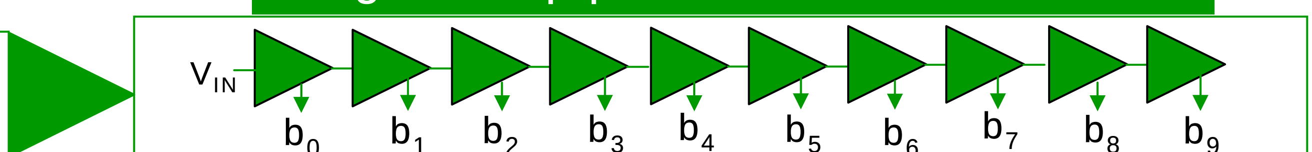
- -First iteration (AMS 0.8 CMOS) is working well
- -New iteration (AMS 0.35 CMOS) submitted in April, 19th





Stage N of pipeline ADC block schema

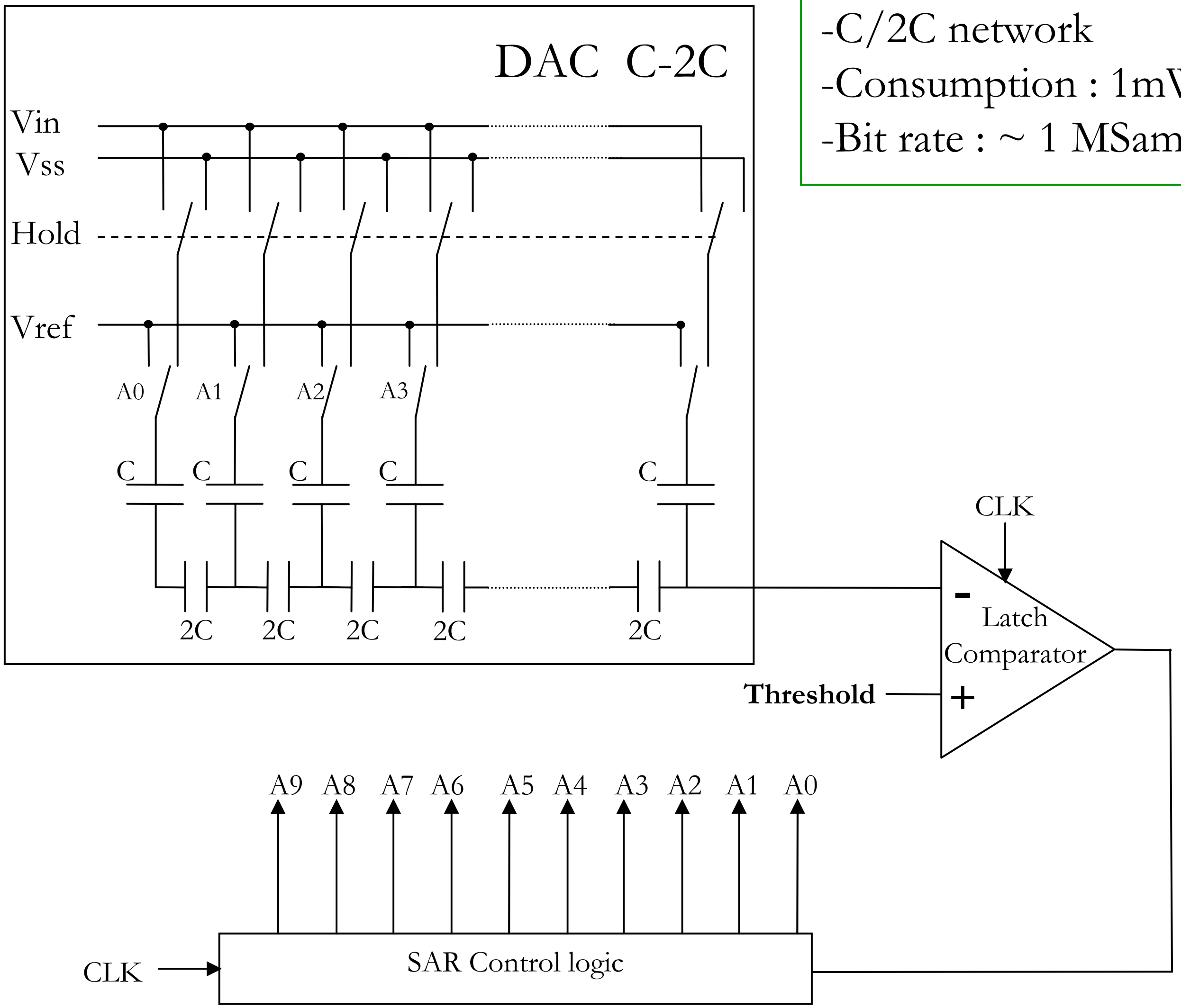
10 bit ADC
→10 stages



R&D on ADCs : SAR C/2C

SAR (successive approximation) ADC

- -10 bits
- -C/2C network
- -Consumption : 1mW
- -Bit rate : ~ 1 MSamples/s



FLC_TECH : a first iteration

FLC_TECH description

-3 channels
-Multi-gain charge preamplifier
-2 shaping : gain 1 and gain 10
-5-depht SCA
-Multiplexed output, auto-trigger and Idle mode

Technology	AMS 0.35 CMOS
Submission	April, 19th 2004