Fermilab ASIC and electronics R&D for Linear Collider

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Fermilab

Outline

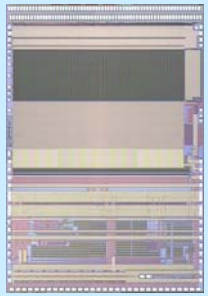
Capabilities

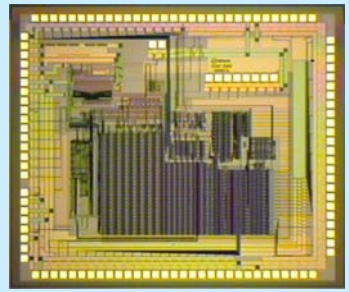
Existing work

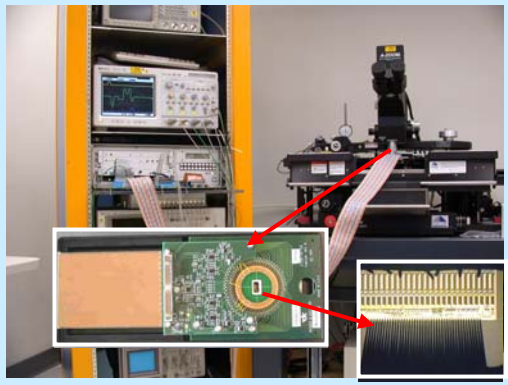
Future work

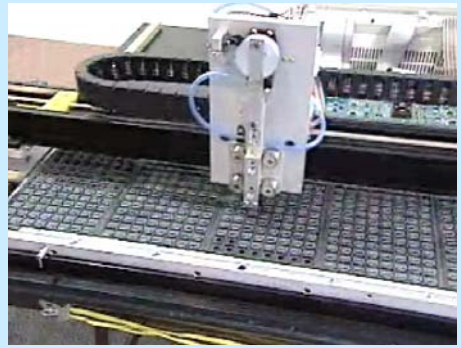
Capabilities

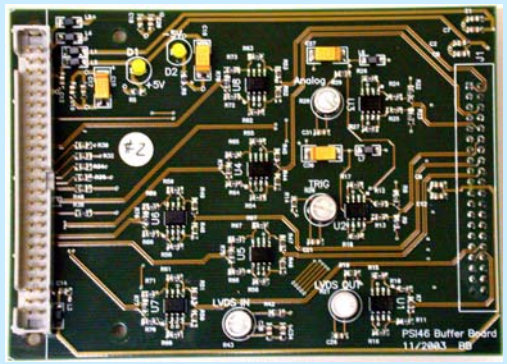
- Five ASIC engineers
  - Analog front-end
  - Digital designs
- Testing group
  - Wafer probing
  - Robotic testing
- Board level design
  - Engineering
  - Layout
  - Technical

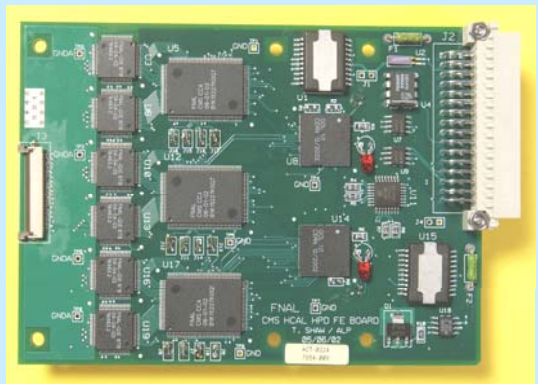








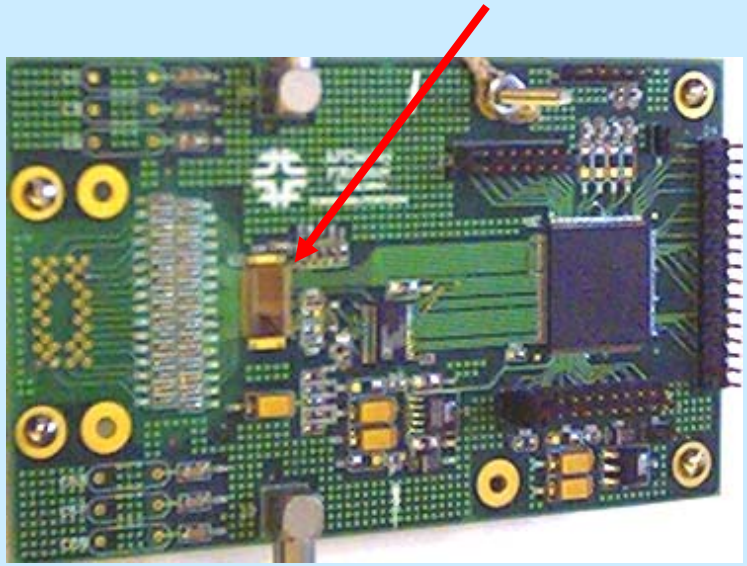




Calorimeter electronics

- Long history of FNAL EED group's involvement in calorimeter electronics: KTeV, CDF, CMS, etc.
- New efforts for neutrino experimentation (Nova, Minerva) are considering technologies that overlap with the proposed LC calorimeters – Large channel counts!

- *Avalanche Photo Diodes* (APDs) can be read out using electronics based upon FNAL-developed MASDA ASIC
  - Demonstration readout boards have been produced for neutrino efforts. One board is possible for LC digital calorimeter R&D.
- New ASIC design based upon MASDA is under development
  - Very flexible, different modes
  - 32 channel device



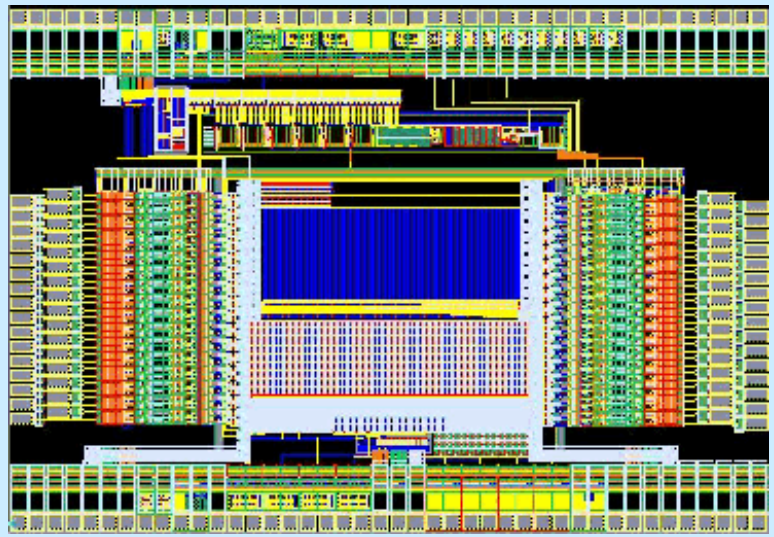
Digital Calorimeter R&D

- "Digital calorimeter" concept uses fine granularity to count hits (proportional to energy) in an "energy flow algorithm." Concept needs demonstration in test beam.
  - RPC readout (Argonne et al) [overlap with Nova R&D]
  - GEM readout (U Texas, Arlington et al)
- 400,000 channel 1m^3 R&D device

DCAL designed for two gains

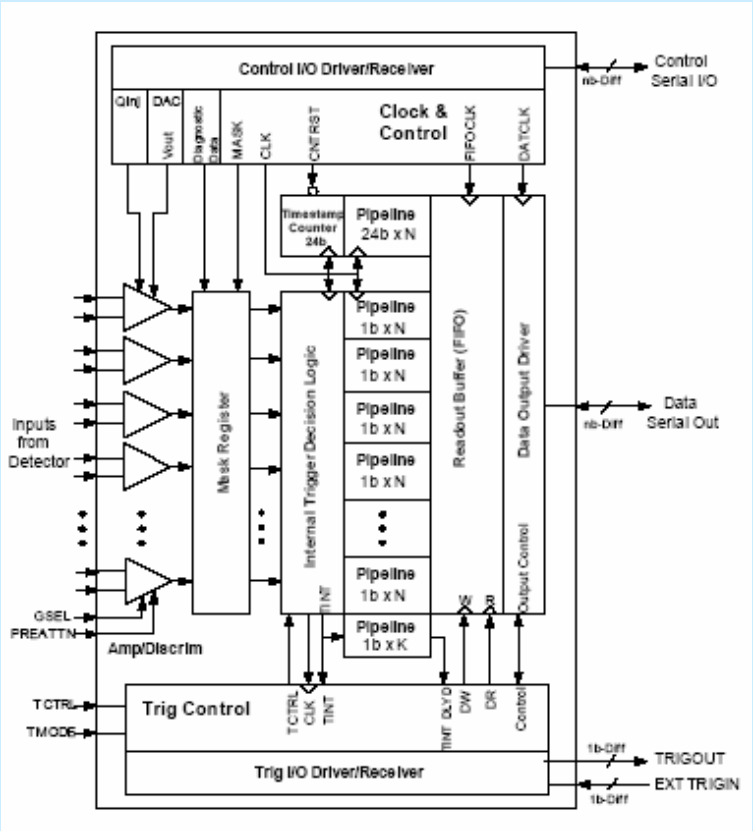
- New ASIC development effort,

the *DCAL chip* - a digital calorimeter readout chip. ASIC design work is nearing completion for submission on March 21 (tomorrow!).

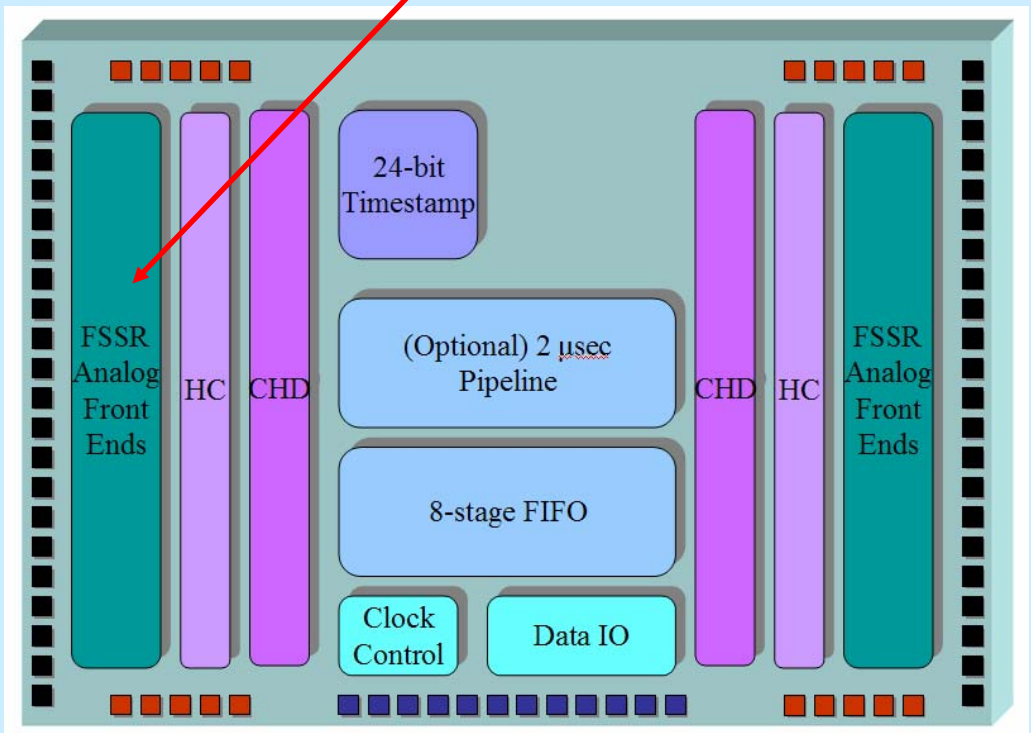


DCAL ASIC

64 channels with input gain either for RPCs or GEMs
Triggerless or triggered operation
100 ns clock cycle
Output is a hit pattern and time stamp

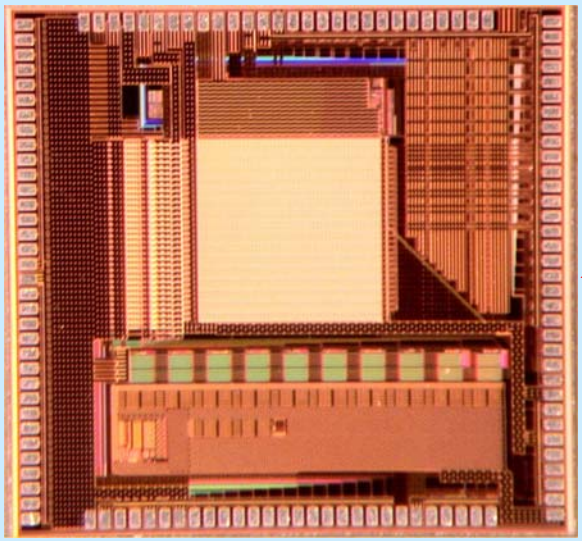


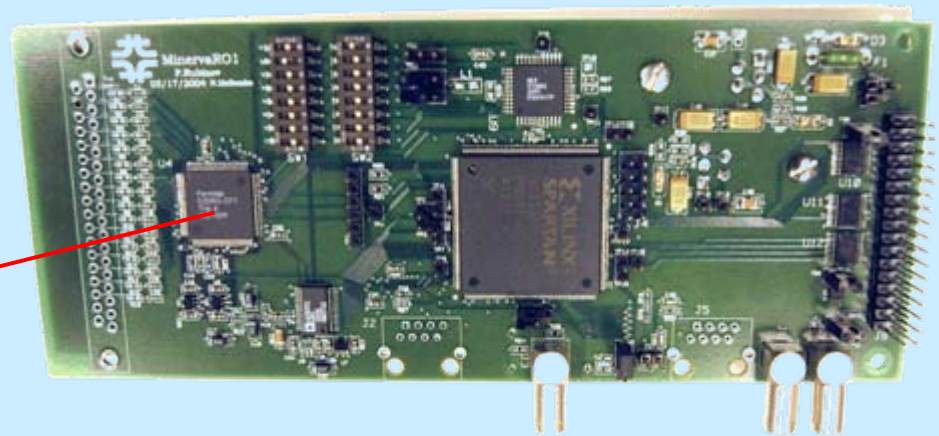
BTeV silicon strip front-end



Trigger Pipeline (TriP) ASIC

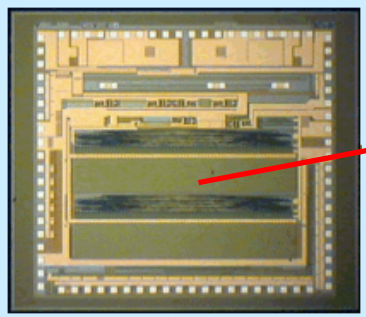
- ASIC designed for D0 fiber tracker
- Scintillator readout useful for Minerva (neutrino's)
- Work to investigate device for ILC muon system
- Pre-amplifier, pipeline, trigger – new device with timing
- Large dynamic range 5-5000 fC
- 32 channels

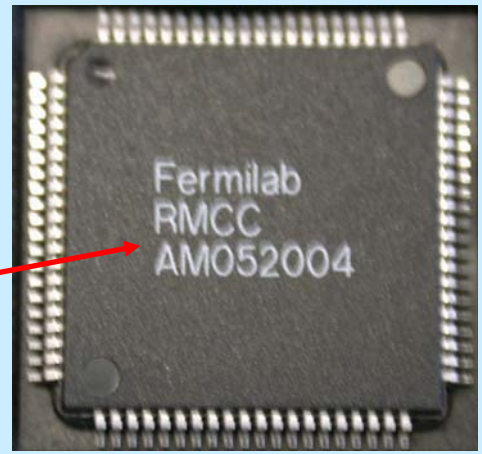




High voltage control ASIC

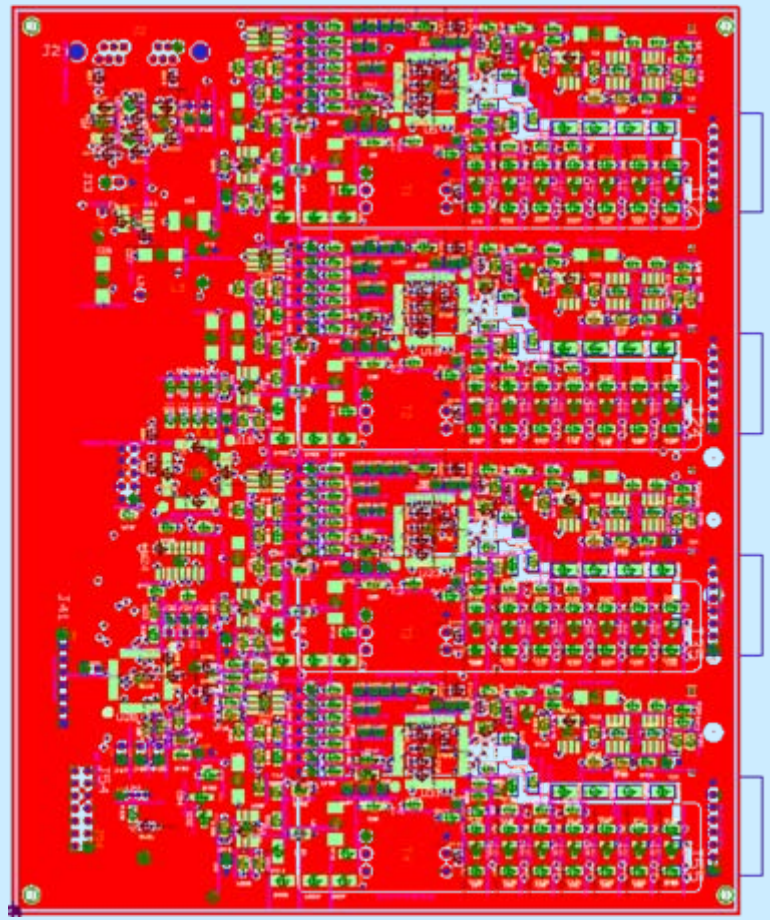
- The RMCC (resonant mode converter chip) is a long standing FNAL circuit design now implemented in a FNAL ASIC. High voltage/low current uses such as phototubes, bias supplies, etc.
- New detectors with many many HV channels will benefit from low cost Cockcroft-Walton with this control ASIC (additional safety benefit of generating HV locally)
- Status: prototype chip works and has been used for PM supply. Parts back from packaging. Work proceeds on a demonstrator printed circuit board for bias voltage.





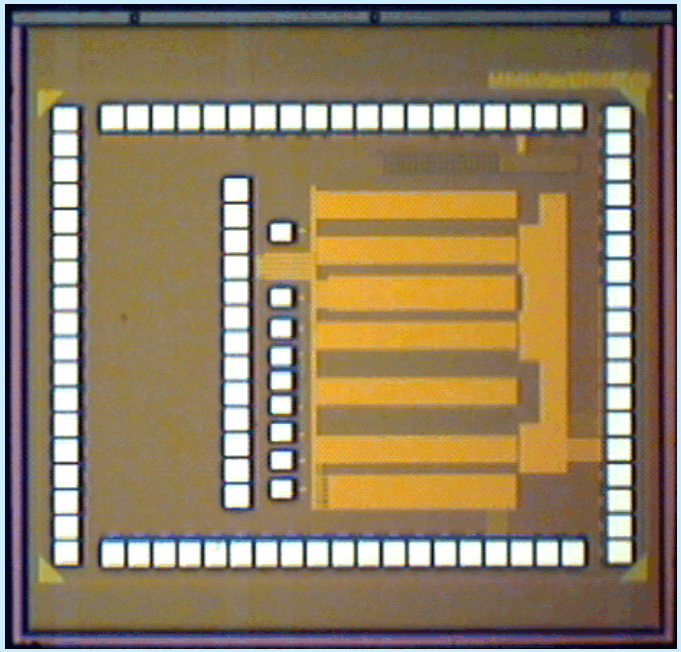
RMCC (cont)

- **Resonant Mode Converter Chip**
  - Useful for LC detector R&D, Off-axis neutrinos, education, etc.
  - Voltage control chip to be used with external step transformer
    - Serial programming interface with 12 bit DAC
    - 12 bit ADC for voltage and temperature read back
    - Polarity programmable
    - ~100μa @ 1000 V
    - Up to 5KV possible, higher with special drive circuit
    - Low ripple ~0.1%
  - **Four-channel demonstration board** has been **fabrication** (LC and neutrino support)



0.13 μm ASIC R&D

- First FNAL device in 0.13μm CMOS
- Test device with pixel cell, and various test structures
- Work in 0.13μm also at LBNL and in Europe



Note: top metal layer hides many of the structures

Current 0.25μm will disappear
Challenge for analog design
Reports of better rad tolerance
Masks are very expensive now
0.25μm($150K)->0.13μm($500K)
but cost of silicon/area similar

Monolithic Active Pixels

- Efforts have been going on world-wide
  - FNAL ASIC engineer contributed to early work
  - Mimosa ASIC devices (Strasbourg) exist
  - Several other efforts
- New efforts in US have started
- FNAL ASIC engineering group has started some collaborative discussions and is planning it's next steps in MAPs R&D
- FNAL physicists interested in MAPs
  - Linear collider R&D
  - Upgrades to LHC experiments

Conclusions

- There has been successful identification of overlapping needs between current and future FNAL projects and Linear Collider detector R&D.
- FNAL has supplied the engineering effort and projects have provided most of the M&S. There has been some cost splitting between LC and other initiatives.
- We have built real hardware: boards and ASICs.
- Fermilab is positioned to continue to contribute to Linear Collider detector R&D in this manner.
- Through this involvement, FNAL is also positioned for leadership roles in LC detector ASIC and electronics R&D.