CERN Beam Test of Silicon-Tungsten Calorimeter Test Module

Shinwoo Nam (Ewha Womans University)

Content: Silicon Sensor, Calorimeter Test Module,
Beam Test and Data Plots

On behalf of
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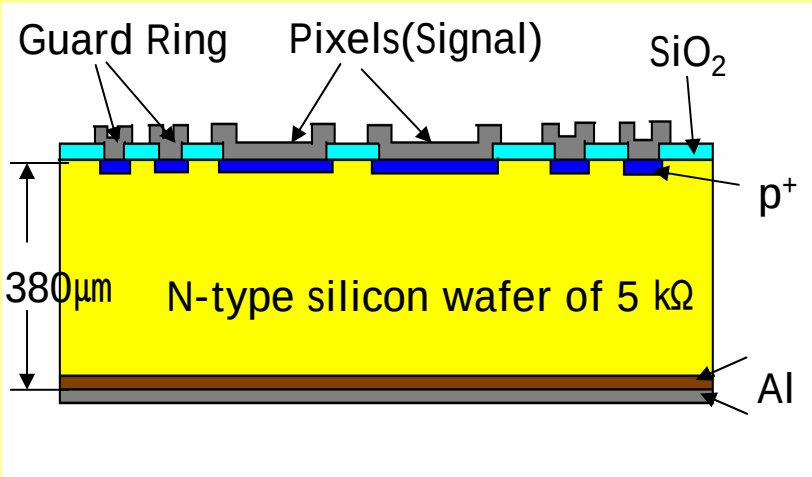
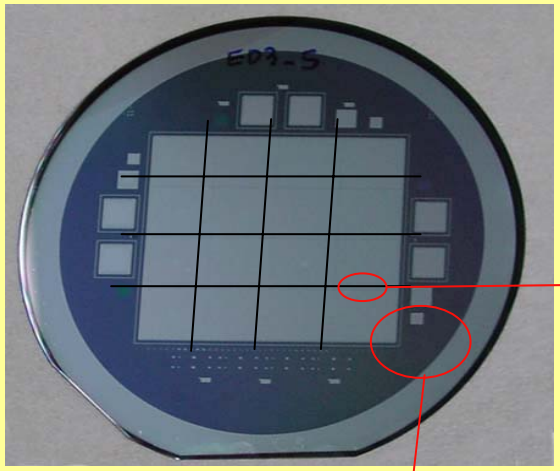
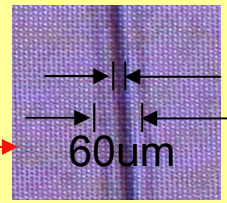
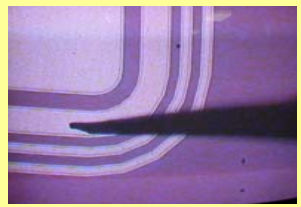
Silicon Sensor (Pixellated PIN Diode)







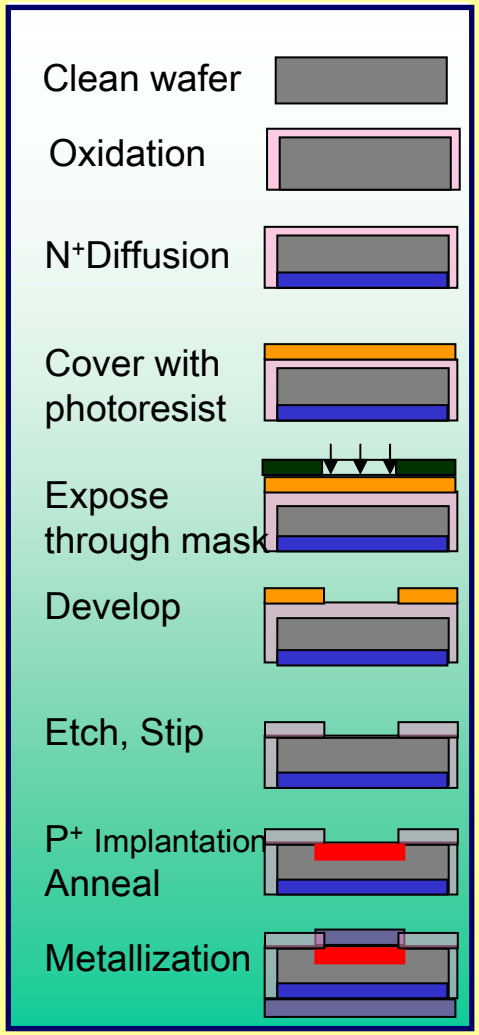


3 Guard Rings

- **Fabricated on 380um 5' wafer**
- **A Sensor Size : 6.52*5.82 cm^2 (including 3 guard rings)**
- **Pixel array : 4*4 matrix**

  1.55 * 1.37 cm^2 each
- **DC coupled**
- **Full depletion voltage : 90V**
- **Leakage current level : about 3 nA per pixel at full depletion voltage**

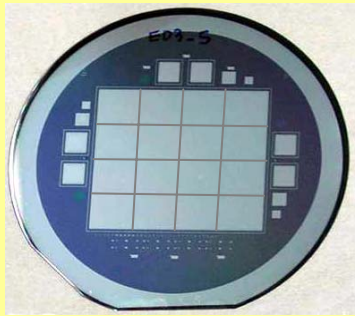
Process of Silicon Fab, Sawing, Bonding



Fabrication process

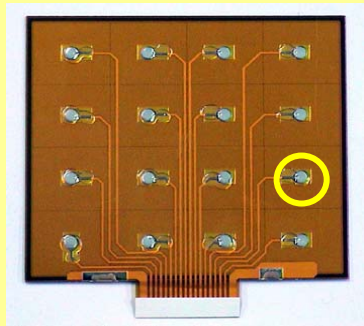
Wafer -> Fabricated PIN diode matrix

Mass Production Fabrication made at SENS Technology (www.senstechnology.co.kr)



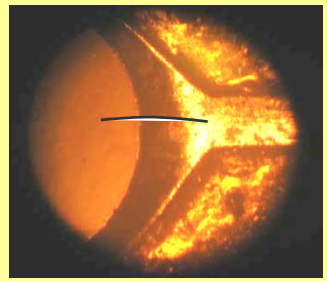
Sawing / attach Kapton tape

Kapton tape has patterned Cu wiring(50um) on it for readout

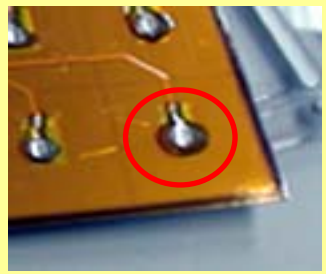


Wire bonding

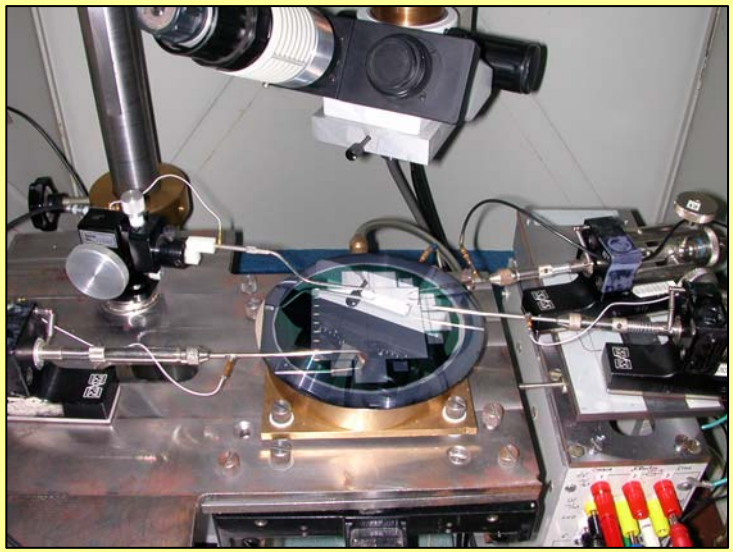
For wire boning to the diode pixel, Al wire with diameter 25 um was used. Recently we added one more wire to reduce risk of bonding failure



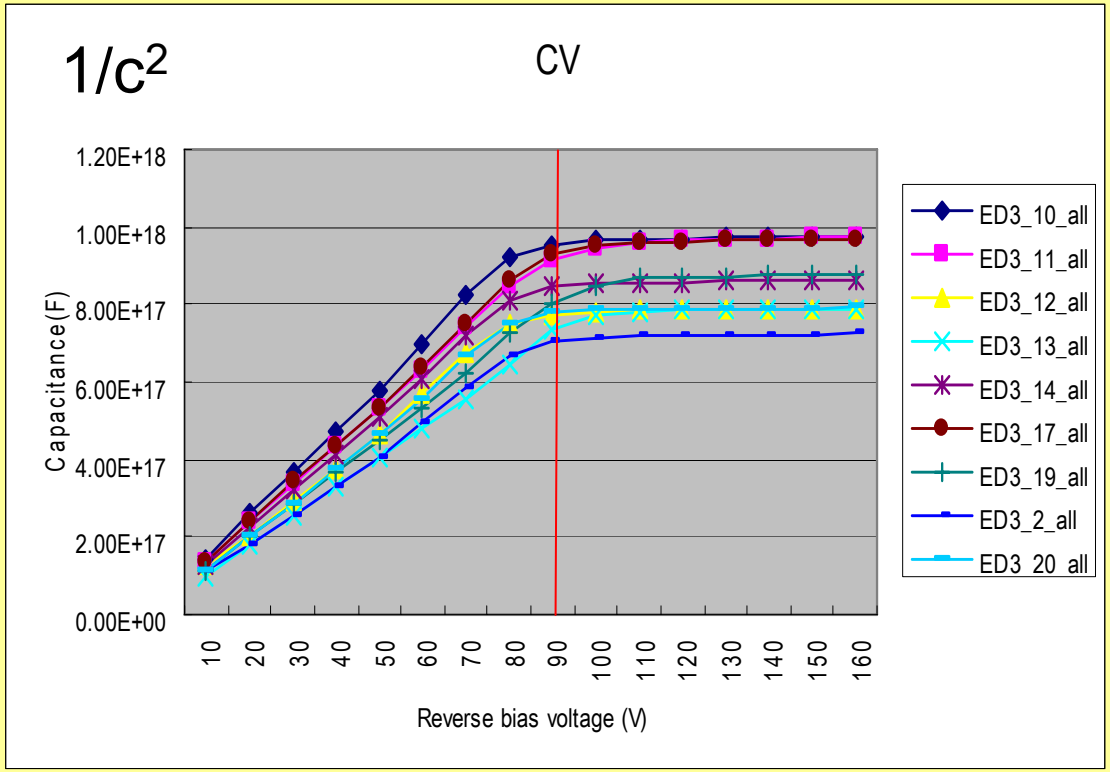
Glob Top (DCE, DP100)
For protection of bonded wire.
It is important to put the glob top in Vacuum to remove the air bubbles in glue.



Capacitance Measurement



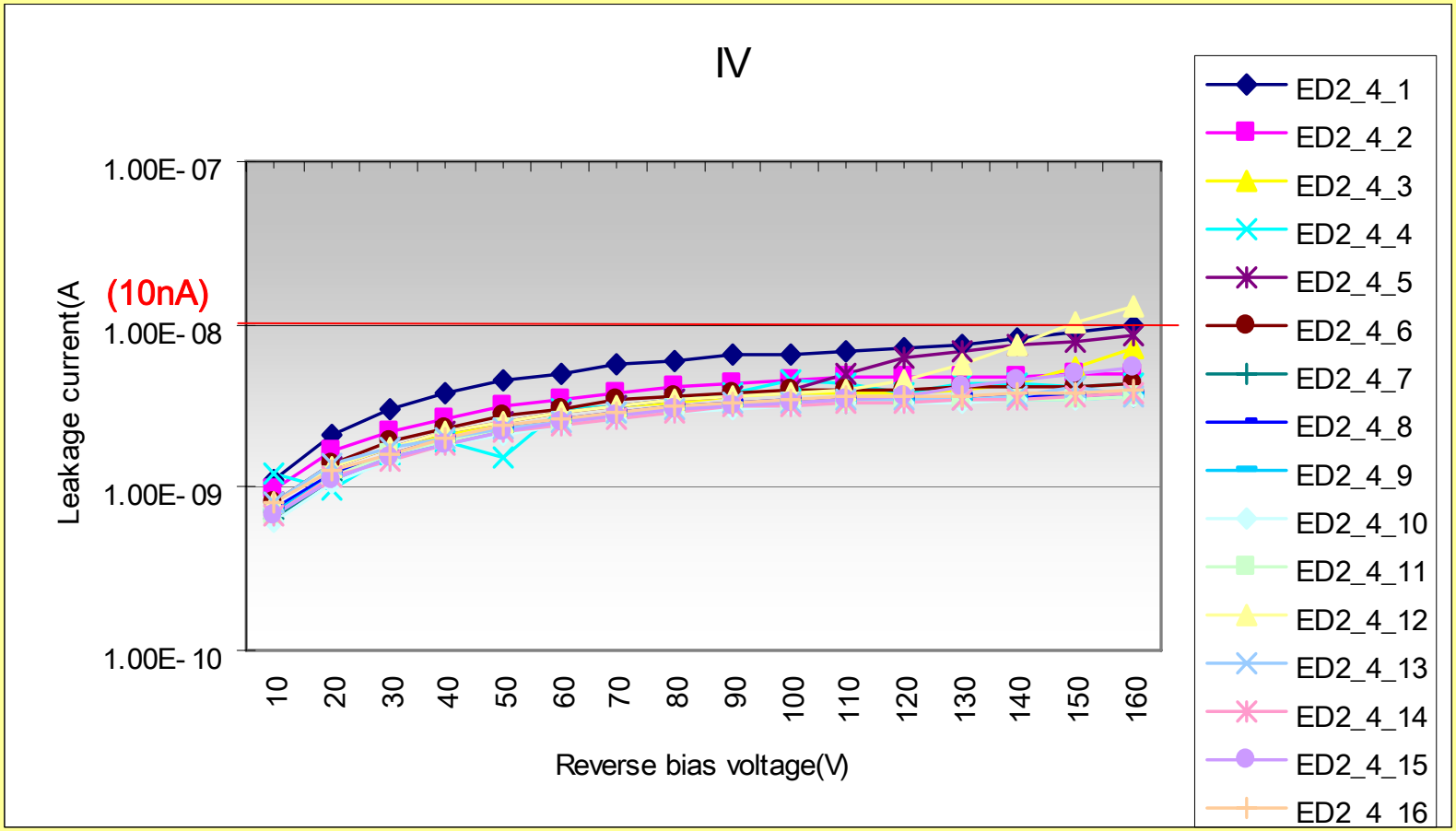
$$V_{dep} = V_{bi} - \frac{d^2}{2\epsilon\epsilon_0\mu_n} \cdot \frac{1}{r}$$



Full depletion voltage for 5kOhm wafer sensor: about 85-90V

Applied 100V because of variation in the thickness and resistivity of wafers

Leakage Current Measurement

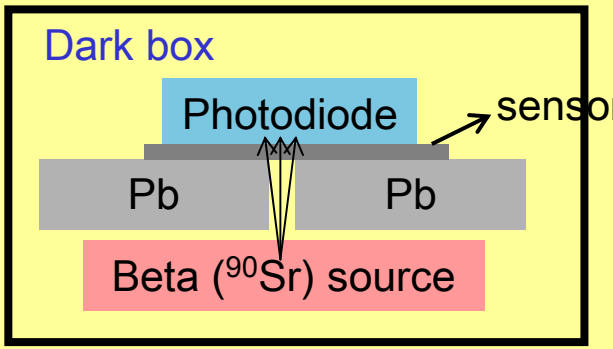


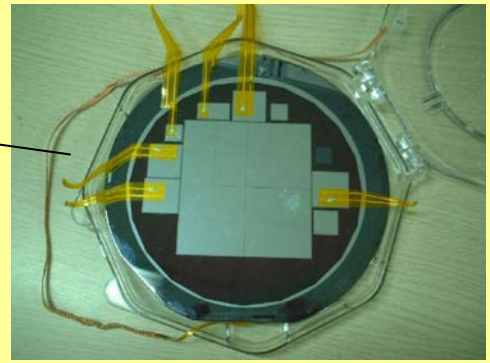
~3nA per pixcel at full depletion voltage !

Close to 90% yield with quality cut of 20nA/pixel at 100V !

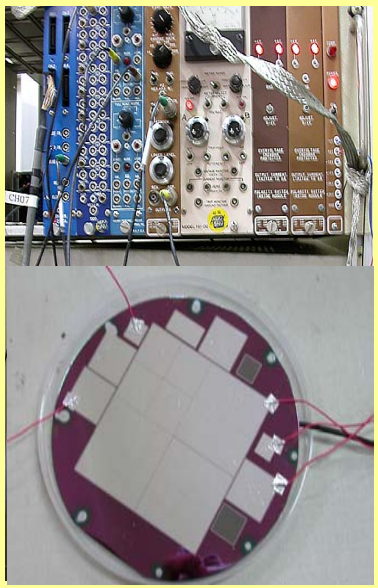
S/N Ratio Measurement with Sr-90 source

(use of single channel very low noise preamp)

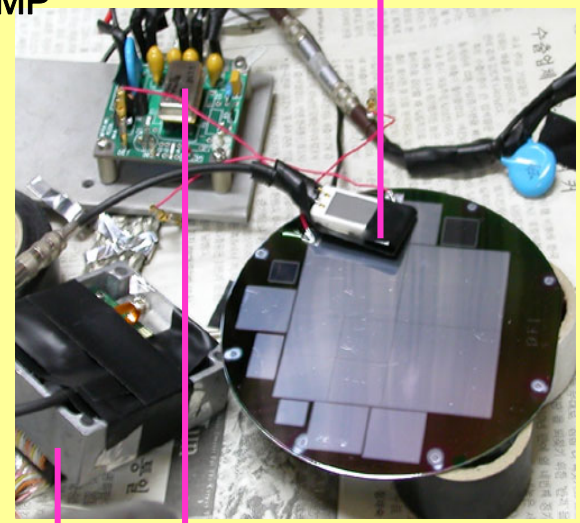


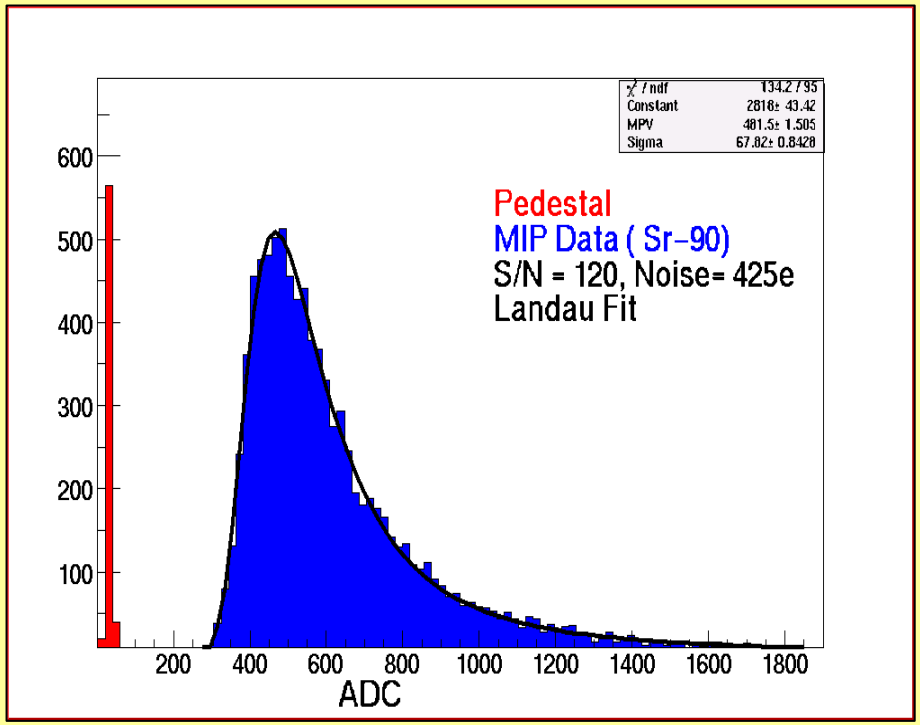


Discriminator
Gate Generator
Shaping AMP

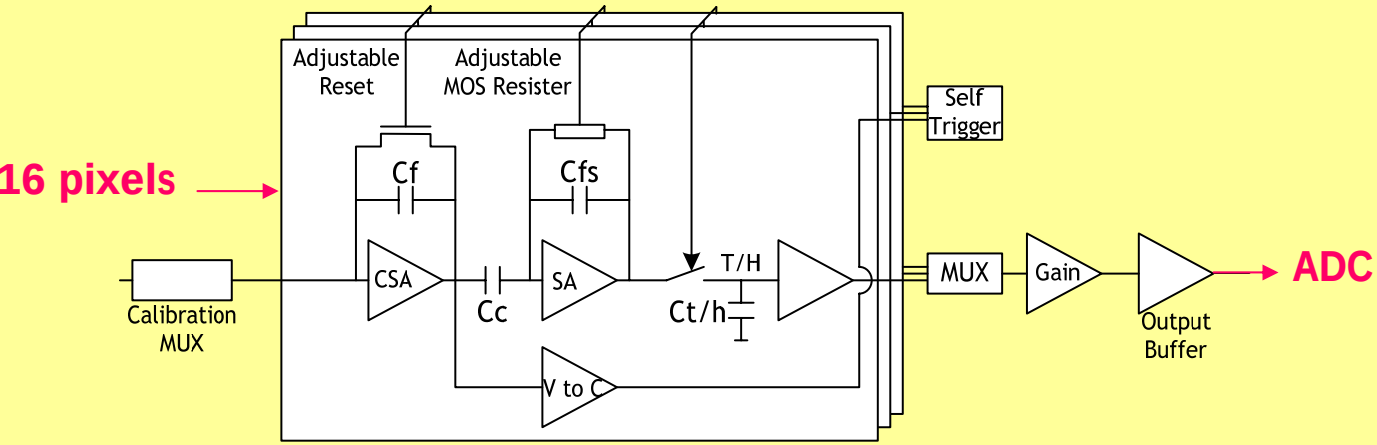


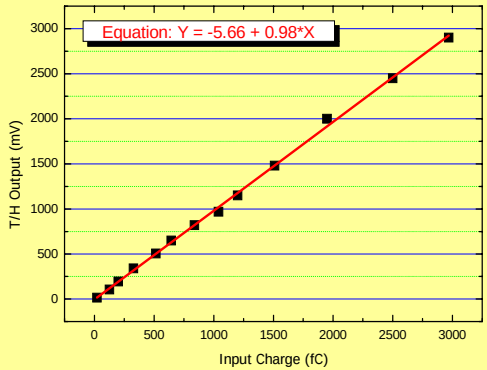
Trigger
Photodiode





Frontend Readout with CR1.4 chip

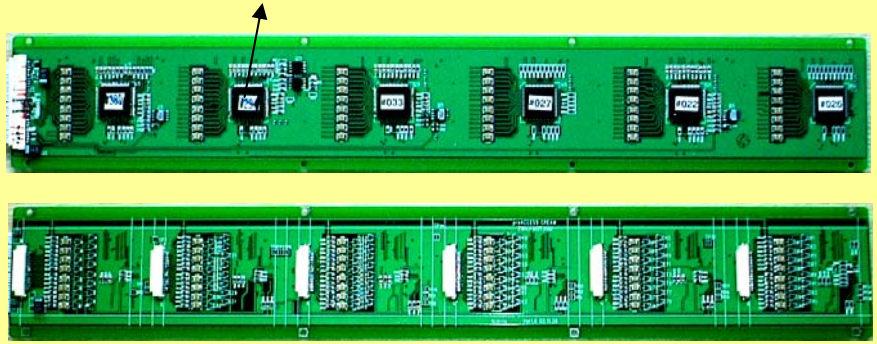




Gain Linearity Test
Using charge calibration
Function of chip

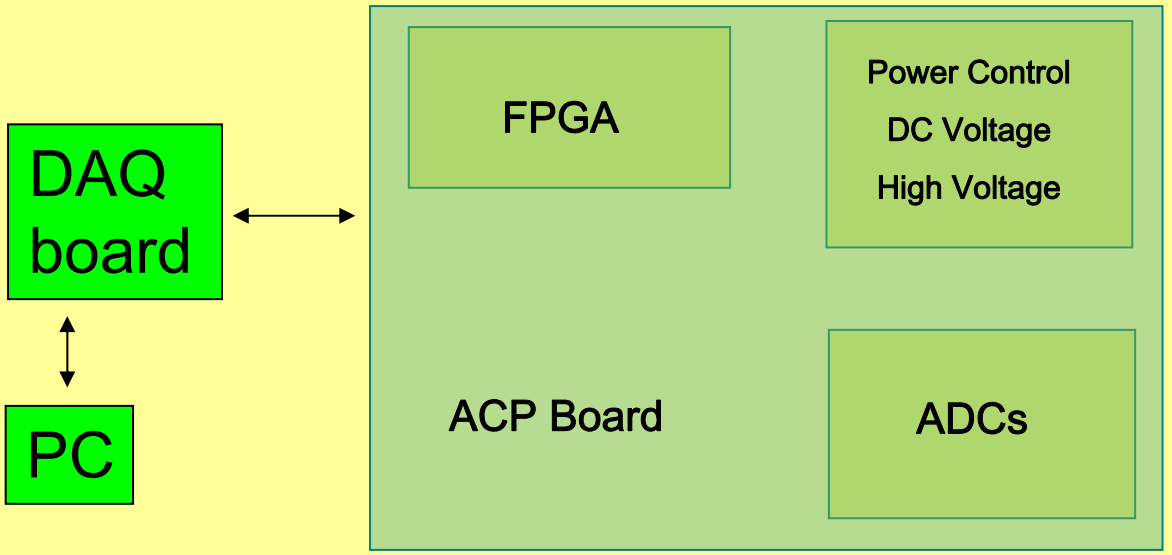
- Developed for the Pamela Experiment
- **16 channels of charge inputs (integrating the charge pulses -> DC levels)**
- **Gain: 1mV/fC**
- **Dynamic Range: to 4000 MIPs**
  - **up to 150 pF capacitance with leakage currents as high as 100 nA. It measures charge from 2.2 fC to 9 pC.**
- **Noise ~ 5000 e**
- **Power: 0.3 mW/ch**
- The outputs of the T/H circuits are multiplexed to a common output buffer that is capable of driving a load of 1k and 100 pF.
- The output of the chip swings from -3V to 4V

CR1.4 chip handles a 16-ch Si sensor



PCB Ladder Prototype

Digital Electronics : ADC, Contorl, Power Board

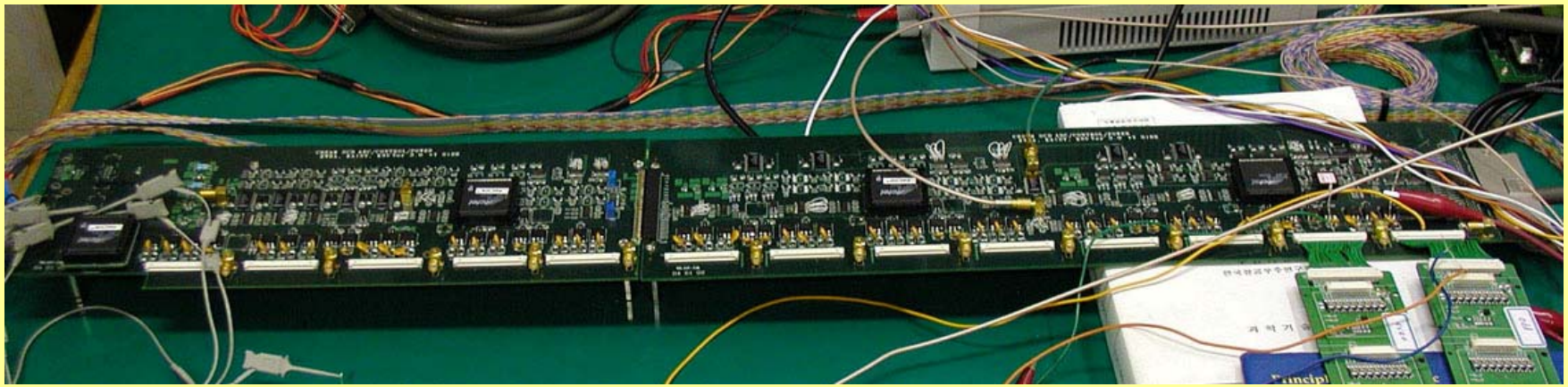


ADC: MAX 1133

- Sampling Speed : 200ksps

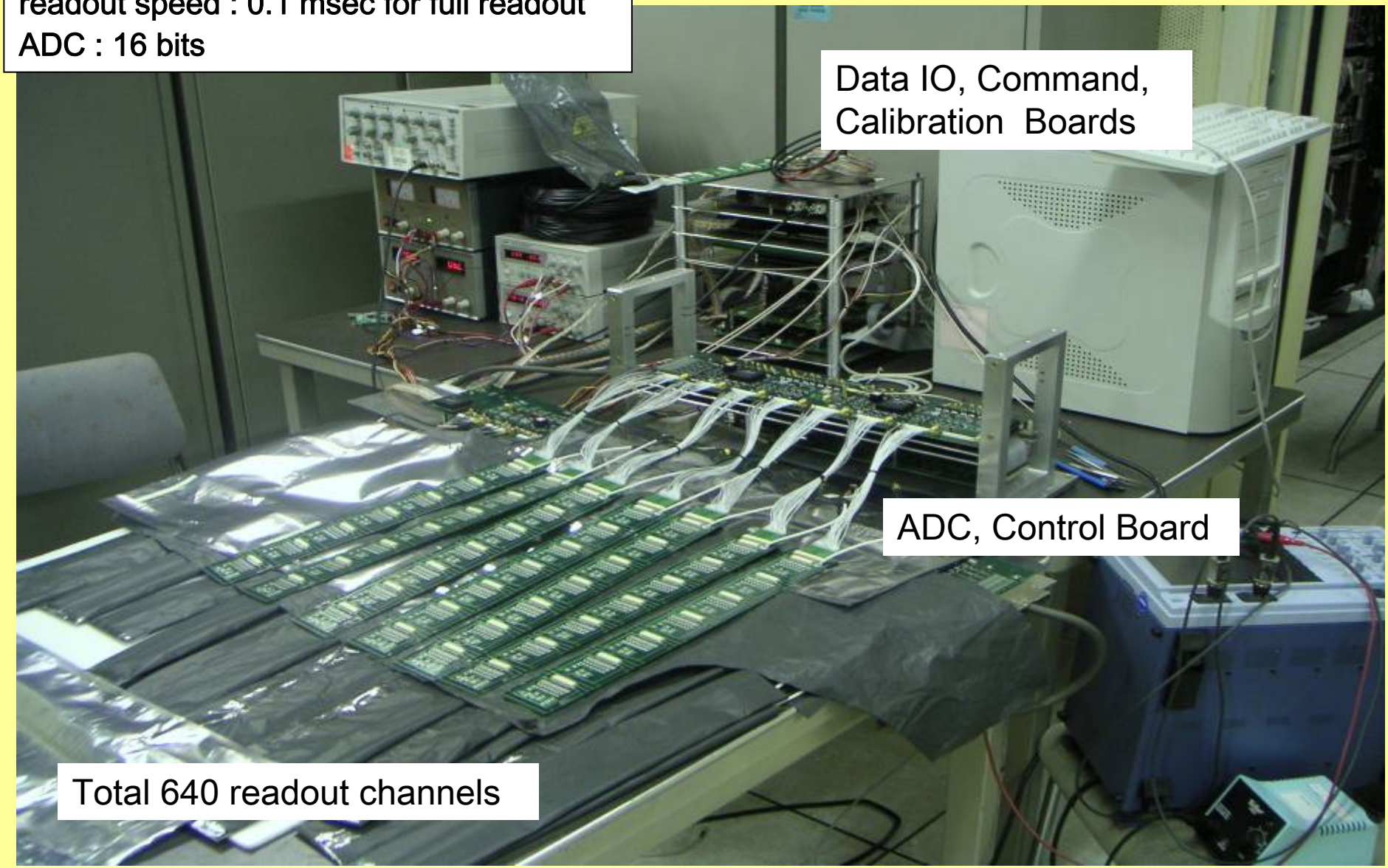
(200ksps X 16bit = 0.4Mbyte/s)

- Resolution : 16bit (65536 Level)



Integration Test of Electronics and DAQ

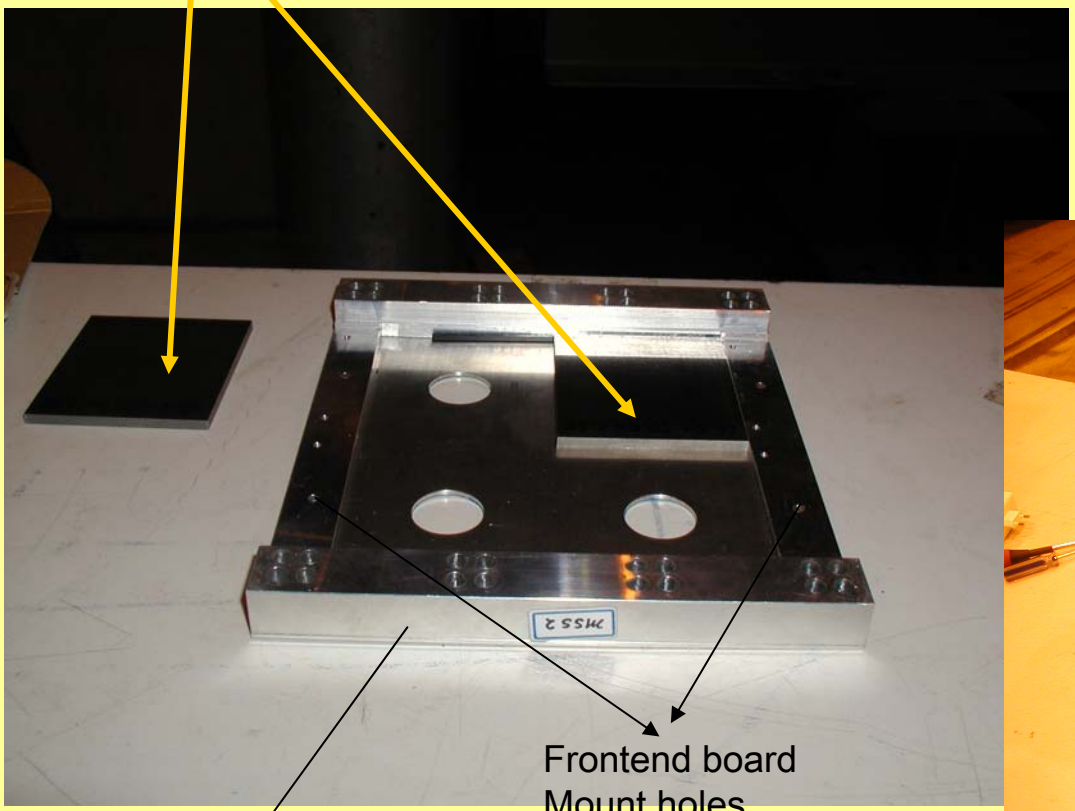
readout speed : 0.1 msec for full readout
ADC : 16 bits



Tungsten and Mechanics

Tungsten

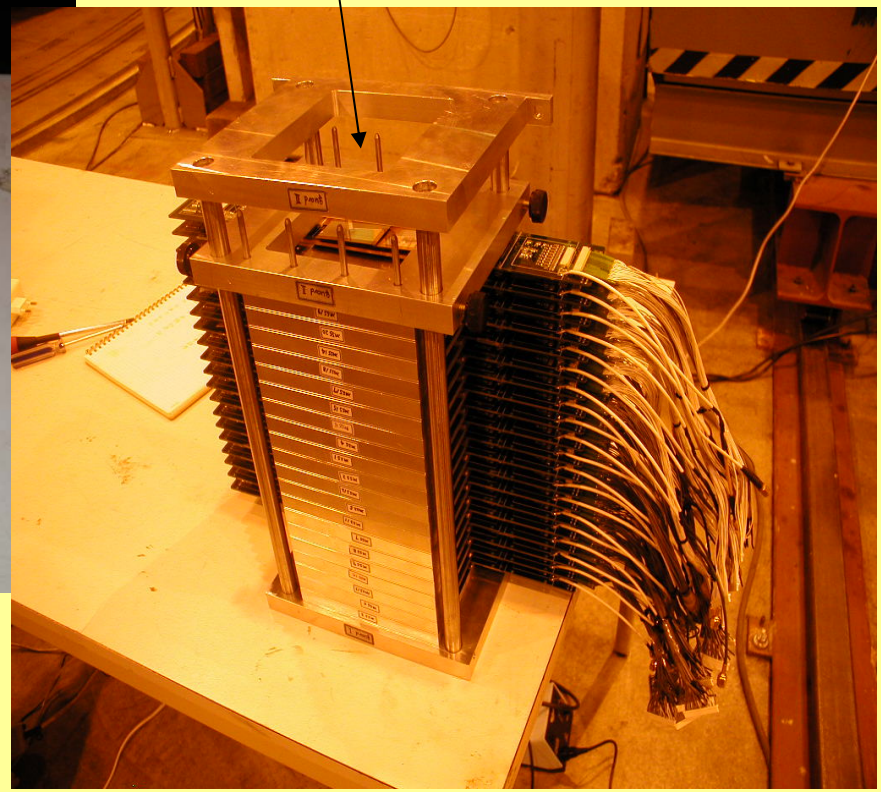
thickness : 3.5 mm (= 1 X0)
Size 65.5 mm X 57.5 mm (~ sensor size)



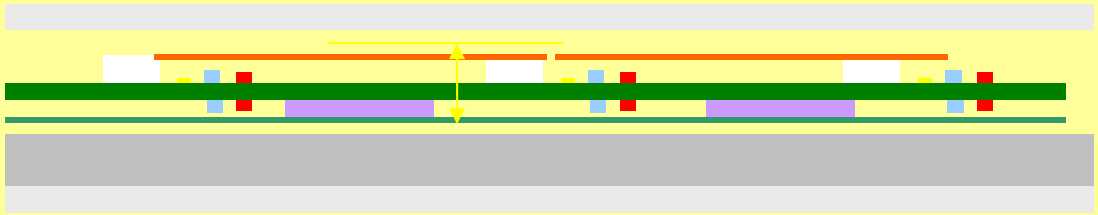
Frontend board
Mount holes

Aluminum Support of a Layer

Test Module : 20 layers stacked



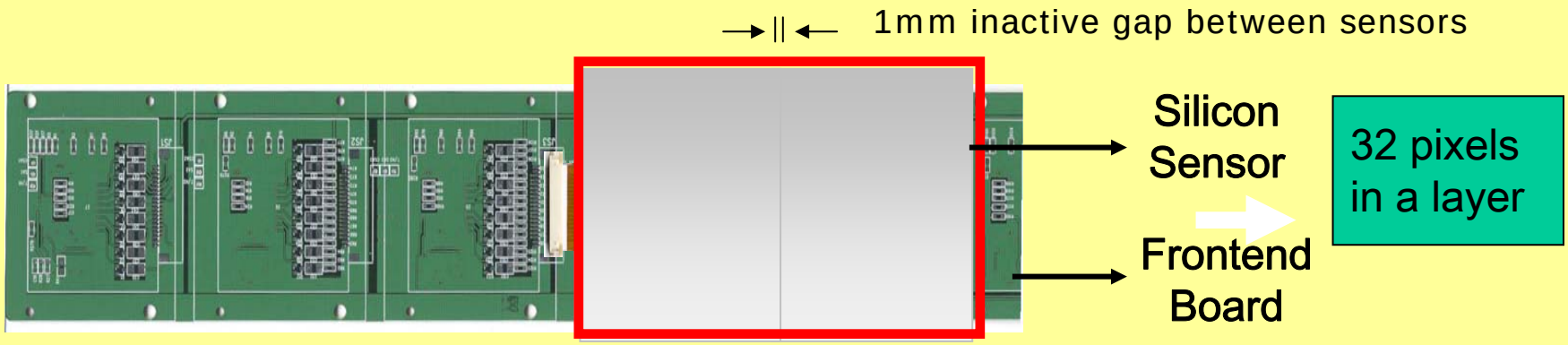
Thickness of an Assembled Layer

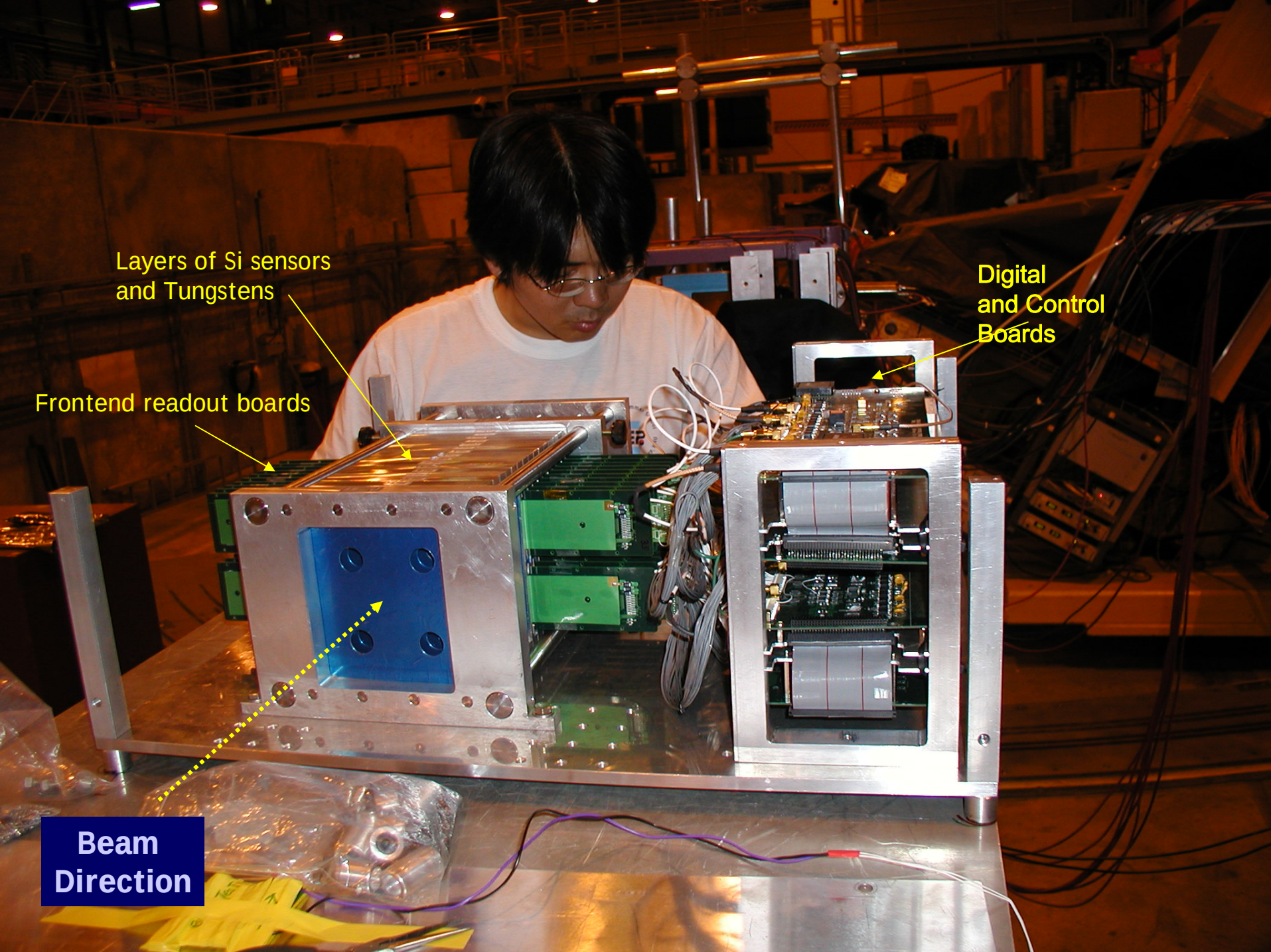


Connector	2.7 mm	Capacitor	1.4 mm
Pcb	1.7 mm	Resistor	0.65 mm
Diode	1.15 mm	*CR 1.4 chip*	*2.45 mm*
Shielding board	*1mm*		

Aluminum	1.5 mm
Sensor and Readout	10 mm
Tungsten	3.5 mm

→ 15 mm

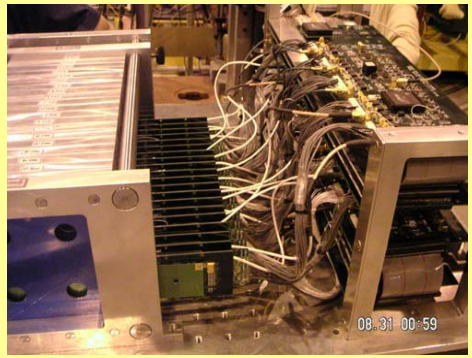



Layers of Si sensors
and Tungstens
Digital
and Control
Boards
Frontend readout boards
Beam
Direction

Summary of Our Test Module

Geometry

- Total 20 layers = 20X
  with uniform layer thickness
- Shower sampling at 19 layers
  with 2 sensors each layer.
- 1mm gap between sensors
- Aligned beam center to the center of a sensor

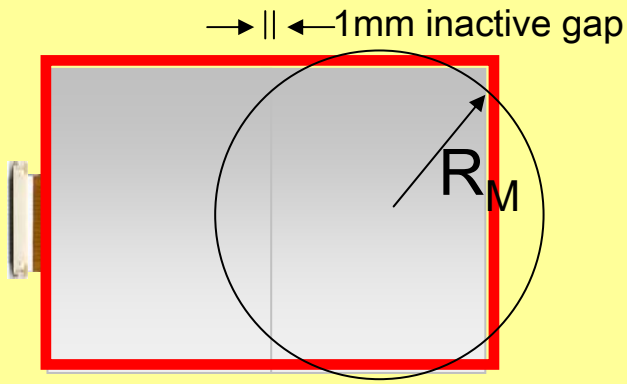


Effective R_M :~ 45mm

from volume ration of material

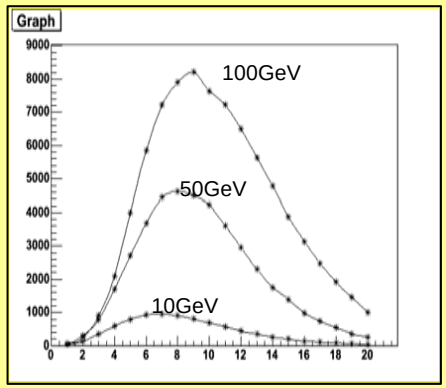
$$\rho_M = E_s \frac{X_0}{E_c} \qquad \frac{1}{X_0} = \sum_i \frac{V_i}{X_i}$$

-> insufficient transverse shower containment

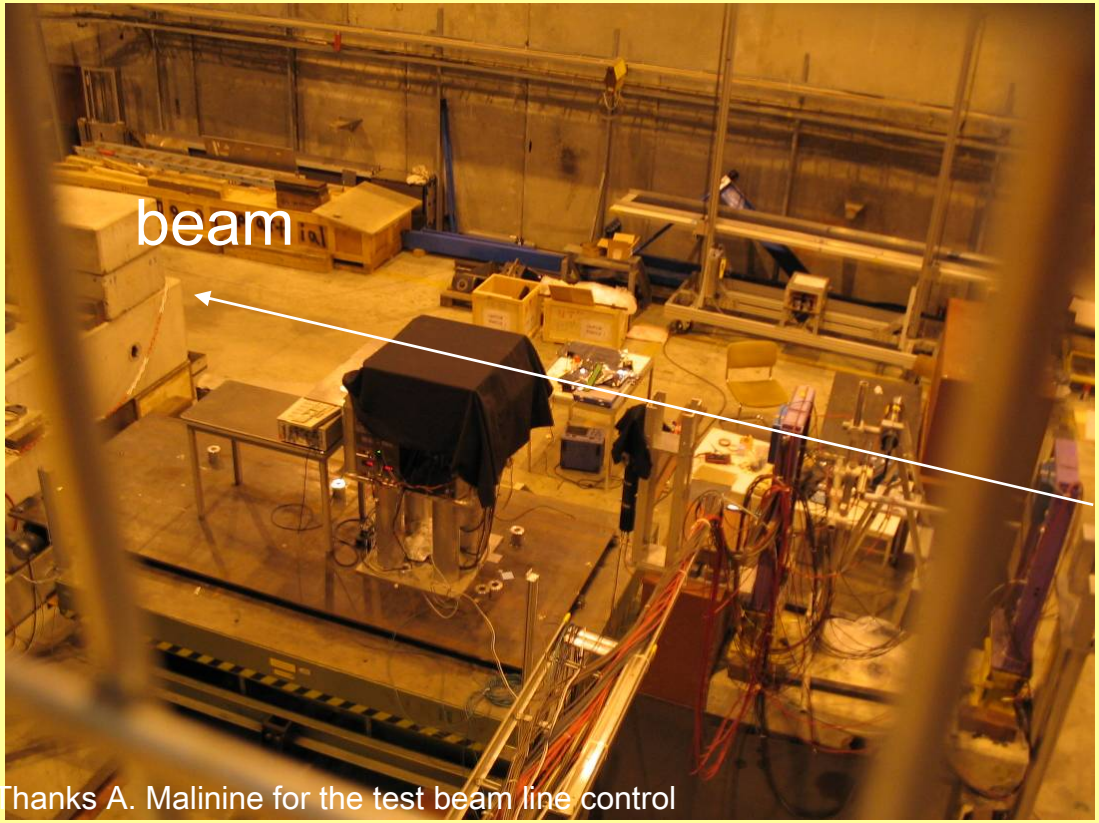


No action taken for
cooling the frontend.
Temperature level
during test ~35 to 40 deg

Geant4 Simulation →



CERN Beam Test



Thanks A. Malinine for the test beam line control

Beam Test : CERN SPS H2 beam line
for a week till Sep. 7 2004
Beam cycle 18.0 sec with 4.8 sec spill time
beam line focus & existing trigger scintillators
give beam spread of ~1 cm diameter
Beam focus worse in muon beam

Steps of Beam Test

1. Tune trigger time delay

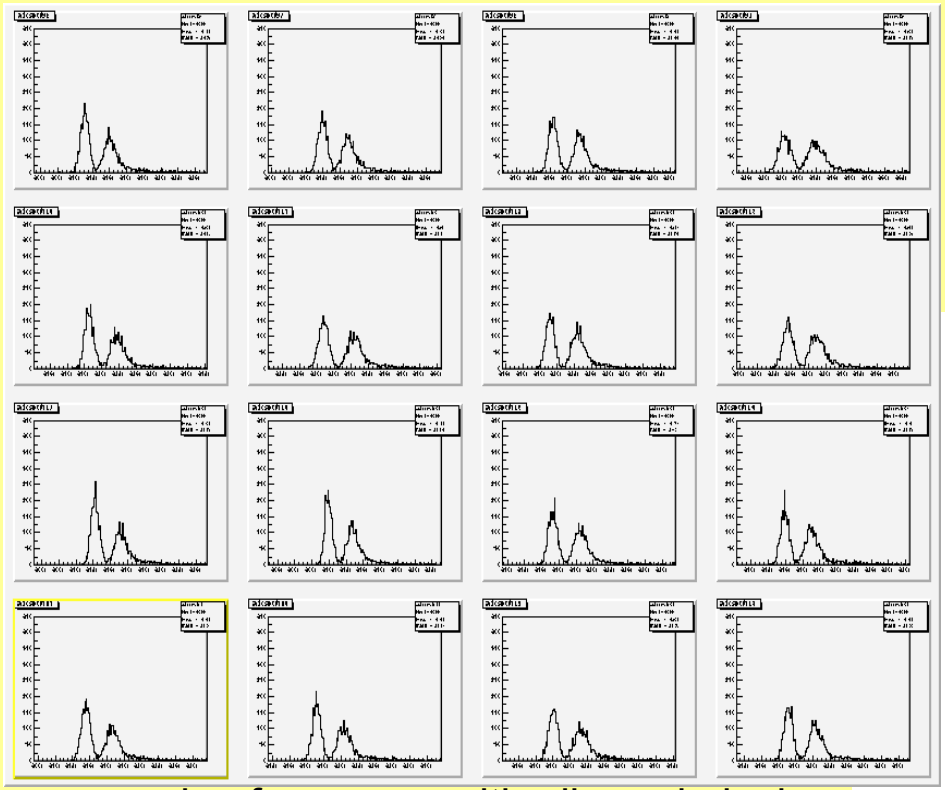
2. Align detector by using movable table
under the our detector

3. MIP calibration of all channels
(using hadron beam (less spread) after removing all tungstens)

4. Data Run
(electron
150,100,80,50,30,20,10 GeV
hadron 150 GeV
muon 150 GeV)

random trigger mixed in the runs for pedestal monitor

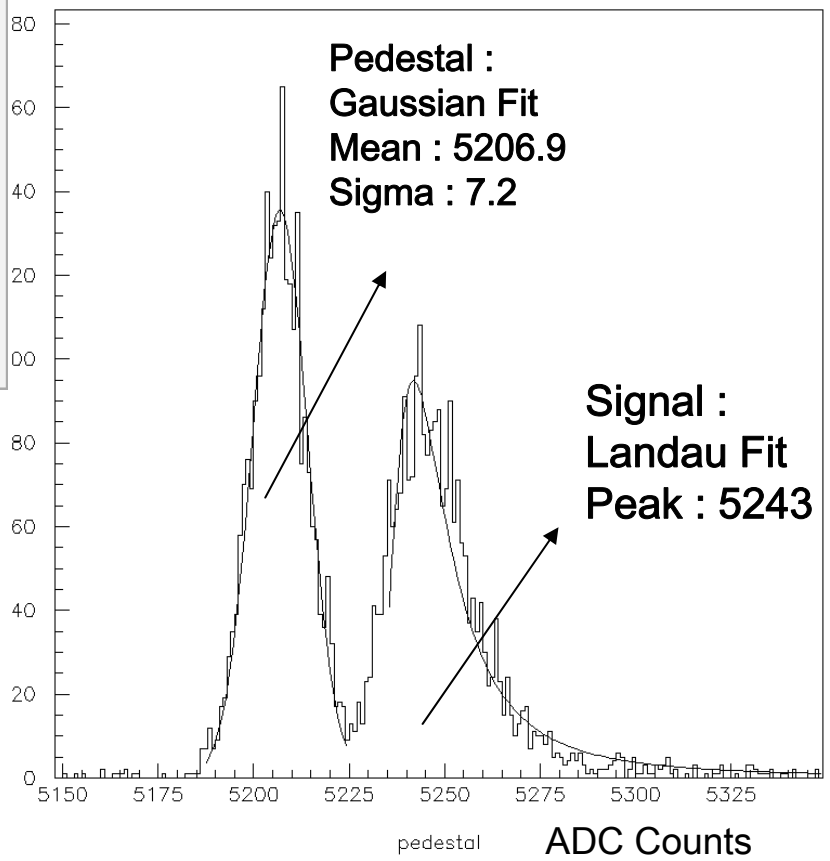
Channel Scan for MIP calibration



an example of a sensor with all good pixels

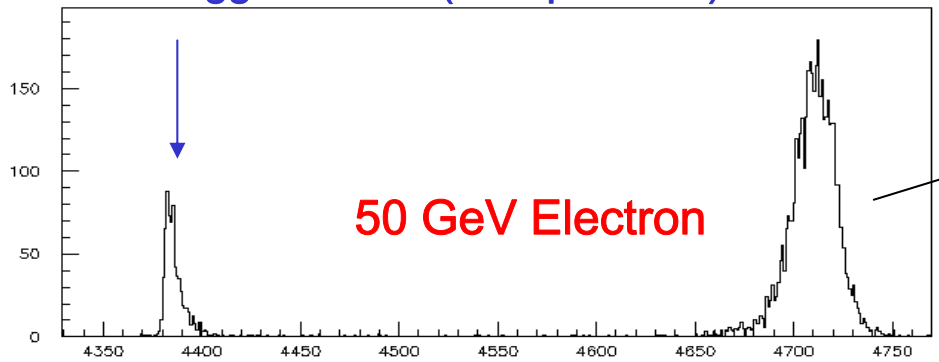
Scanned over all 640 channels
with 100 GeV hadron Beam
(no tungsten)

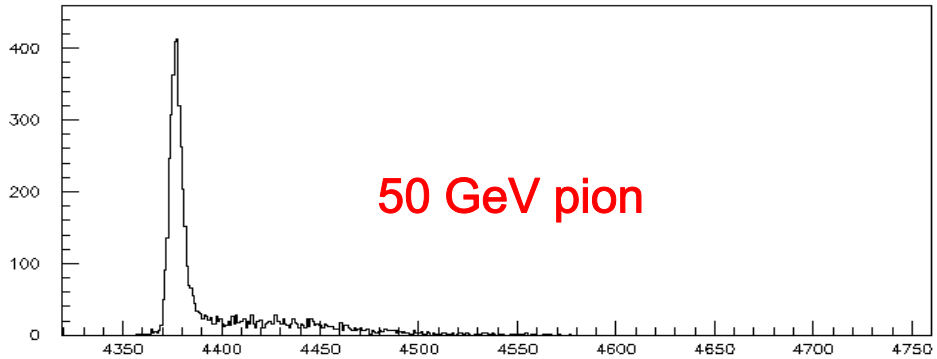
S/N = 5.2

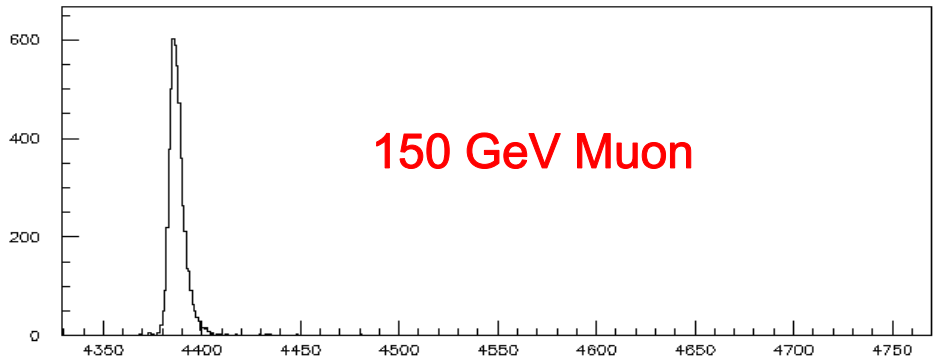


Detector Response to Different Particles

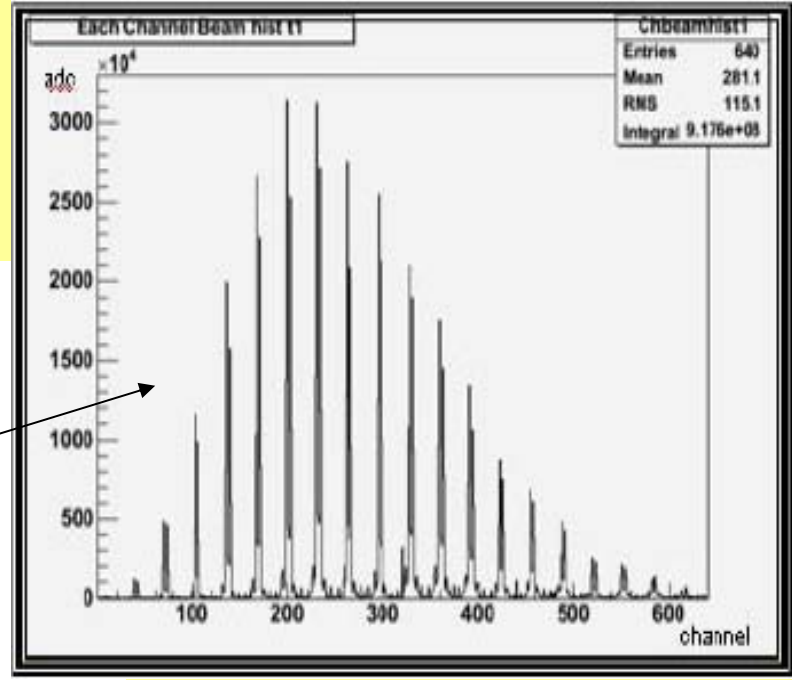
Random Trigger events (total pedestal)







Total ADC of an event / 640

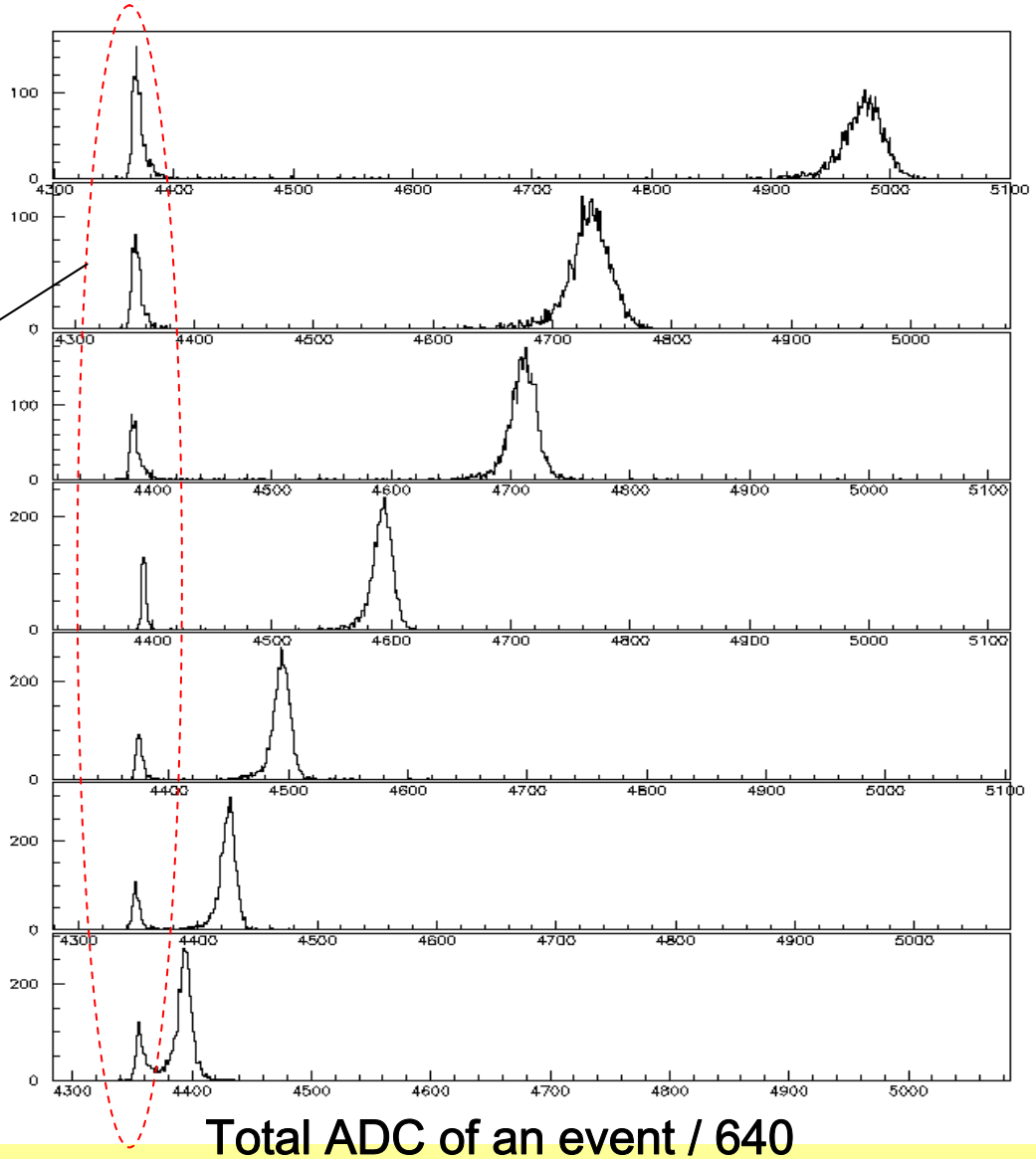


Online Shower Profile Monitor
Pedestal subtracted

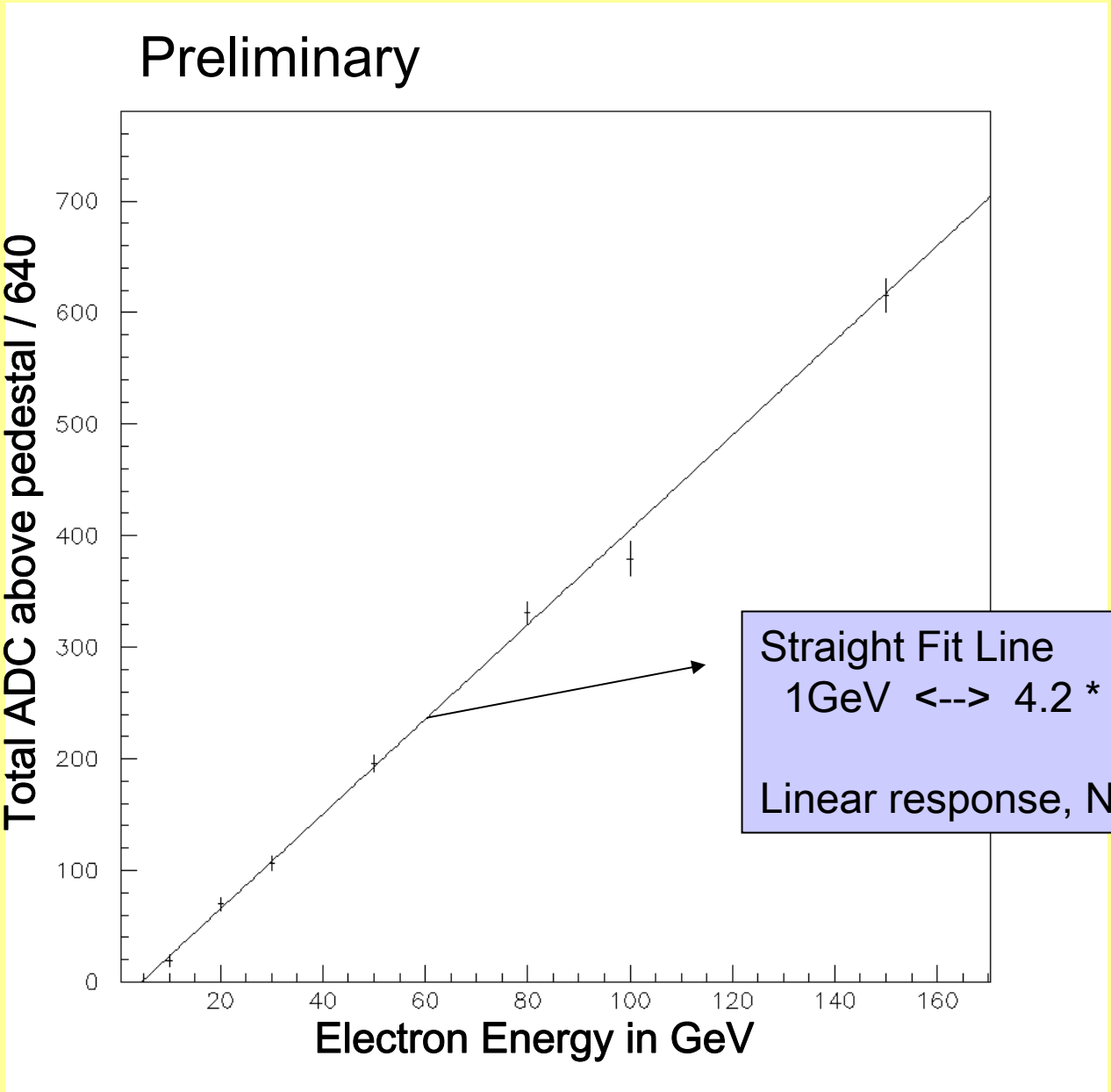
First Analysis :
sum ADC counts of all channels

No rejection of dead, noisy channels, No gain calibration applied

Detector Response to Different e^- Energy Shower



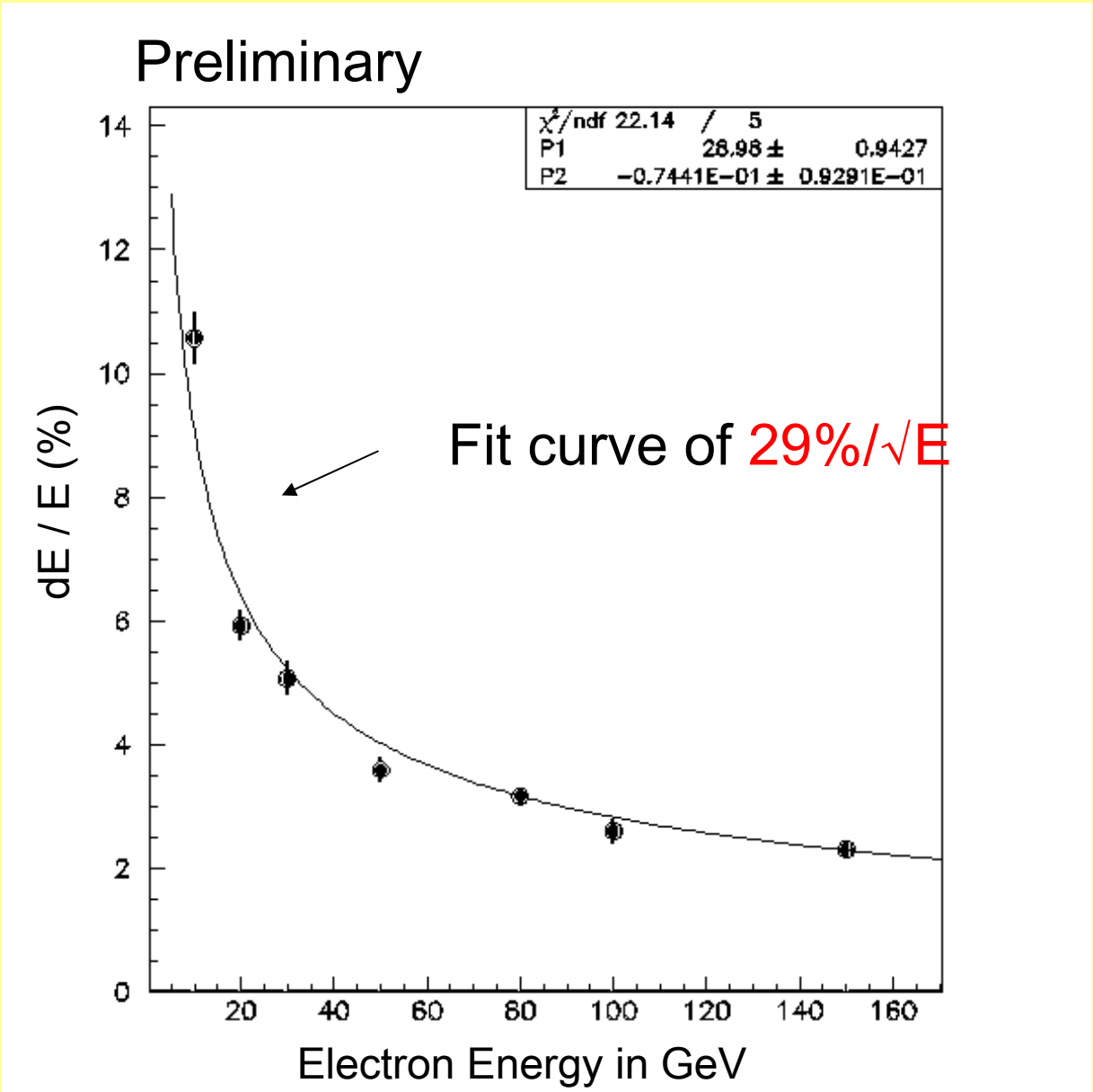
Calorimeter Calibration



Straight Fit Line
1GeV <--> 4.2 * 640 ADC Counts

Linear response, No saturation

Energy Resolution



- Geant4 simulation of this setup taking into account only shower leakage gives 18%/√E.
- The effect of bad channels, gain calibration, and beam spread are not included here.
- Working on further analysis

Summary and Remarks

- **We have an experience on successful design and production of Si Pixel sensors**
  - **shows the yield close to 90% and better than the expectation**
  - **excellent Si sensors, typically I_d =10nA/cm^2**
- **Si-W Test Module for LC was built and exposed to the CERN beams '2004**
  - **Preliminary result 28%/√E, (MC 18%/√E without taking into account of**
    - Noisy channels (~10%)
    - ADC unstable(~10%)
    - Deal channels (~2%)
    - Gain calibration
    - Beam spread
- **The cost of Silicon is down to \$5/cm^2, hope to down to less than \$2/cm^2**
- **Prototype-II design with thinner layers and AC-coupled sensors is in progress**