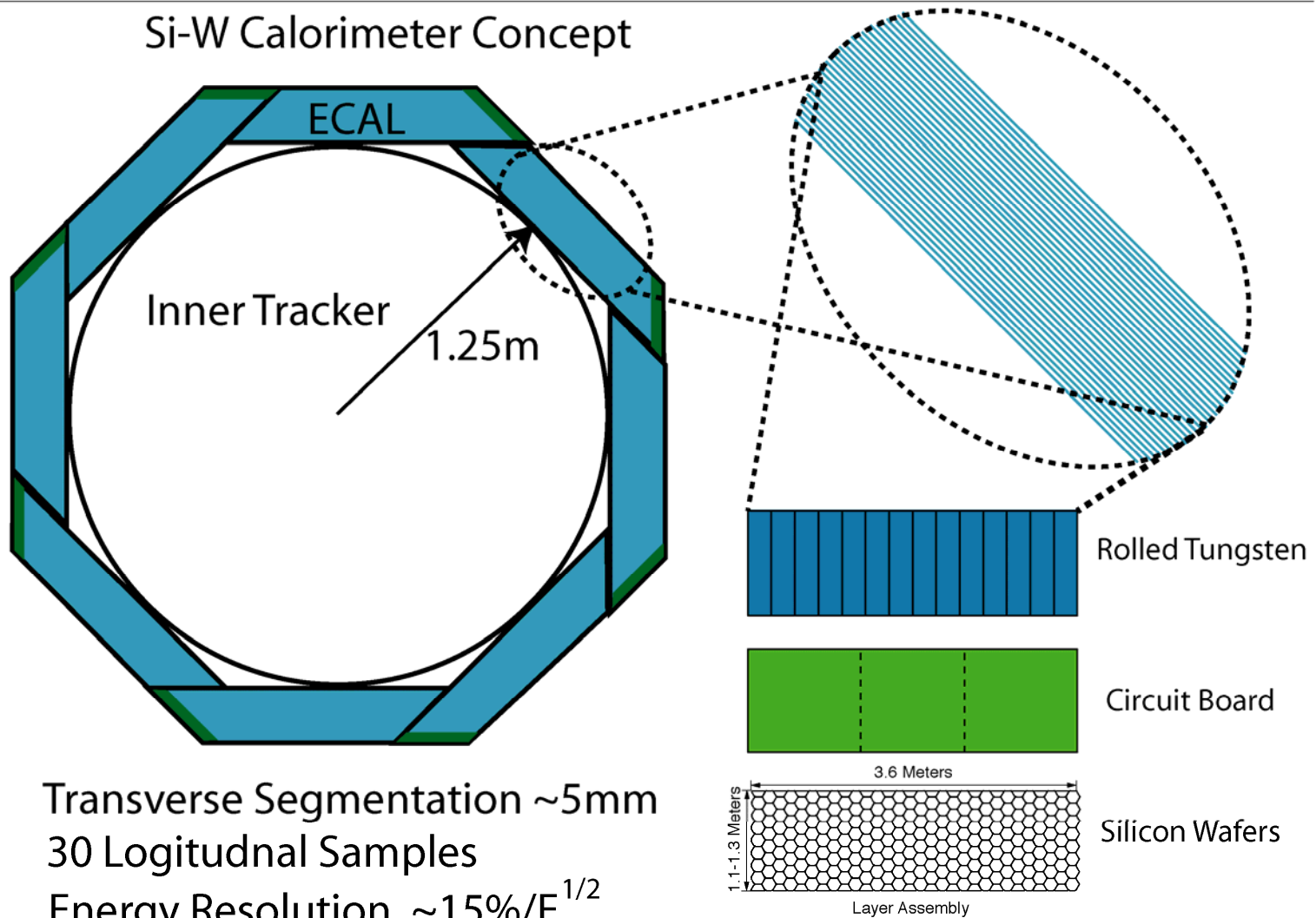# SiD Electronic Concepts

- **SLAC**
  - D. Freytag
  - G. Haller
  - J. Deng
  - mb
- **Oregon**
  - J. Brau
  - R. Frey
  - D. Strom
- **BNL**
  - V. Radeka

Overview

- SLAC/Oregon/BNL is developing a read out chip (ROC) for the Si-W calorimeter.
  - Highly integrated into structural design – bump bonded to detector
  - 1024 pixels / ROC ---Thus working name KPiX
  - Rough concept for "DAQ" strategy.
- Similar architecture with reduced dynamic range should work for Si strips. 2048 pixels / ROC
- Similar architecture should work for HCal and muon system.
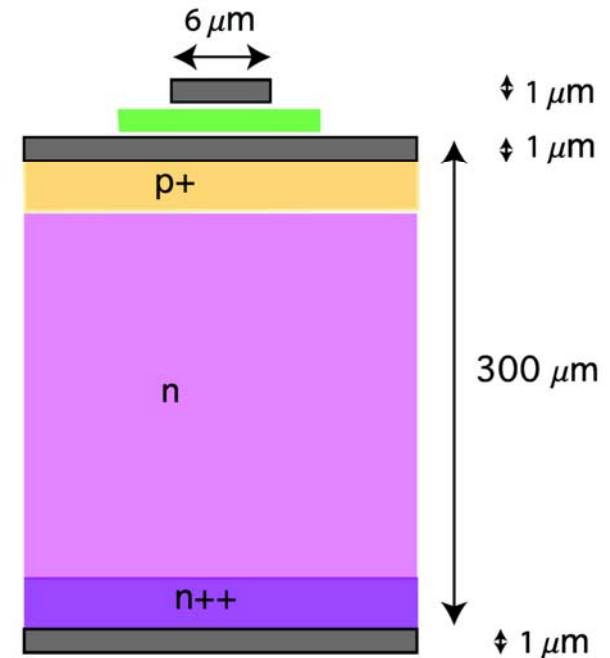- Will not work for very forward systems.
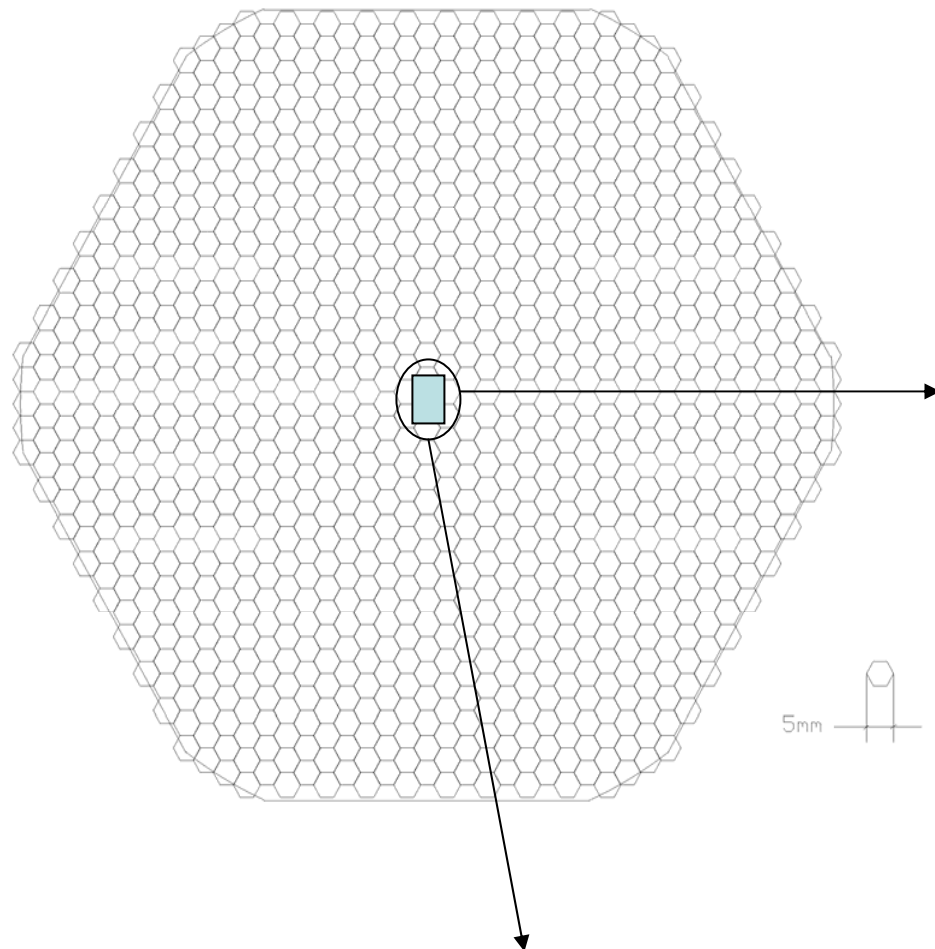
Concept

Si-W Calorimeter Concept

ECAL

Inner Tracker

1.25m

Transverse Segmentation ~5mm
30 Logitudnal Samples
Energy Resolution ~15%/$E^{1/2}$

Rolled Tungsten

Circuit Board

3.6 Meters

1.1-1.3 Meters

Silicon Wafers

Layer Assembly

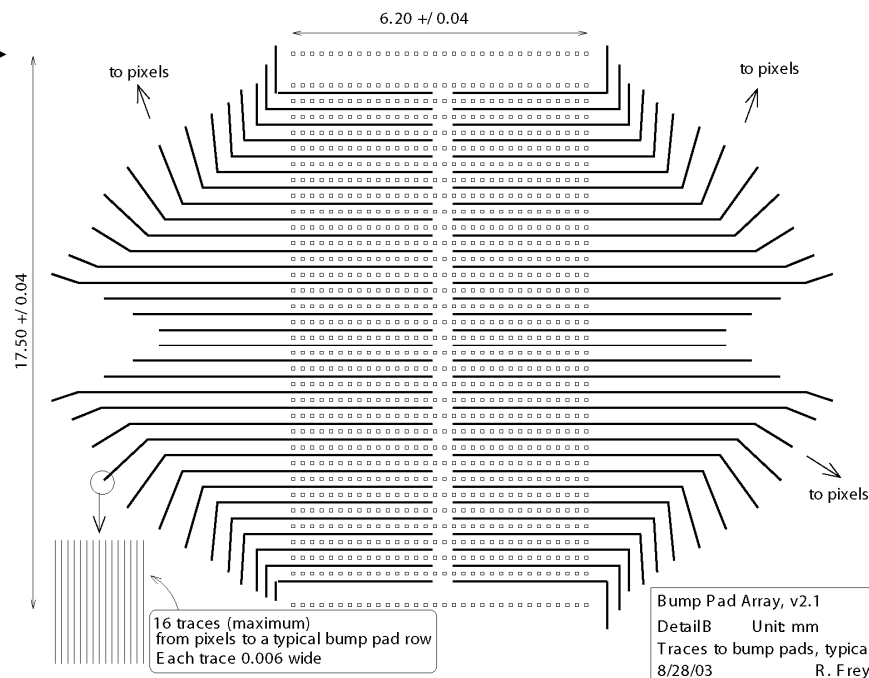# Electronics requirements

- **Signals**
    - <2000 e noise
    - Require MIPs with S/N > 7
    - Max. signal 2500 MIPs (5mm pixels)
- **Capacitance**
    - Pixels: 5.7 pF
    - Traces: ~0.8 pF per pixel crossing
    - Crosstalk: 0.8 pF/Gain x C_{in} < 1%
- **Resistance**
    - 300 ohm max
- **Power**
    - < 40 mW/wafer $\Rightarrow$ power cycling
        (An important LC feature!)
- Provide fully digitized outputs of charge and time on one ASIC for every wafer.

Wafer and readout chip

6.20 +/ 0.04

17.50 +/ 0.04

to pixels

to pixels

to pixels

5mm

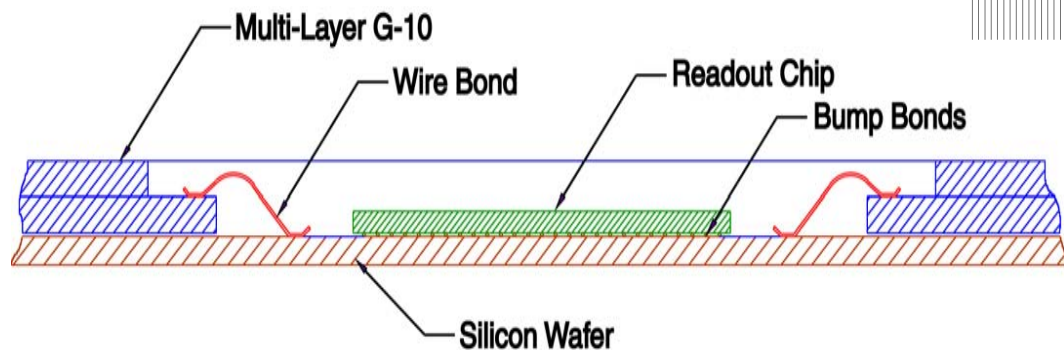16 traces (maximum)
from pixels to a typical bump pad row
Each trace 0.006 wide

Bump Pad Array, v2.1
DetailB   Unit: mm
Traces to bump pads, typical
8/28/03   R. Frey

Multi-Layer G-10

Wire Bond

Readout Chip

Bump Bonds

Silicon Wafer

ch
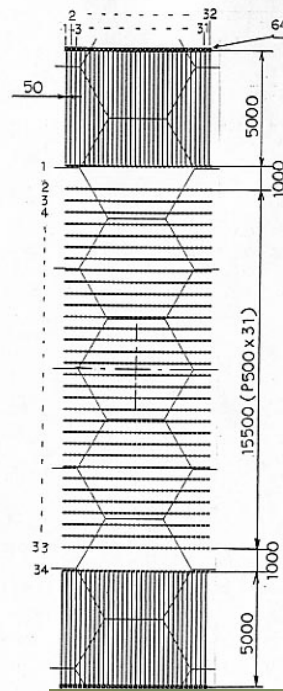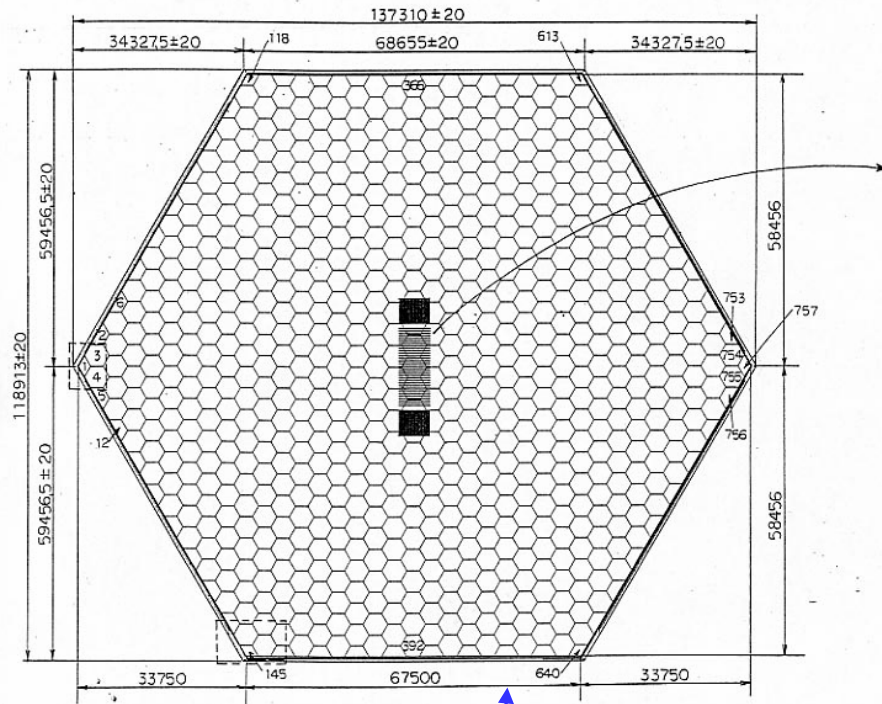
Detector Layout

Real Thing
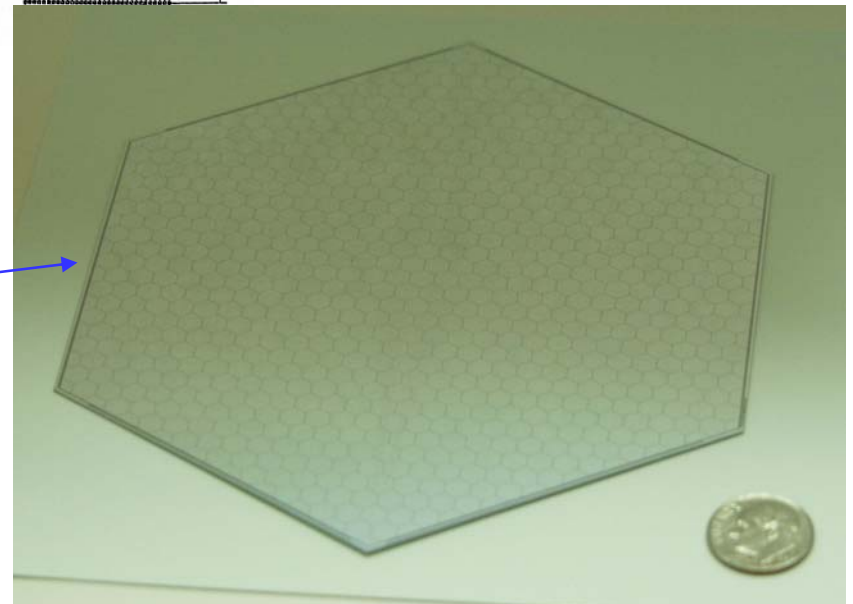
	Document #	Date Effective
		12/15/2004
	Prepared by(s)	Supersedes
	Breidenbach/Freytag/Haller/Milgrome	None
Project Name	Subsystem/Office	
Document Title		
Conceptual Design of W-SI Front-End ASIC		

Version 1.3

There is an 18 page technical document, now in its 4th major revision for register assignments, etc for the cold bunch structure.

Si-W Pixel Analog Section

1 of 1024 pixels

Low Gain

Reset

High Gain (default)

Range Logic → Range Register

Reset

Range Threshold

Wilkinson scaler and logic

Latch (4x)

Source

Track

Analog 1

Analog 4

Leakage Current Servo

Event Threshold

Bunch Clock

Control Logic
Pulses to Timing Latch, Range Latch, and Event Counter

Reset

Track

Cal Dac

Cal Strobe

Simplified Timing:

There are ~ 3000 bunches separated by ~300 ns in a train, and trains are separated by ~200 ms.

Say a signal above event threshold happens at bunch n and time T0.
The Event discriminator triggers in ~100 ns and removes resets and strobes the Timing Latch (12 bit), range latch (1 bit) and Event Counter (5 bits).
The Range discriminator triggers in ~100 ns if the signal exceeds the Range Threshold.
When the glitch from the Range switch has had time to settle, Track connects the sample capacitor to the amplifier output. (~150 ns)
The Track signal opens the switch isolating the sample capacitor at T0 + 1 micro s. At this time, the amplitude of the signal at T0 is held on the Sample Capacitor .
Reset is asserted (synched to the bunch clock) . Note that the second capacitor is reset at startup and following an event, while the high gain (small) capacitor is reset each bunch crossing (except while processing an event)
The system is ready for another signal in ~1.2 microsec.
After the bunch train, the capacitor charge is measured by a Wilkinson converter.

Si-W Pixel Analog Section

1 of 1024 pixels

Low Gain

Reset

Range Logic → Range Register

Reset

High Gain (default)

Range Threshold

Wilkinson scaler and logic

Latch (4x)

Source

Track

Analog 1

Analog 4

Leakage Current Servo

Event Threshold

Control Logic
Pulses to Timing Latch, Range Latch, and Event Counter

Reset

Track

Bunch Clock →

Cal Dac

Cal Strobe

**Cal strobe gated by 1024 long SR.
Pixel pattern arbitrary.**

Simplified Timing:

There are ~ 3000 bunches separated by ~300 ns in a train, and trains are separated by ~200 ms.

Say a signal above event threshold happens at bunch n and time T0.
The Event discriminator triggers in ~100 ns and removes resets and strobes the Timing Latch (12 bit), range latch (1 bit) and Event Counter (5 bits).
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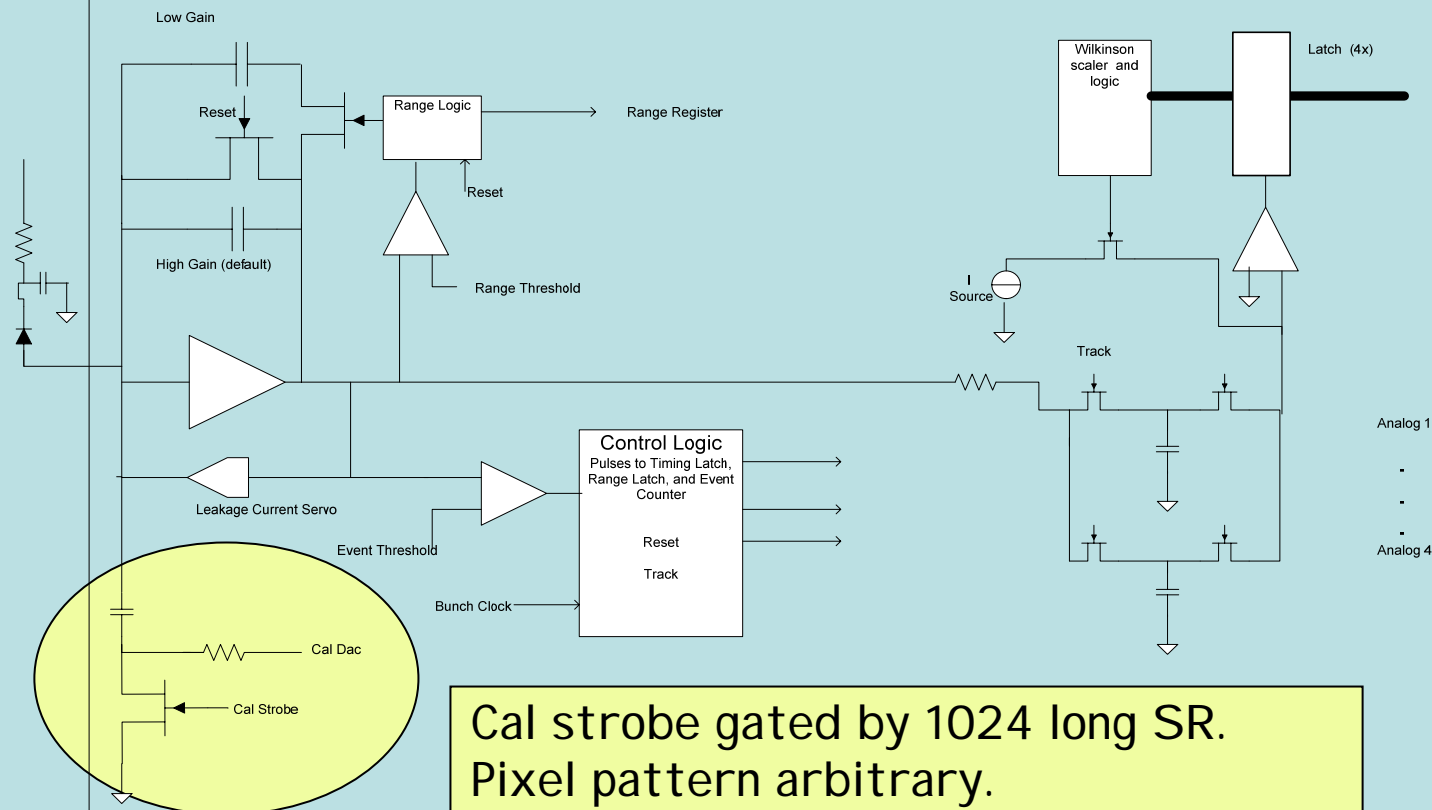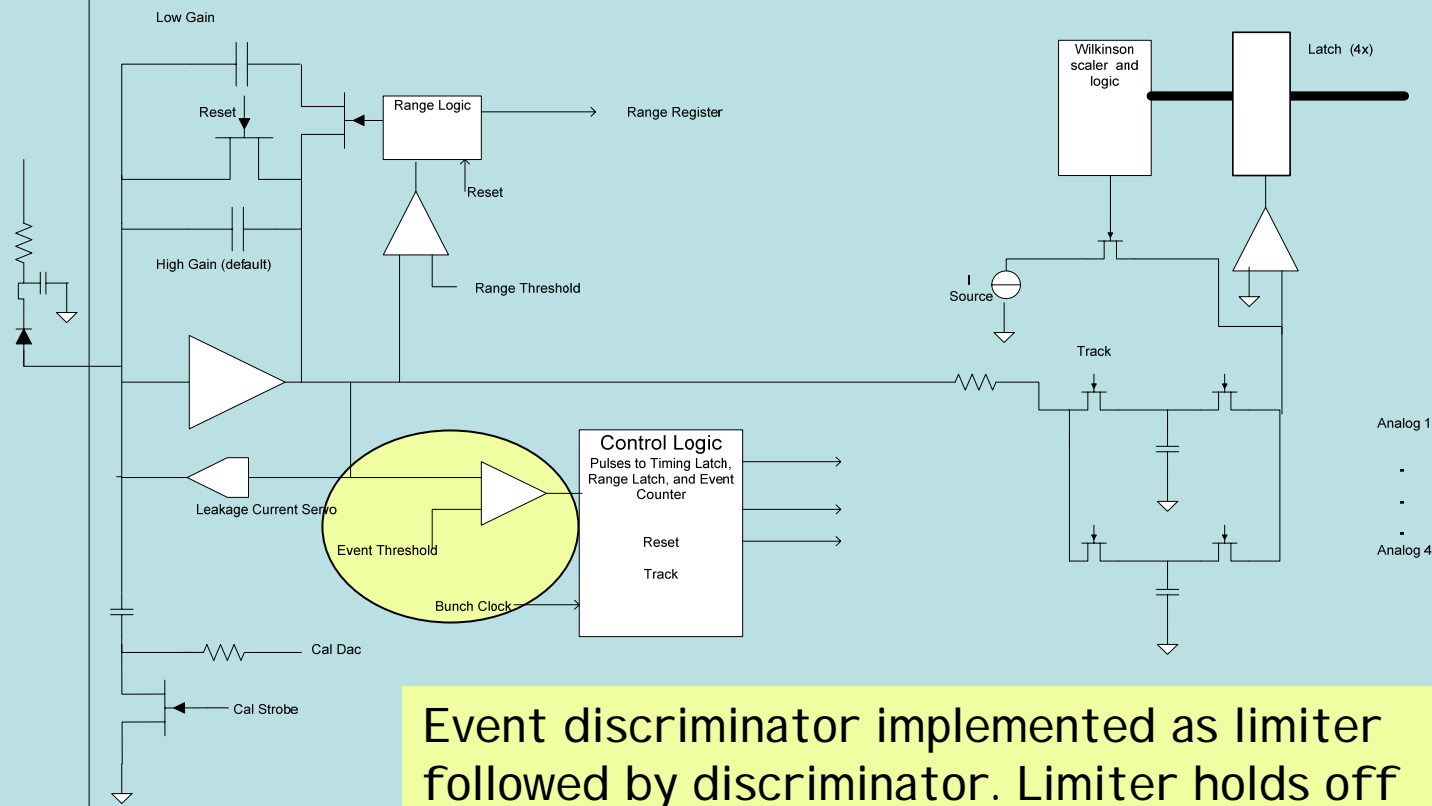Reset is asserted (synched to the bunch clock) . Note that the second capacitor is reset at startup and following an event, while the high gain (small) capacitor is reset each bunch crossing (except while processing an event)
The system is ready for another signal in ~1.2 microsec.
After the bunch train, the capacitor charge is measured by a Wilkinson converter.

1 of 1024 pixels

Low Gain

Wilkinson scaler and logic

Latch (4x)

Reset

Range Logic → Range Register

Reset

High Gain (default)

Range Threshold

Source

Track

Control Logic
Pulses to Timing Latch,
Range Latch, and Event
Counter

Reset

Track

Leakage Current Servo

Event Threshold

Bunch Clock

Analog 1

.
.
.
Analog 4

Cal Dac

Cal Strobe

Simplified Timing:

There are ~ 3000 bunches separated

Say a signal above event threshold h
The Event discriminator triggers in ~
The Range discriminator triggers in ~
When the glitch from the Range swit
The Track signal opens the switch is
Reset is asserted (synched to the bu
while processing an event)
The system is ready for another signal in ~1.2 microsec.
After the bunch train, the capacitor charge is measured by a Wilkinson converter.

Event discriminator implemented as limiter followed by discriminator. Limiter holds off resets, permitting longer integration time for discriminator and data hold. Discriminator threshold selected from either of two ROC wide DAC's.
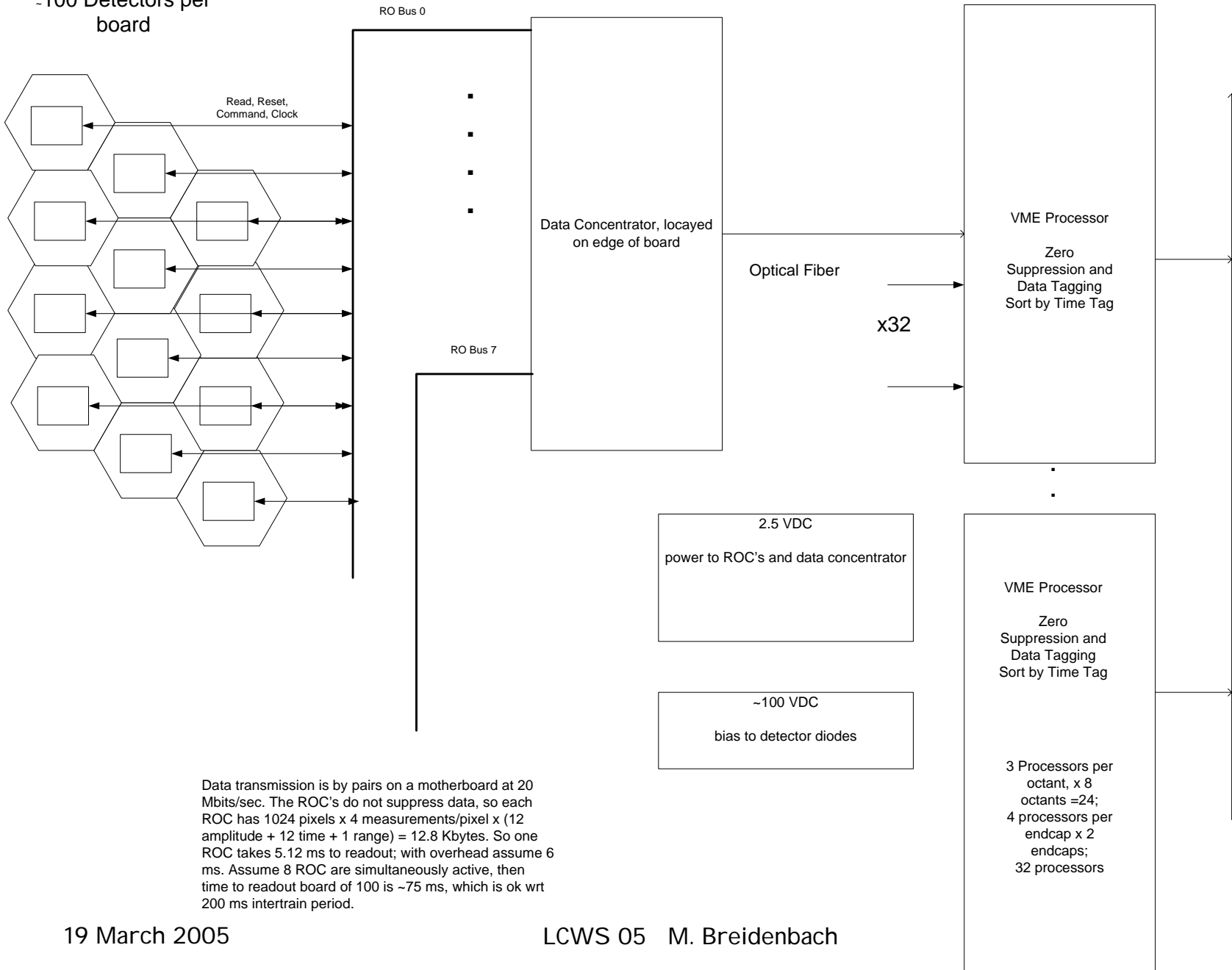
Pulse "Shaping"

- Take full advantage of synchronous bunch structure:
  - Reset (clamp) feedback cap before bunch arrival. This is equivalent to double correlated sampling, except that the "before" measurement is forced to zero. This takes out low frequency noise and any integrated excursions of the amplifier.
  - Integration time constant will be 0.5 – 1 μsec. Sample *synchronously* at 2 – 3 integration time constants.
  - Time from reset 1 – 3 μsec, which is equivalent to a 1 – 3 μsec differentiation.

- Noise: ~1000 e$^-$ for ~ 20 pF. (100 μA through input FET).

Power

| Phase | Current (ma) | Instantaneous Power (mw) | Cold Train/Bunch Structure | | | Average Power (mw) | Comments |
			Time begin (us)	Time End (us)	Duty Factor		
All Analog "on"	370.00	930.00	0.00	1,020.00	5.10E-03	4.7	Power ok with current through FET's
Hold "on", charge amp off	85.00	210.00	1,021.00	1,220.00	9.95E-04	0.2	
Analog power down	4.00	10.00	1,020.00	200,000.00	9.95E-01	9.9	
LVDS Receiver, etc		3.00	0.00	200,000.00	1.00E+00	3.0	Receiver always on.
Decode/Program		10.00	1.00	100.00	4.95E-04	0.0	Sequencing is vague!
ADC		100.00	1,021.00	1,220.00	9.95E-04	0.1	
Readout		50.00	1,220.00	3,220.00	1.00E-02	0.5	
Total						18.5	Total power OK

~100 Detectors per board

RO Bus 0

Read, Reset, Command, Clock

Data Concentrator, locayed on edge of board

RO Bus 7

Optical Fiber

x32

VME Processor

Zero Suppression and Data Tagging Sort by Time Tag

2.5 VDC

power to ROC's and data concentrator

VME Processor

Zero Suppression and Data Tagging Sort by Time Tag

~100 VDC

bias to detector diodes

3 Processors per octant, x 8 octants =24; 4 processors per endcap x 2 endcaps; 32 processors

Data transmission is by pairs on a motherboard at 20 Mbits/sec. The ROC's do not suppress data, so each ROC has 1024 pixels x 4 measurements/pixel x (12 amplitude + 12 time + 1 range) = 12.8 Kbytes. So one ROC takes 5.12 ms to readout; with overhead assume 6 ms. Assume 8 ROC are simultaneously active, then time to readout board of 100 is ~75 ms, which is ok wrt 200 ms intertrain period.
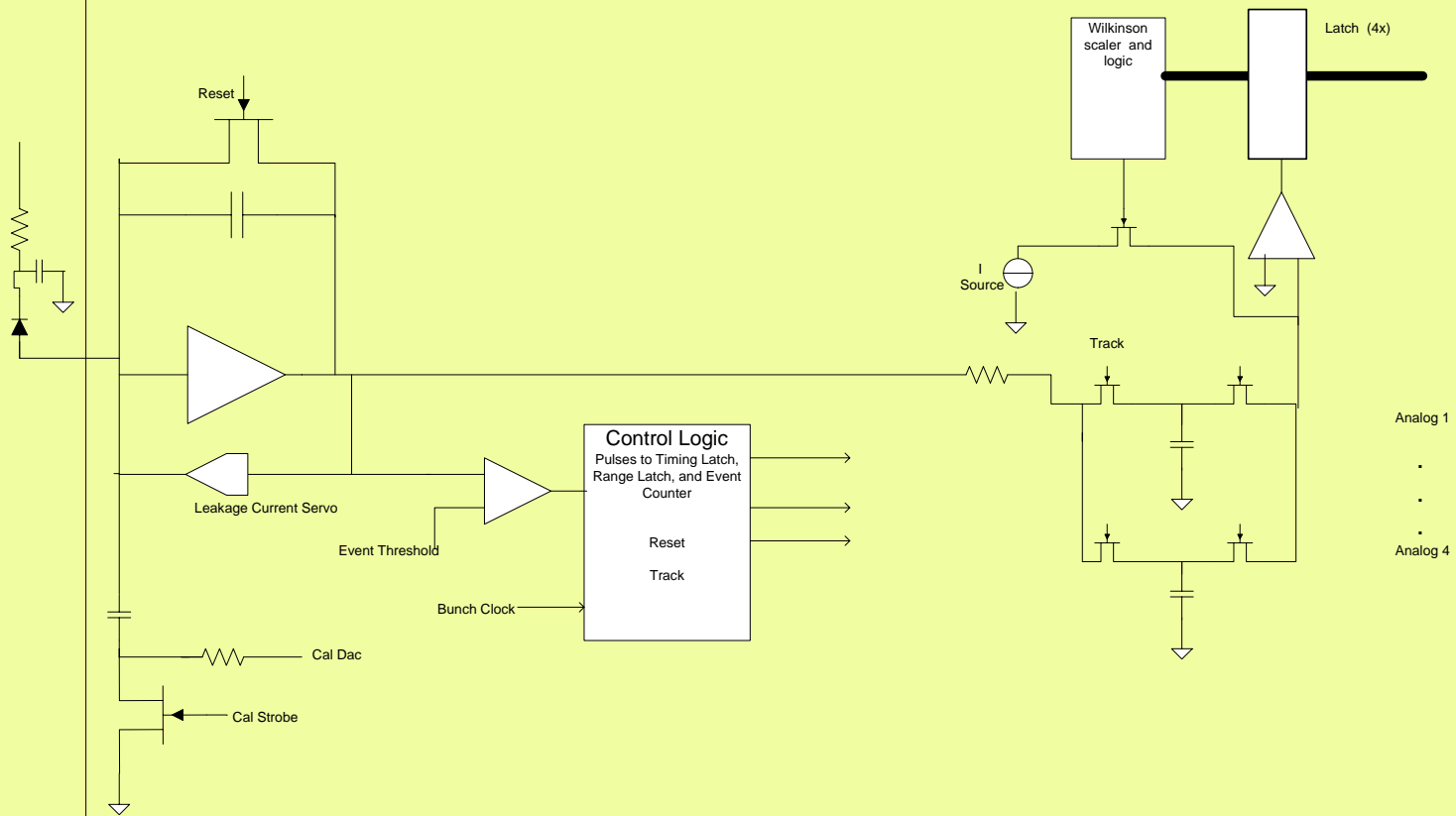
Tracker Pixel Analog Section

1 of 2048 pixels

Simplified Timing:

There are ~ 3000 bunches separated by ~300 ns in a train, and trains are separated by ~200 ms.

Say a signal above event threshold happens at bunch n and time T0.
The Event discriminator triggers in ~100 ns and removes resets and strobes the Timing Latch (12 bit) and Event Counter (5 bits).
Track connects the sample capacitor to the amplifier output. (~150 ns)
The Track signal opens the switch isolating the sample capacitor at T0 + 1 micro s. At this time, the amplitude of the signal at T0 is held on the Sample Capacitor .
Reset is asserted (synched to the bunch clock)
The system is ready for another signal in ~1.2 microsec.
After the bunch train, the capacitor charge is measured by a Wilkinson converter.
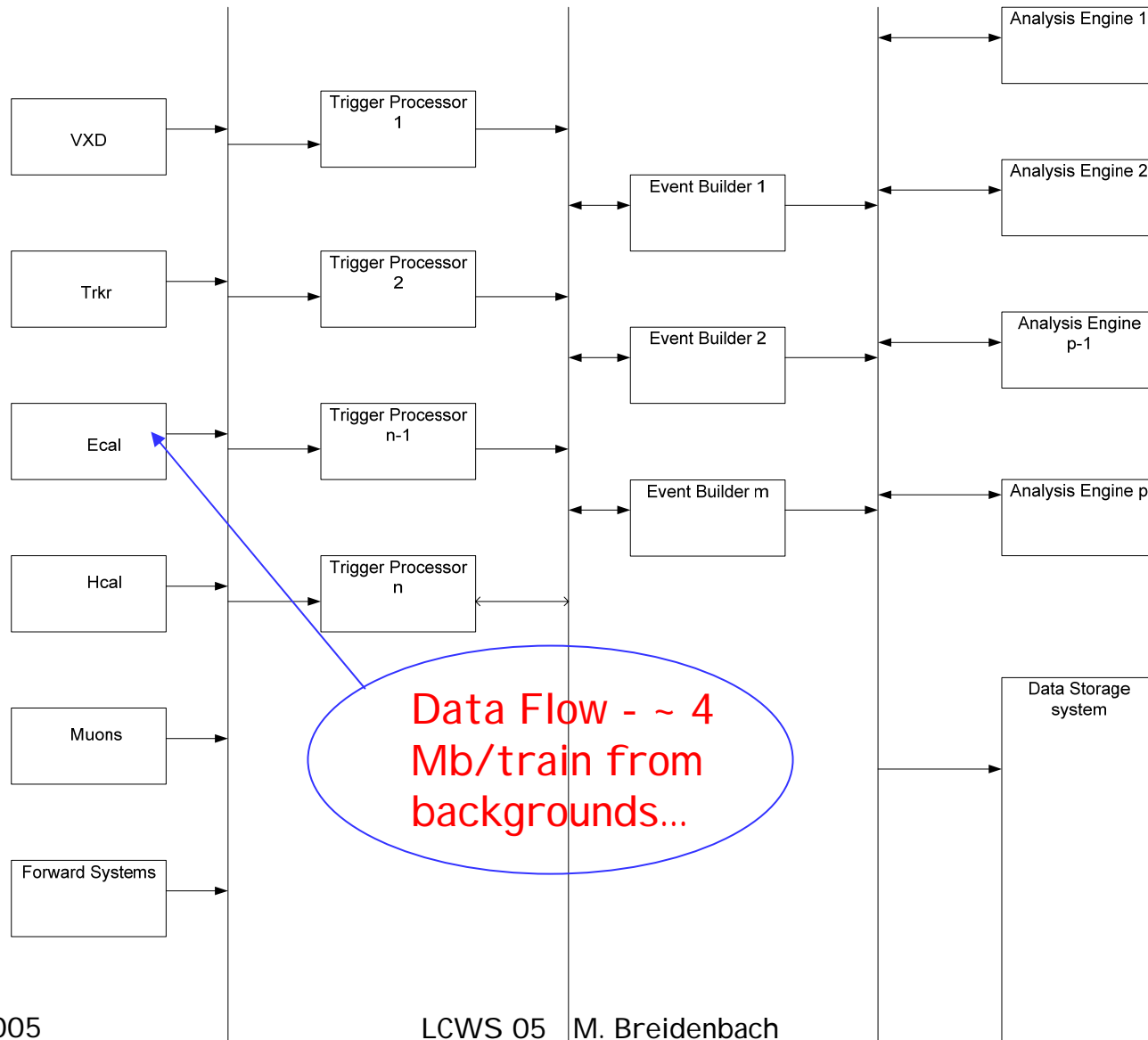
Comments

- The basic architecture should work with all the low occupancy sub-systems.
  - Including Tracker, EmCal, HCal, and muon system.
  - It does not address VXD issues – presumably CMOS to be developed – or the completely occupied Very Forward Calorimeters.
  - A variant might work in the forward regions of the tracker and calorimeters.
- The architecture is insensitive to the bunch separation within a train.
- The cost of a mask set is high, so development will be with (probably) 8 x 8 subsets instead of the 32 x 32 array.
- The unit cost of a large number of chips seems fine - <~ $40.
- Substantial design and simulation is done on EMCal Readout chip. Layout is progressing.
- ~No work done on anything else.