Progress towards a Long Shaping-Time Readout for Silicon Strips

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SLAC LCWS05
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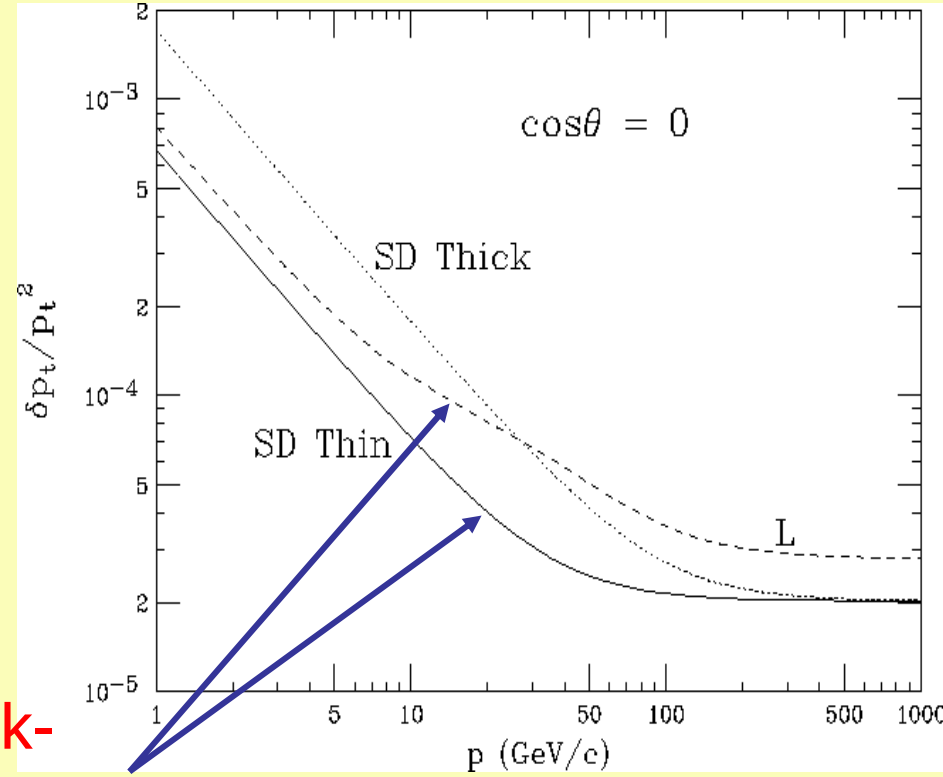
The Gossamer Tracker

Ideas:

- Long ladders ➔ substantially limit electronics readout and associated support
- Thin inner detector layers
- Exploit duty cycle ➔ eliminate need for active cooling



➔ Competitive with gaseous tracking over full range of momenta

Also: forward region...

Idea: Noise vs. Shaping Time

Agilent 0.5 μm CMOS process (qualified by GLAST)

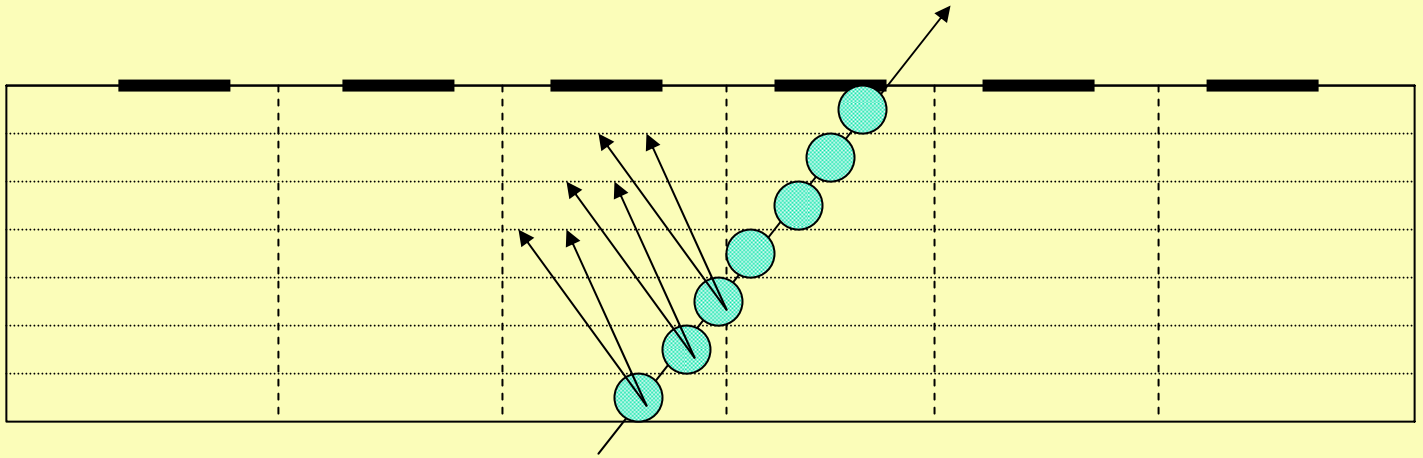
Min-i for 300μm Si is about 24,000 electrons

Shaping (μs)	Length (cm)	Noise (e^-)
1	100	2200
1	200	3950
3	100	1250
3	200	2200
10	100	1000
10	200	1850

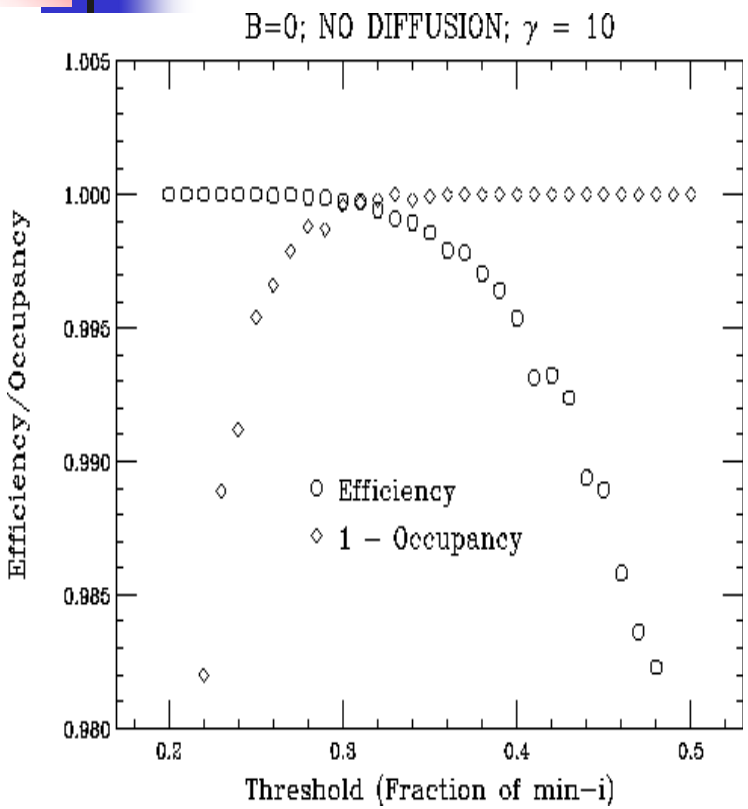
Pulse Development Simulation

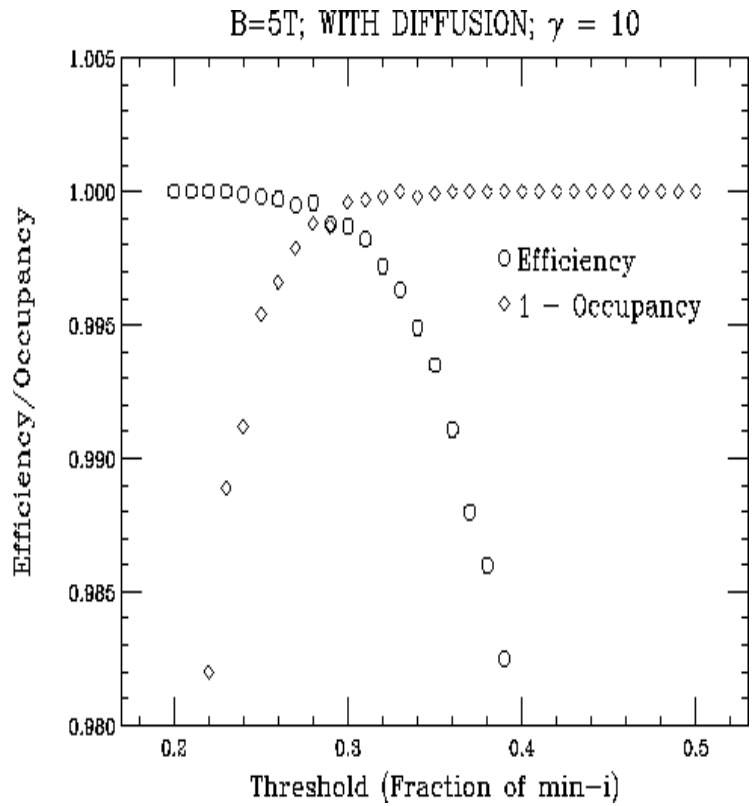
Long Shaping-Time Limit: strip sees signal if and only if hole is collected onto strip (no electrostatic coupling to neighboring strips)

Incorporates: Landau statistics (SSSimSide; Gerry Lynch LBNL), detector geometry and orientation, diffusion and space-charge, Lorentz angle, electronic response



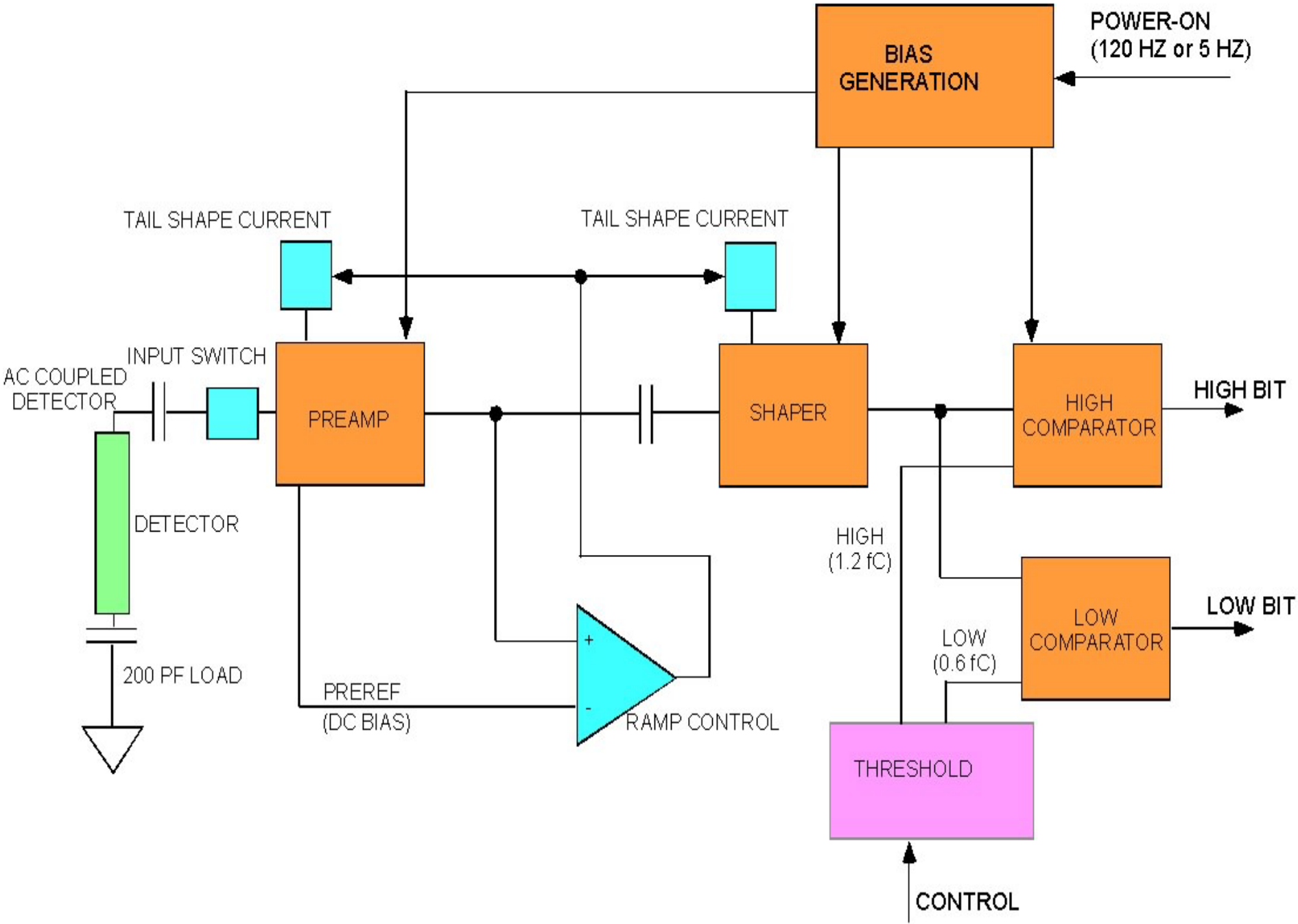
Result: S/N for 167cm Ladder





At shaping time of 3μs; 0.5 μm process qualified by GLAST

SILICON TRACKER FRONT-END ARCHITECTURE



THE BAD NEWS

ASIC submitted 11/04 in 0.25 μm TSMC mixed signal RF; received 12/04

Chip shows no life; inspection reveals vias between pads and circuitry not present (our mistake)

Attempts to install via with FIB (focused ion beam) technology not successful.

BUT:

We need to re-optimize for superconducting beam

We are now up to speed on 0.25 μm; expect to re-submit in May; results by August.

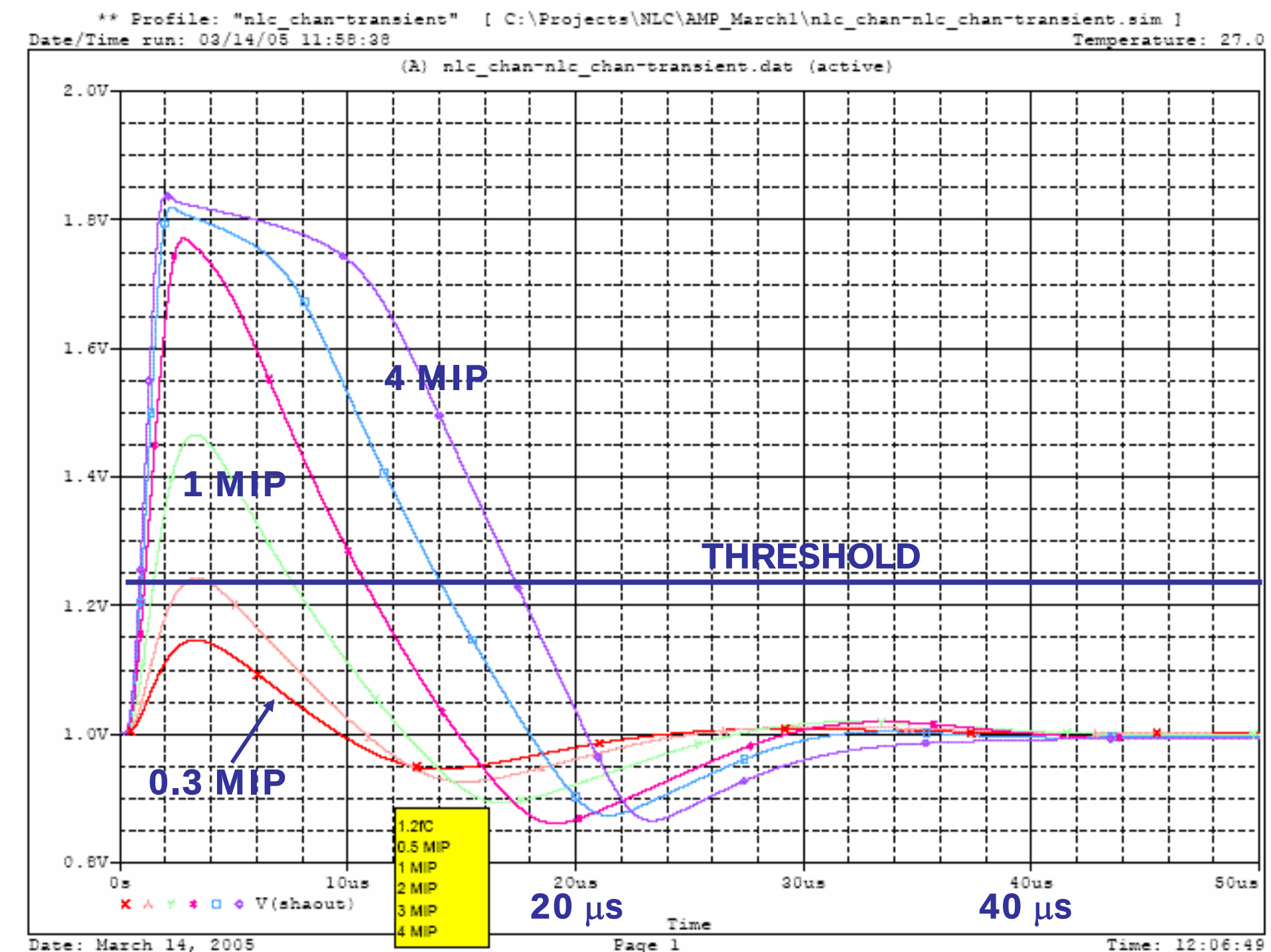
Cold Technology Issues

Power switching less demanding (5 vs 120 Hz)

Need to worry about dead time as channel recovers from noise hits, with frequency f_n:

$$f_n = \frac{1}{4\sqrt{3}\tau_s} \exp\left(-\frac{1}{2} \frac{Q_{thresh}^2}{Q_{noise}^2} \right)$$

From our simulation, for 167cm ladder, Q_{thresh}/Q_{noise}=3.8 ➔ 35 Hz noise rate, or .029 per TESLA train. If recovery kept to 25μs, this is about 0.08% dead time recovering from noise hits (roughly the same on innermost layer due to physics occupancy!).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Date/Time run: 03/14/05 11:58:38
Temperature: 27.0
(A) nlc_chan-nlc_chan-transient.dat (active)
2.0V
1.8V
1.6V
1.4V
1.2V
1.0V
0.8V
4 MIP
1 MIP
THRESHOLD
0.3 MIP
1.2fC
0.5 MIP
1 MIP
2 MIP
3 MIP
4 MIP
0s
10us
20us
30us
40us
50us
V(shaout)
20 µs
40 µs
Time
Date: March 14, 2005
Page 1
Time: 12:06:49

Some Issue to Explore with a Test Beam Run

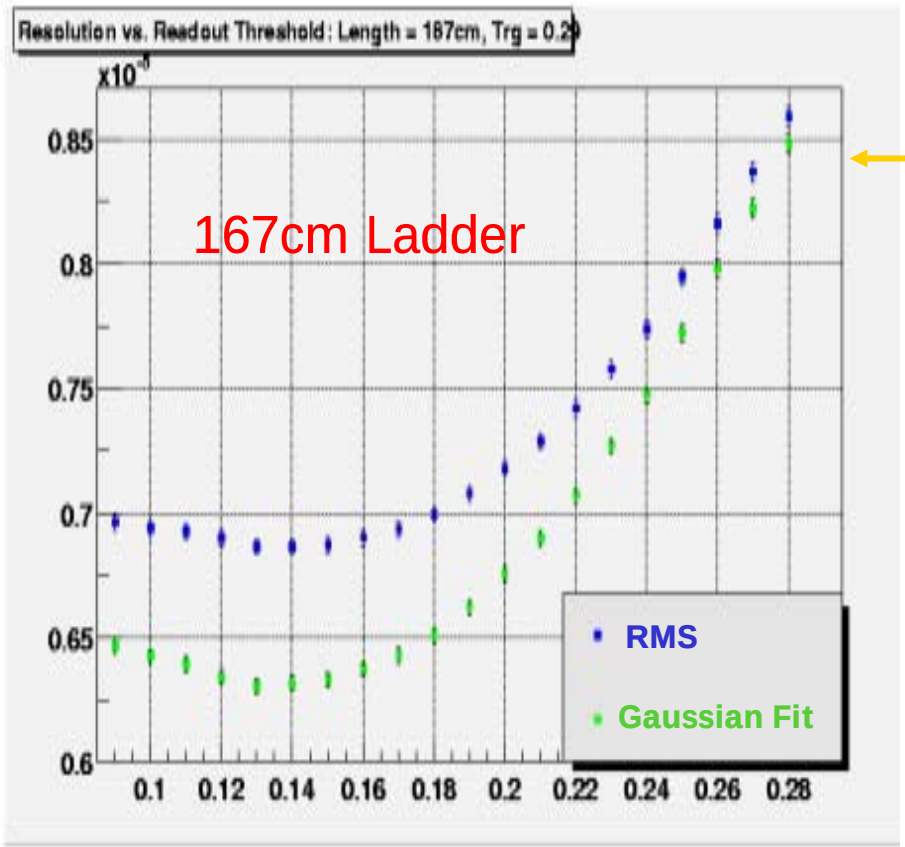
Bruce Schumm, SiLC meeting 2/16/05

This talk will be geared towards long shaping-time silicon readout, as informed by common sense plus our pulse development simulation.

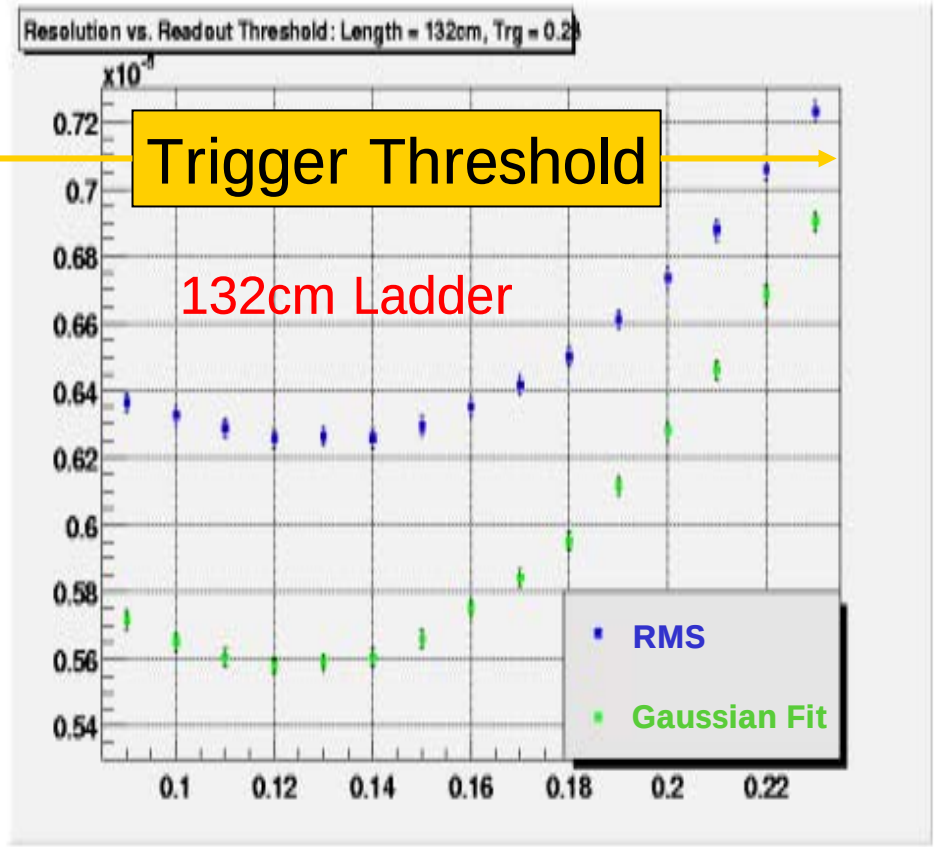
Primary issues:

- Power cycling
- Signal/noise (long ladders); efficiency and occupancy
- Point resolution
- Analog resolution (dE/dX)

Resolution With and Without Second (Readout) Threshold

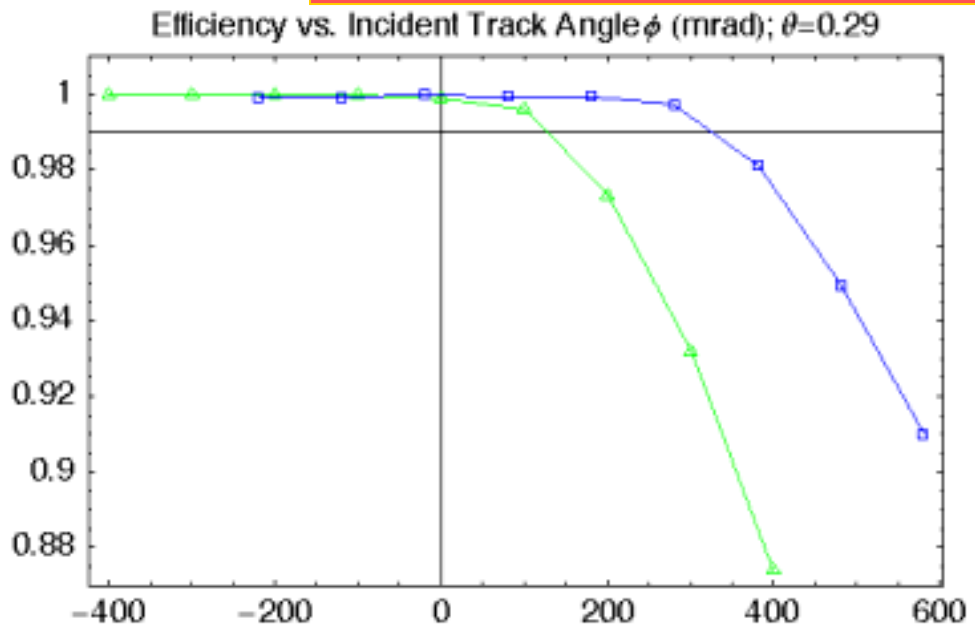


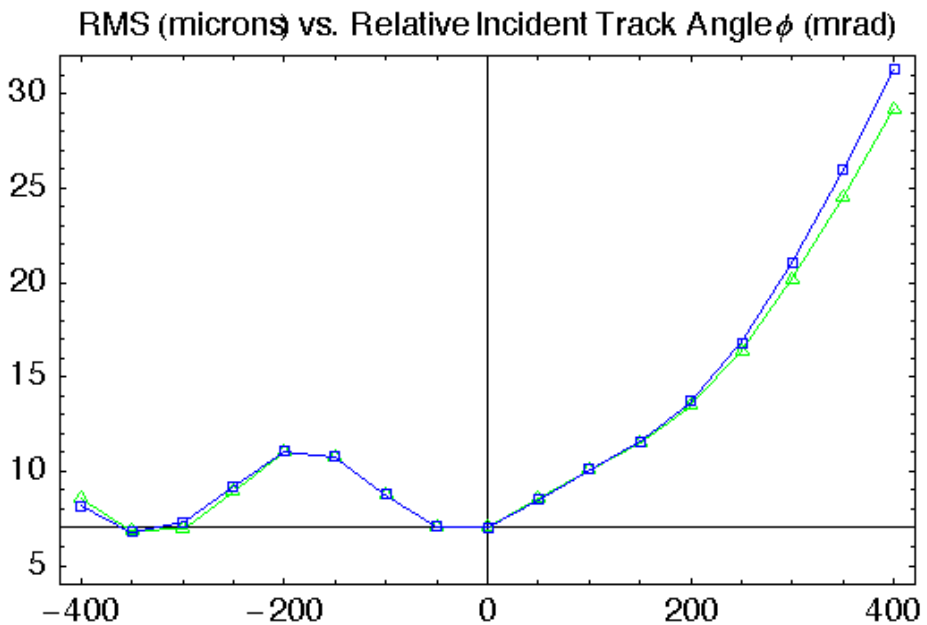
Trigger Threshold

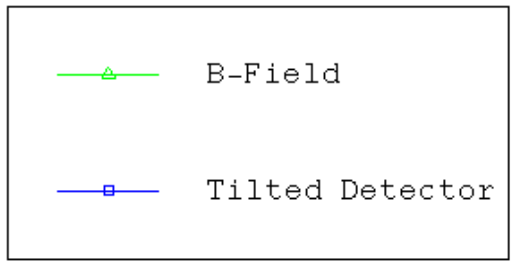


Readout Threshold (Fraction of min-i)

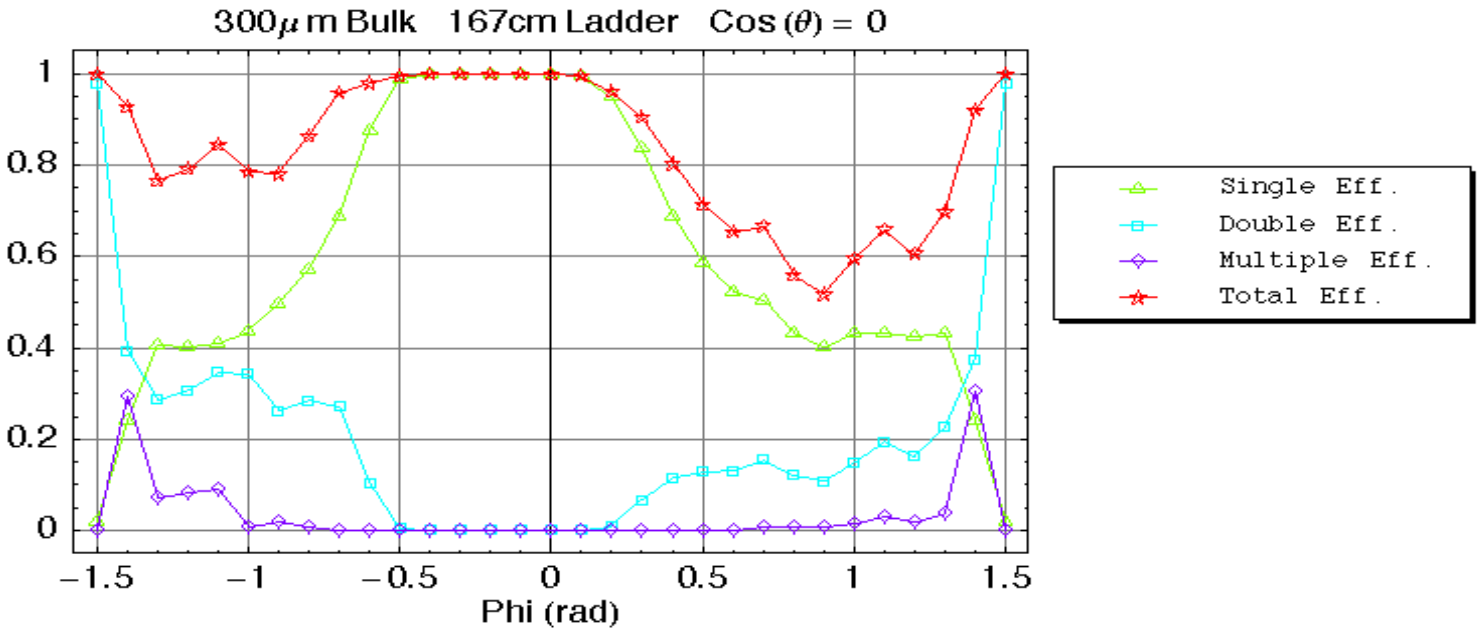
Non-normal incidence

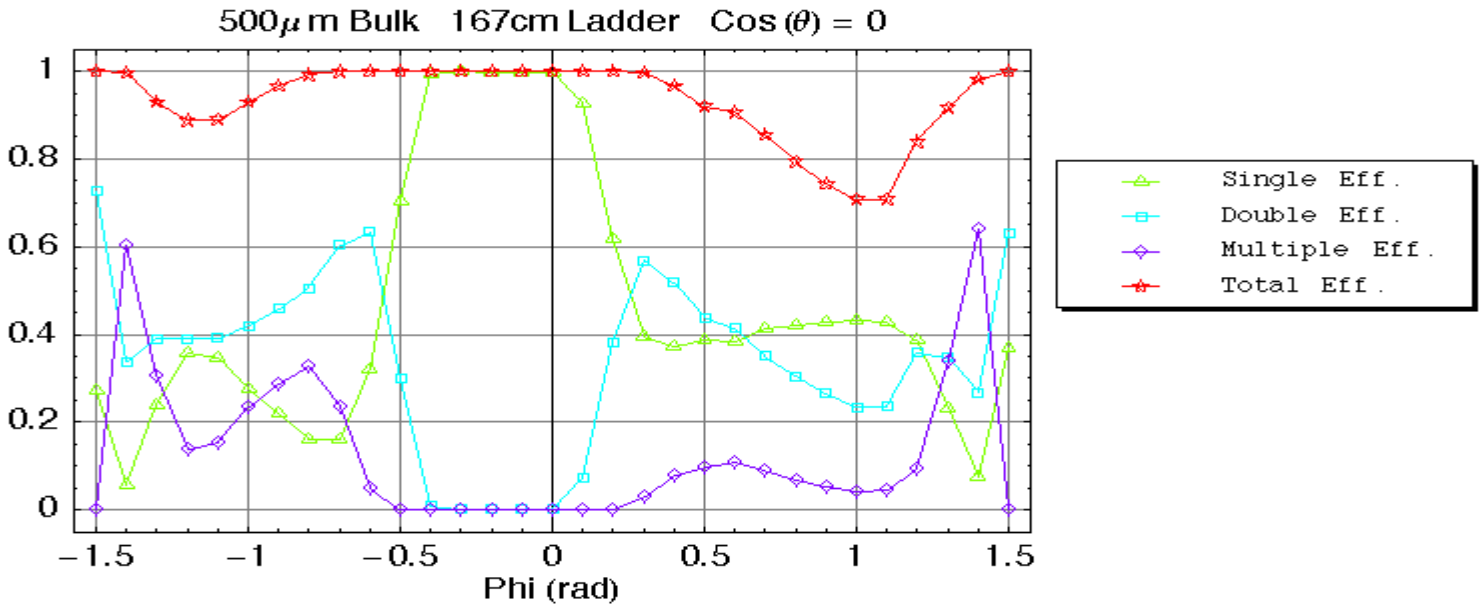






Thicker Sensors in Outer Layers?





SUMMARY

Sullen admission that first prototype chip was DOA

Second iteration to be submitted in May; optimized for cold technology

But still working towards testbeam run in Fall 2006. Critical issues requiring testbeam are:

- Efficiency/occupancy, as a function of entering pitch and dip angles
- Resolution, and resolution vs. angle
- Efficiency/resolution vs. sensor thickness
- How high a magnetic field can we do our studies in?