Front-End and Readout Electronics for Silicon Trackers at the ILC

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On behalf of
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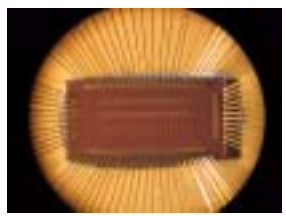


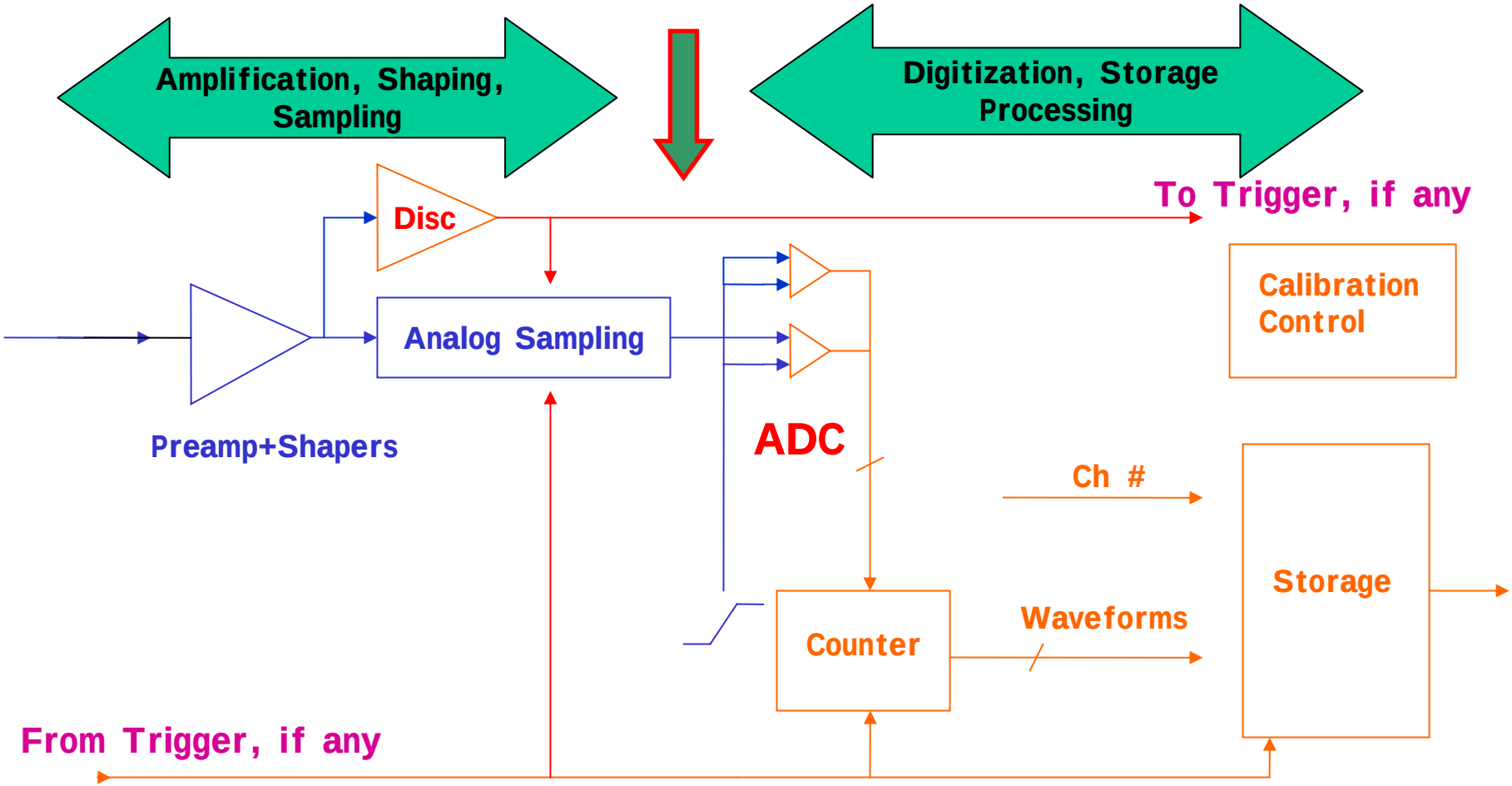
Summary

Silicon Tracker	a few $100m^2$, a few 10^6 strips
Asynchronous events	~ 1 ms
Data taking/pre-processing	~ 200 ms
Occupancy:	< 1 % in most parts of the detector

Goals:

Low noise preamplifiers
Shaping times 500ns - 5μs (Strip length dependent)
Analog sampling
Highly shared ADC
Sparsification
Very low power dissipation
Power cycling
Compact and transparent
Choice of DSμE
SiGe under consideration for VFE analog

Front-end processing

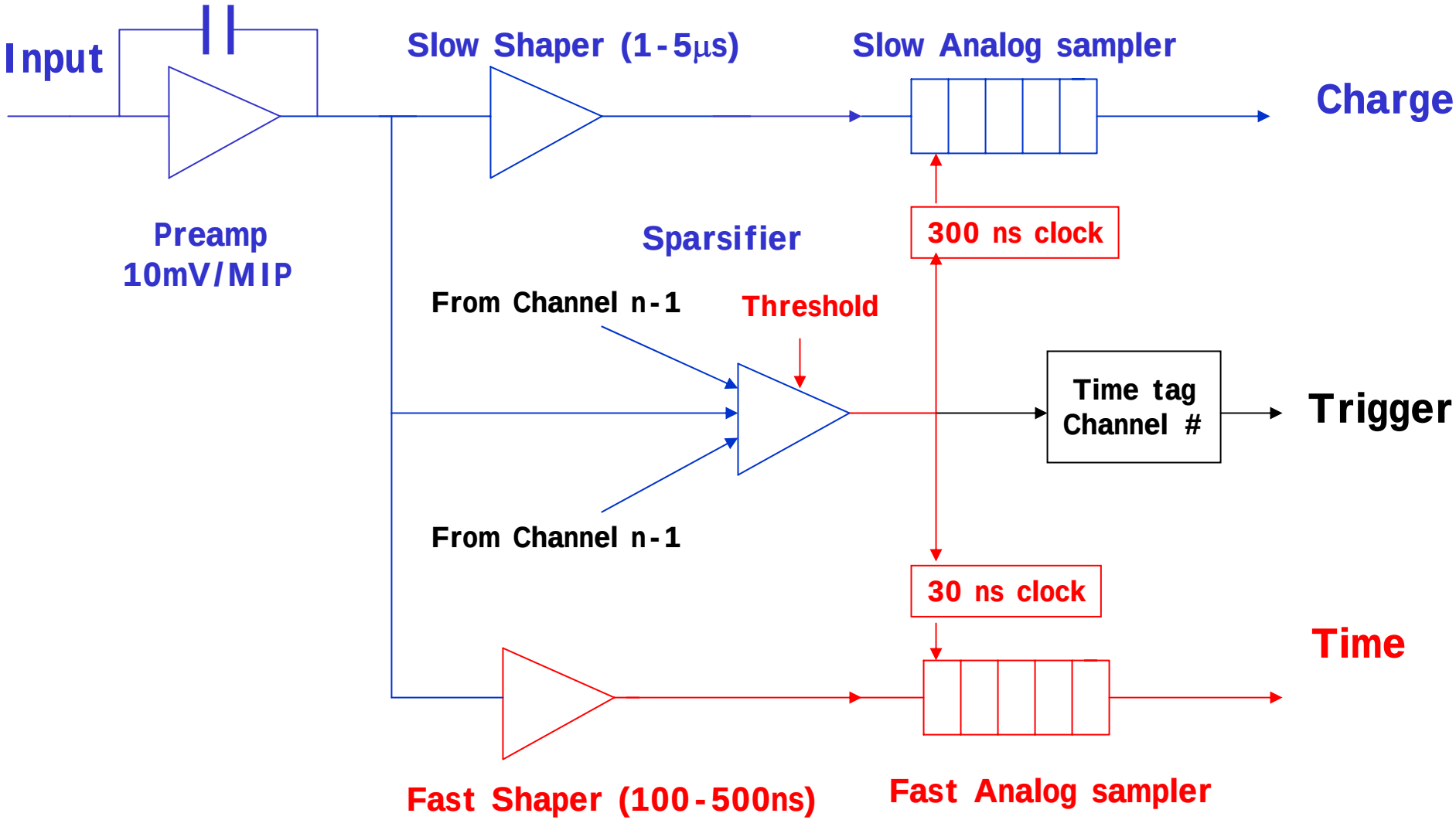


Charge 1-50 MIP, S/N~15-20

Technologies

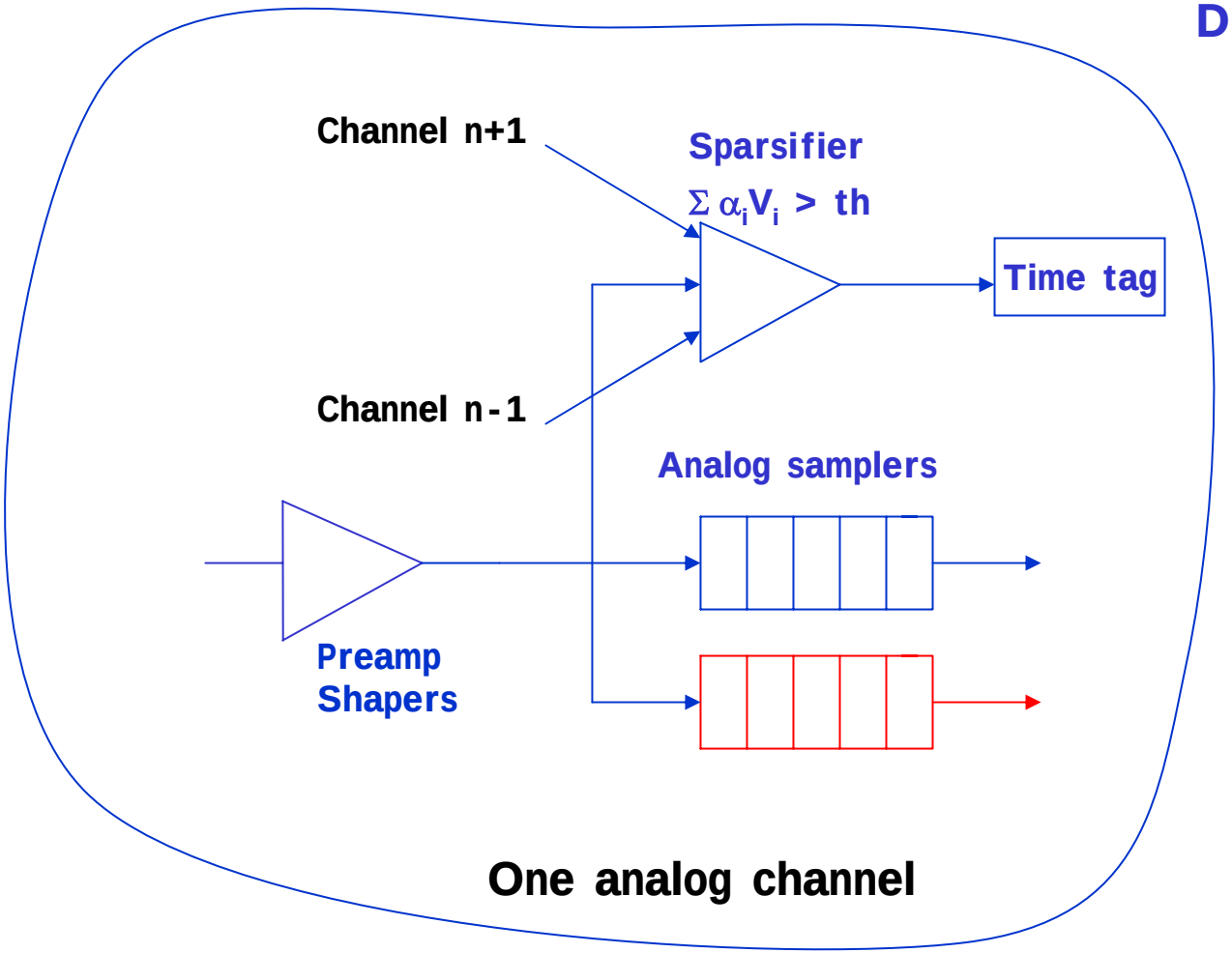
- **Deep Sub-Micron CMOS UMC 0.18 μm**
- **SiGe envisaged for analog section**

Analog Pulse Sampling Front-end under evaluation
Very preliminary ideas

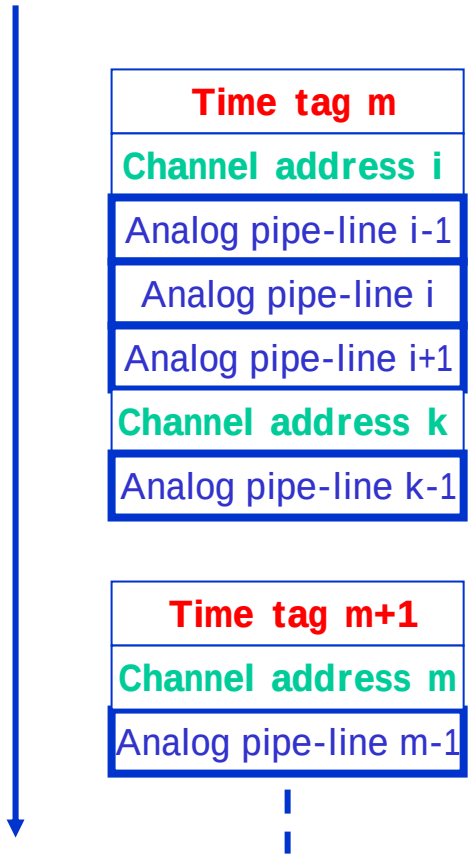


Silicon area and power dissipation investigated

Analog storage, digitization and sparse readout

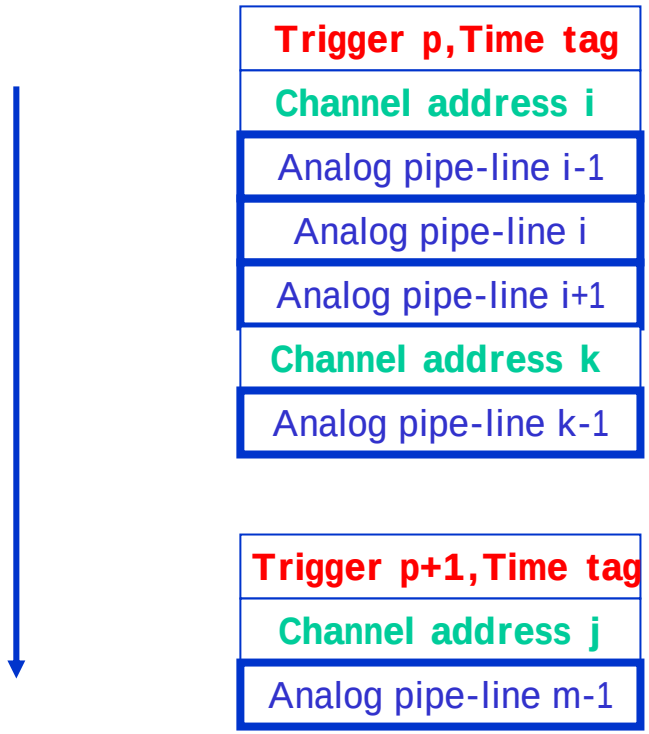


Digitization



Analog sampling after each local event
Digitization after each train

Triggered readout ?



Shorter pipeline length
By how much ?
To be evaluated

Increased deadtime ?
To be evaluated

Analog sampling on each local event
Sparse readout after each trigger

Required/Expected Performance

Noise, gain:

- Preamp + Shaper

@ 3 μs shaping time, 50 pF detector
simulated ENC 920 e- 85 e- + 16.5 e-/pF

Gain 8mV/MIP over 1-75 MIP

Power:

- Preamp + Shaper + Analog Sampler

Preamp: 70 μW Shaper: 110 μW Analog sampler 200 μW ?

· Shared ADC/TDC

ADC: 10 bits, 2-3 μs, 110 μW

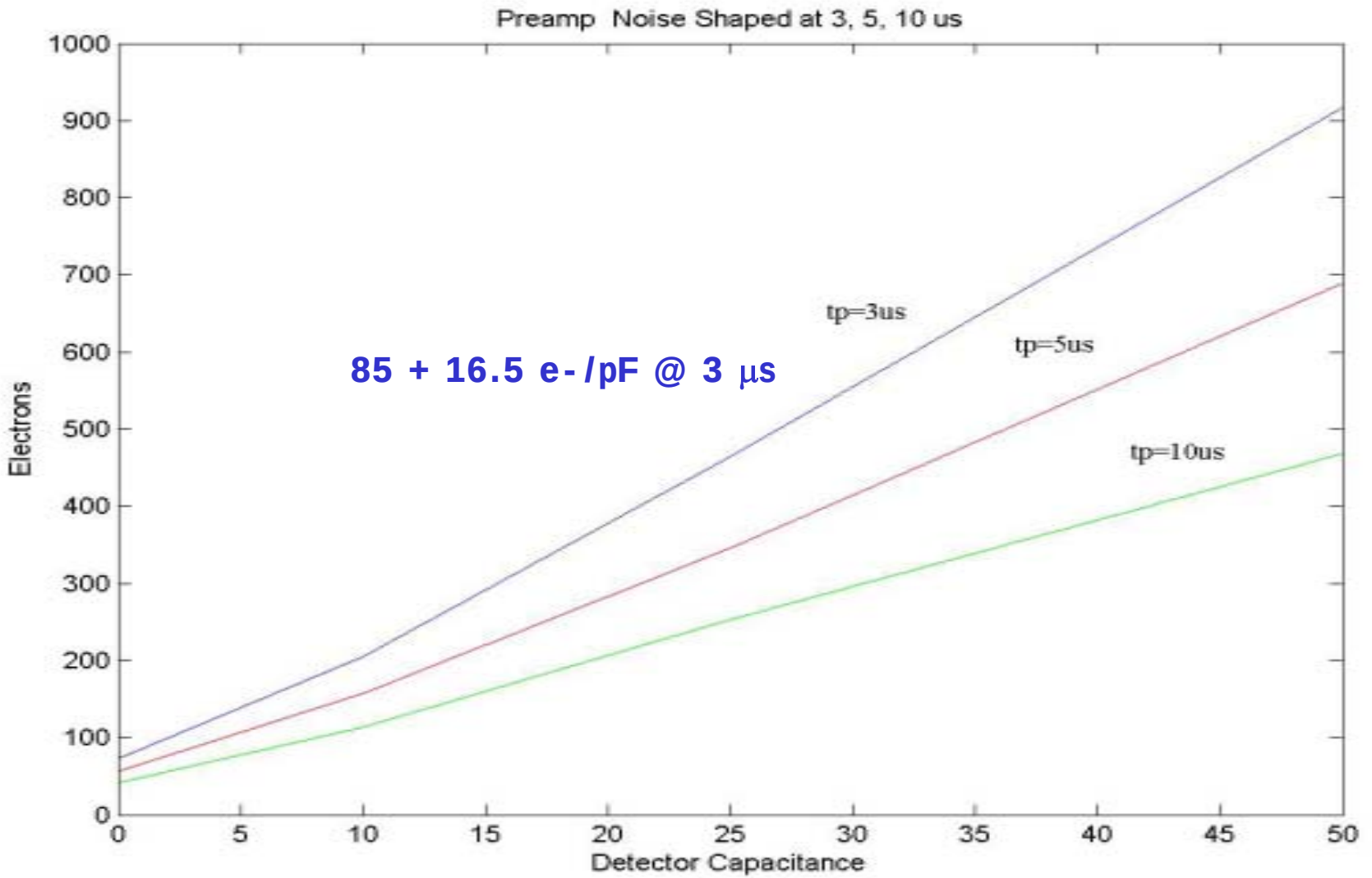
Total: ***300 + 200 μW / channel***

Power Switching:

If Analog + ADC are running during collisions only:
e.g. 1.2/100 duty cycle and 5 10^6 channels, then:

Total: **500 10^{-6} x 5 10^6 x 1.2/100 =** ***30 Watts***

Noise (Simulations)



Consider Silicon-Germanium technology as faster/less noisy alternative

Overall Noise

g_m = 0.69 mA/V @ 60 μW power
τ = 3μs
C= 50 pF
I_{leak} = 10nA
R_{bias}= 10MΩ

Detector + FET Leakage: $N_{leak} = e/q\ \mathrm{sqrt}(q\ I\tau/4)$

Bias resistor: $N_{bias} = e/q\ \mathrm{sqrt}(\tau\ kT/2R)$

$$N_{tot}^2 = N_{fet}^2 + N_{leak}^2 + N_{bias}^2$$

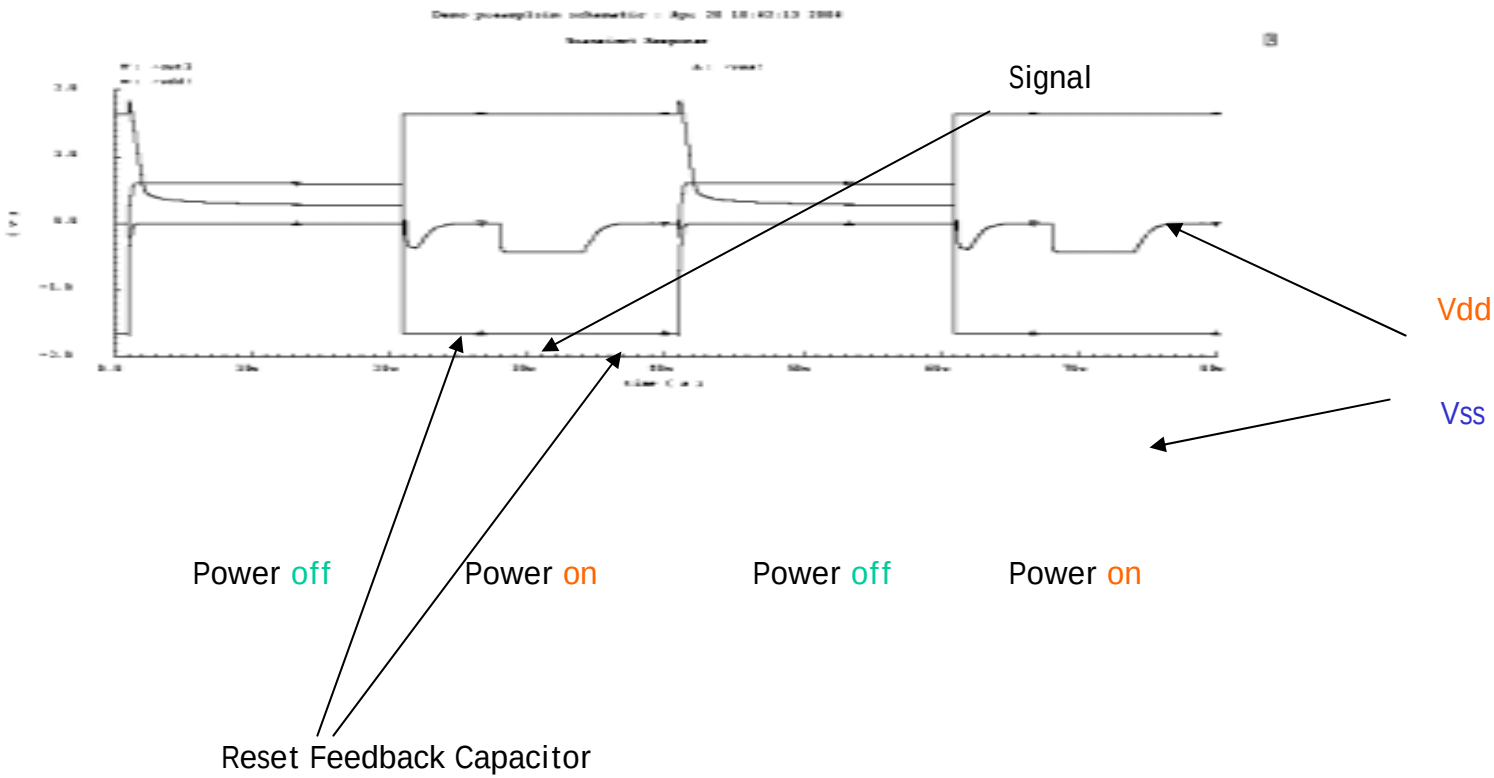
N_{fet}= 910 electrons
N_{leak}= 588 electrons
N_{bias}= 423 electrons

N_{tot}= 1163 electrons

Preamp Power Switching (reminder)

- Reset the feedback capacitor after switching on and before switching off (Takes 5 us)

- Open and close two switches feeding Vdd Vss (Ron~=100 Ω) Power is zero when switched off



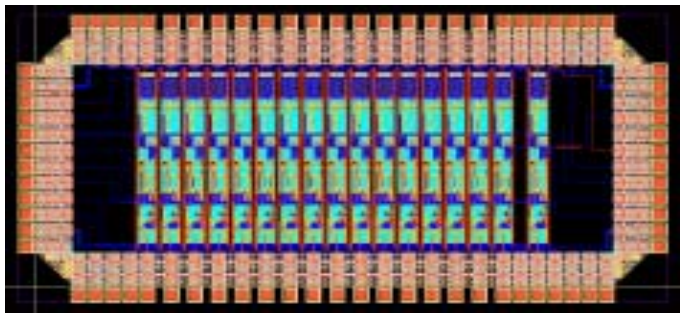
Prototype chip received February 28th

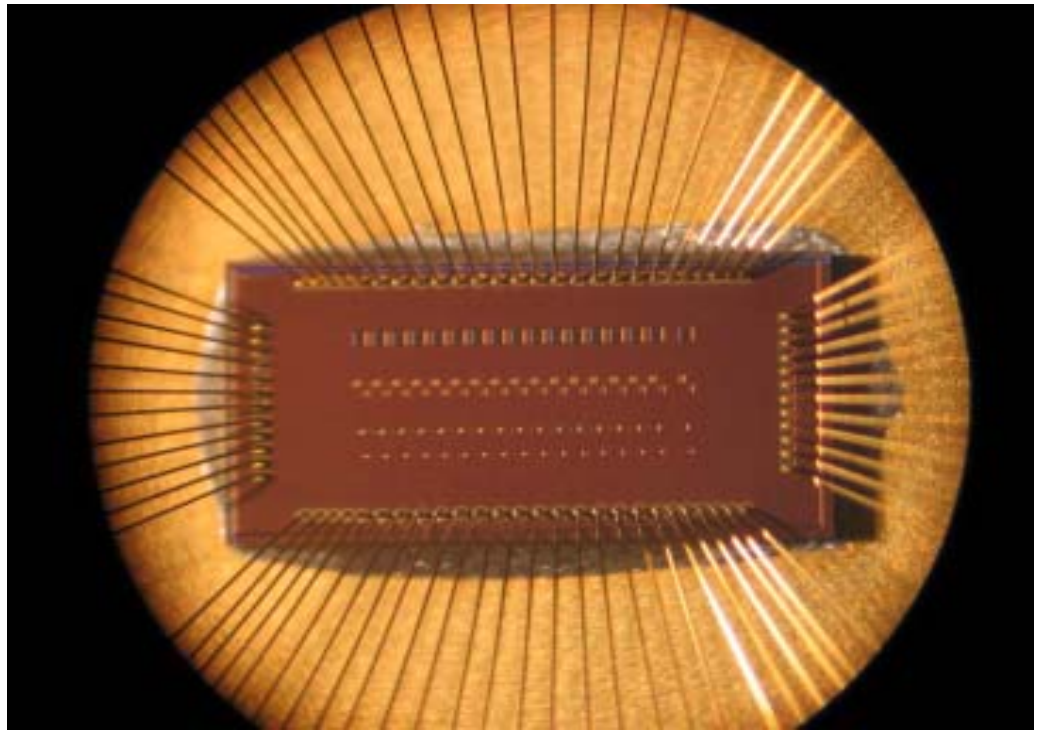
One analog channel

UMC 0.18 μm CMOS *Europractice (Leuven, Belgium)*

- **16 ch + 1 Preamp, Shaper, Sample & Hold, ADC Comparator**
- **Two blocks of 1.6 x 1.6 mm² each**

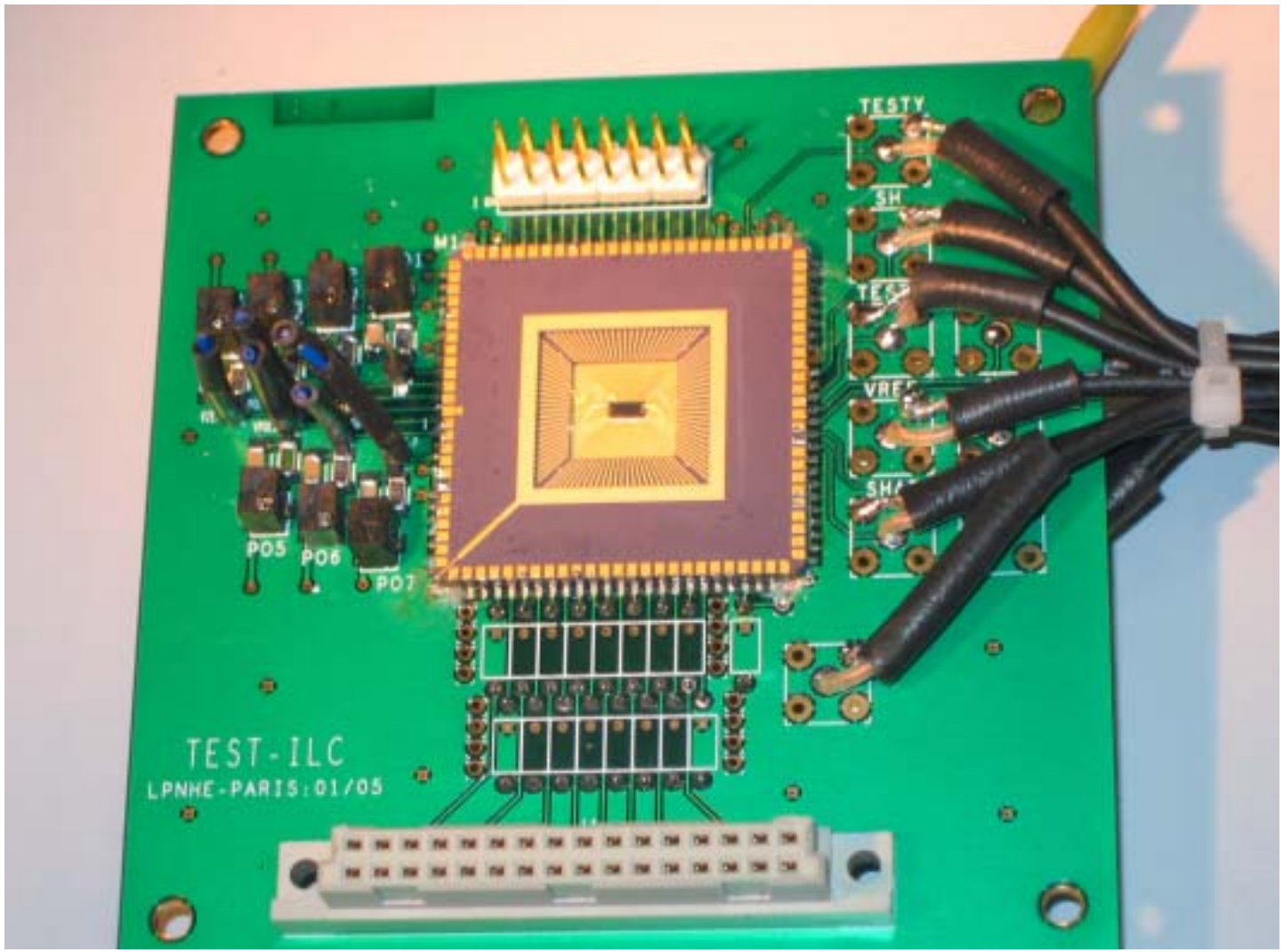
Silicon





16 + 1 channel UMC 0.18 um chip (layout and picture)

Test Card

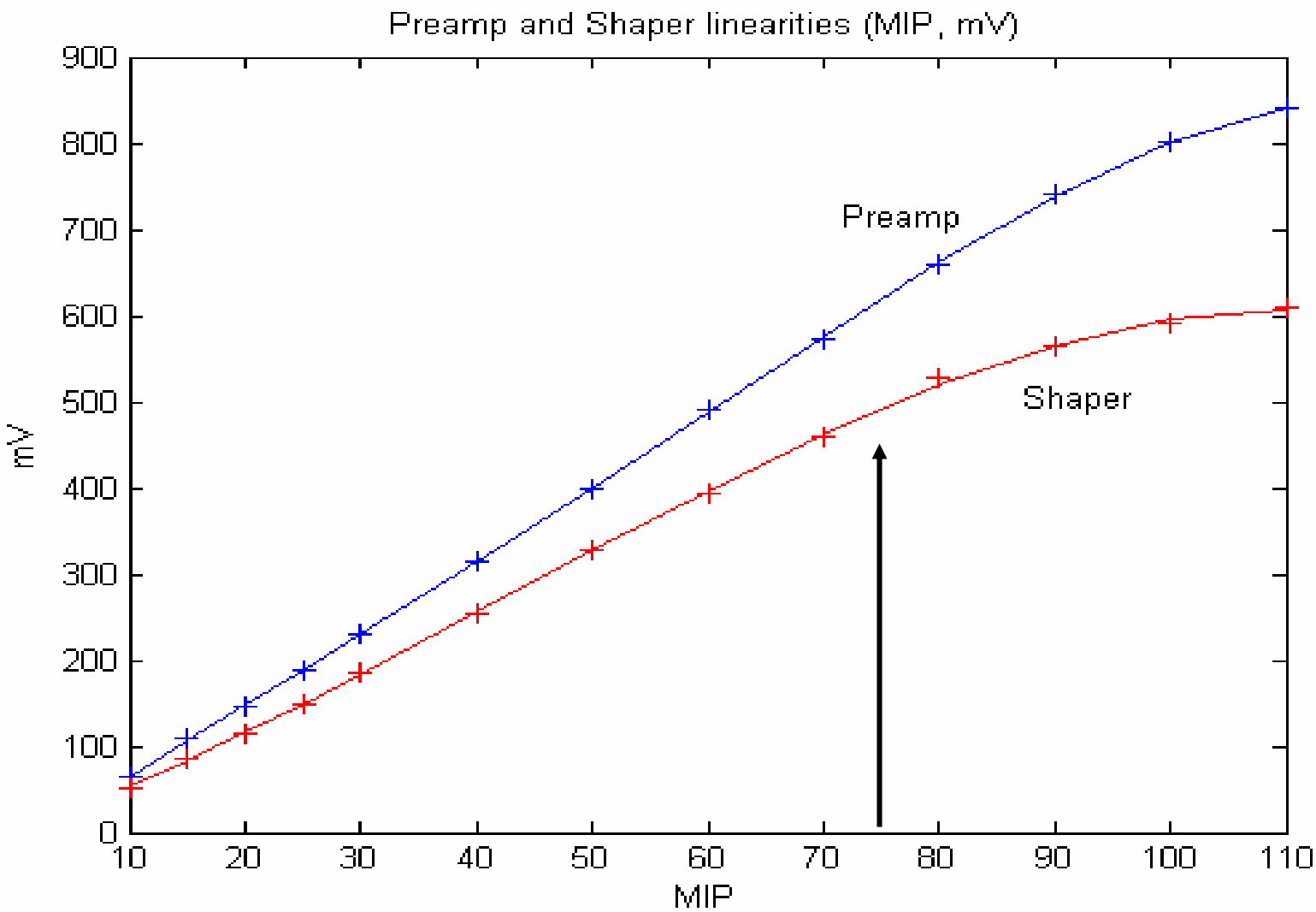


Just received !
Very first preliminary results

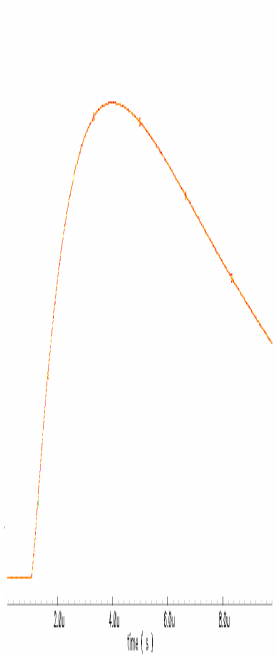
Two tested chips fully functional

Preamp + Shaper	**Under**		
	Preamp: Gain	**8mV/MIP**	**OK**
	Linearity	**+/-1.5%**	
	Dynamic range:	**75 MIP**	**OK**
	Noise @ 3.3pF input cap, 3 μs shaping time:		
		205 e-	**140 e- expected**
Shaper:	**2 - 10 μs tunable peaking time**		**OK**
Power:	**Preamp**	**90 μW**	**70 μW expected**
	Shaper	**110 μW**	**OK**

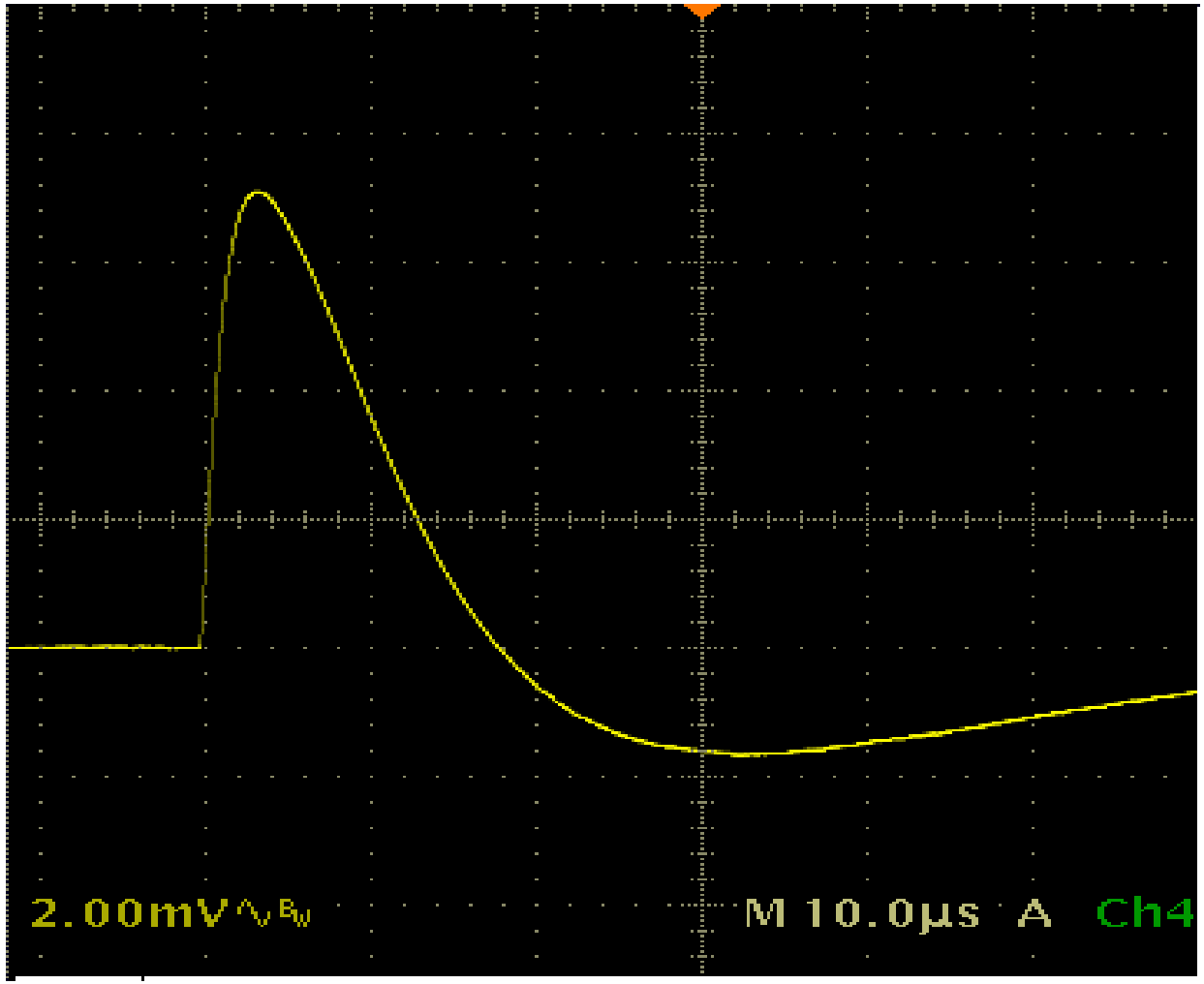
Linearities



Shaper waveform



Spice output



Shaper output at 4 us peaking time (8 MIP input)

After these very promising first results, much more tests to be done…

Future

➔ Complete the present chip tests
➔ Tests with actual Silicon detectors

Next version will greatly benefit from these thorough series of tests

➔ Submit a 128 channel chip fall '05

Will include:

➔ Analog
- Fast and slow shapers
- Sparsifier
- Analog samplers

➔ Digital
- Full ADC
- Buffering

➔ Follow the trend towards shorter gate lengths: .09μm when available and after .18 μm is fully mastered

Conclusion

Deep Sub Micron CMOS technology:

- Allows to implement a highly integrated front-end for SiLC that does not degrade the detector resolution, both in time and amplitude within an affordable power and material budget.

- Allows to implement system integration such as calibration, data compaction, cluster centroid, fast tracking algorithms.

- The present design can be adapted to shorter time shaping to equip shorter strips.

- First Silicon chip in UMC 0.18 μm CMOS was just received, and is being tested. Very promising first results.

- 128-channel chips including analog sampling, ADC and the digital part for the next version hopefully submitted Fall '05

- Multiplexing up to 512 channels to ADC is foreseen

- SiGe technology considered as a possible competing technology for analog.