Performance of an ILC-DEPFET System

Bonn – Mannheim – Munich Collaboration

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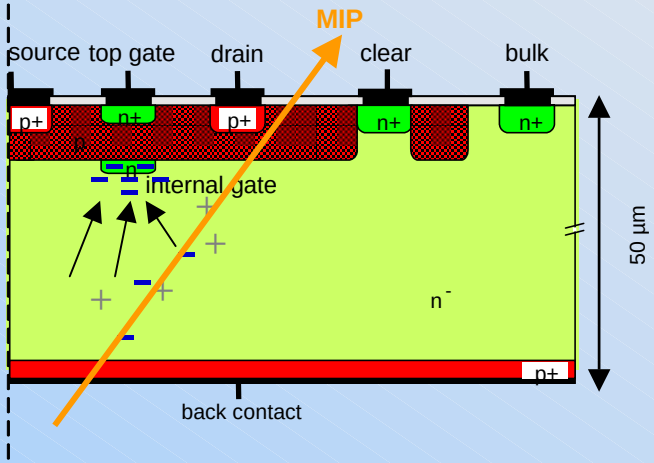
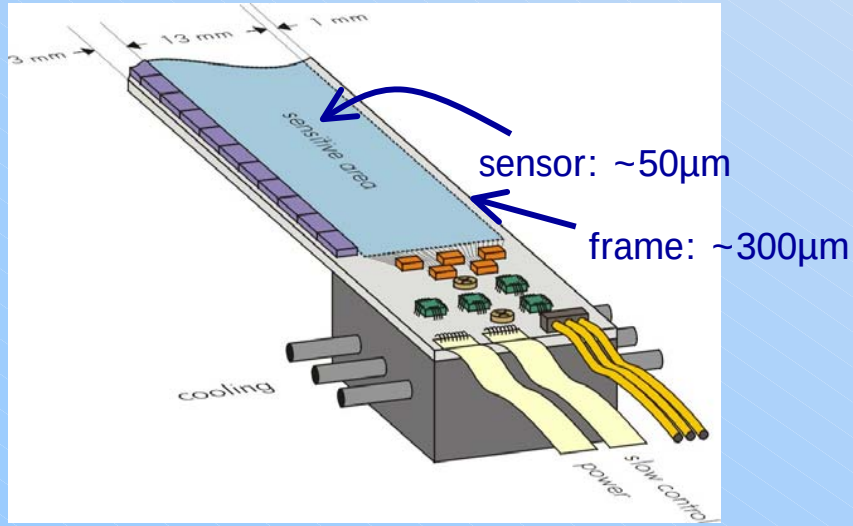
outline

- DEPFET features for an ILC vertex detector
- ILC-DEPFET System
- System Performance
- Testbeam @ DESY
- Summary / Outlook

DEPFET features for the ILC vtx-d

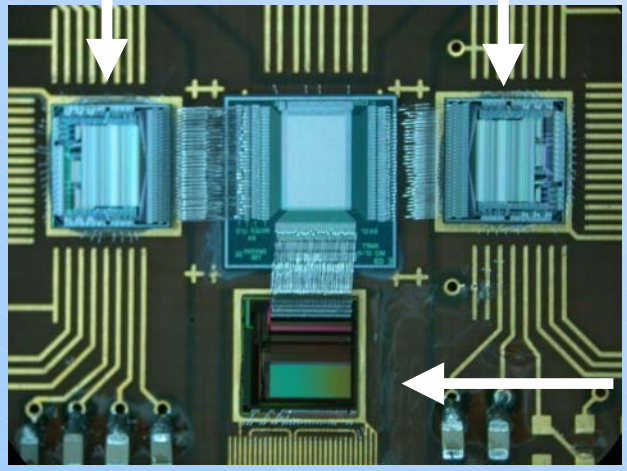


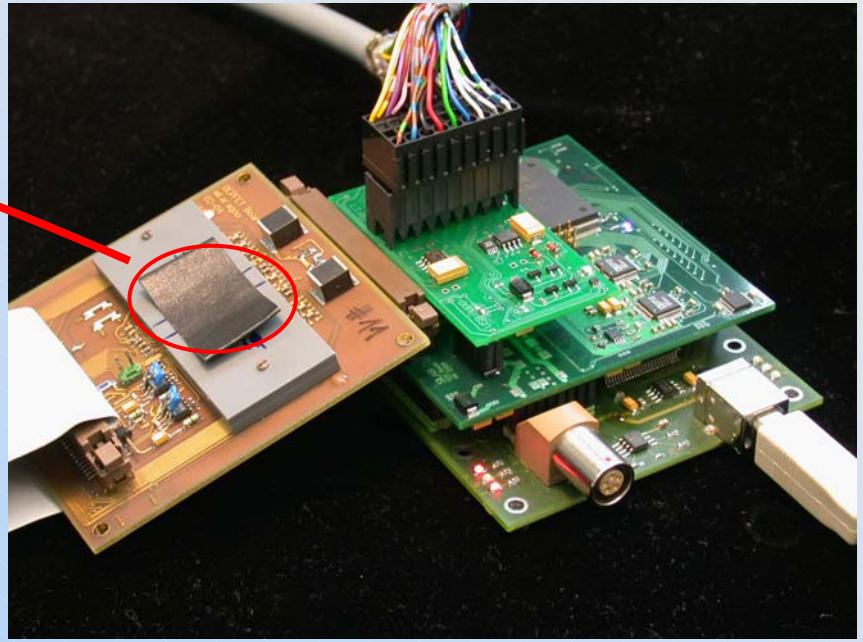
charge collection in fully depleted substrate



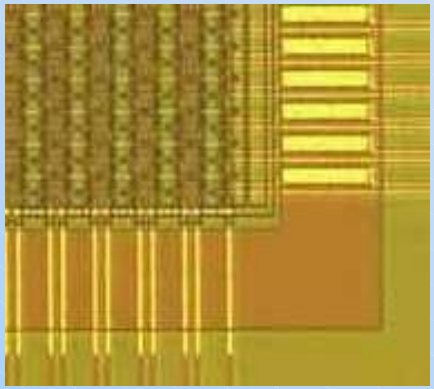
- small pixels 20-30µm
- radiation tolerance (>200krad)
- low noise
- thin devices (50µm) → S/N = 40
- low power (row-wise operation)
- fast readout (cold machine), 50MHz line rate
- zero suppressed data

ILC-DEPFET system



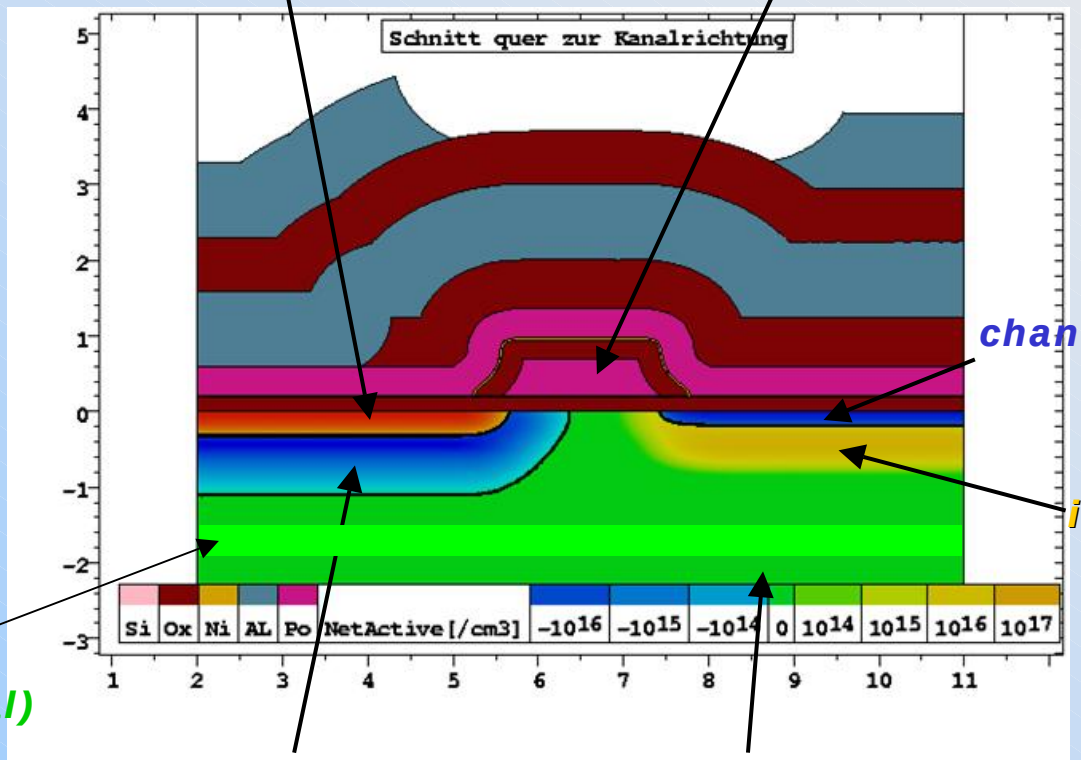


Sensor: clear efficiency



64x128 pixel
double metal matrix
(20x30µm^2 pixels)

<u>for ILC:</u>
no clocking of the clear-gate



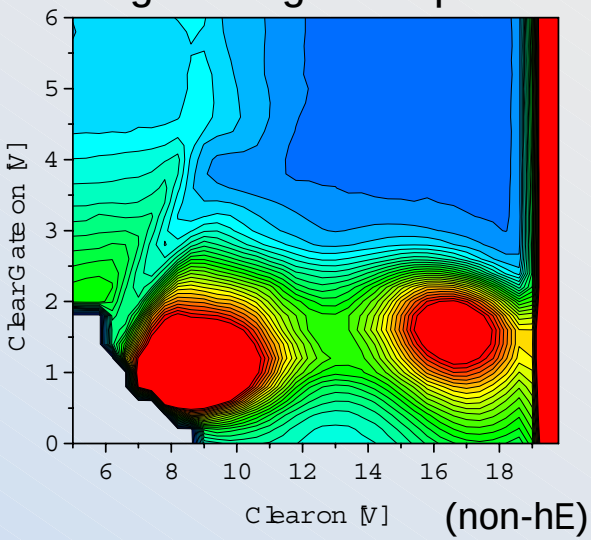
clear efficiency (cont'd)

DEPFET parameters analyzed to find optimal design:

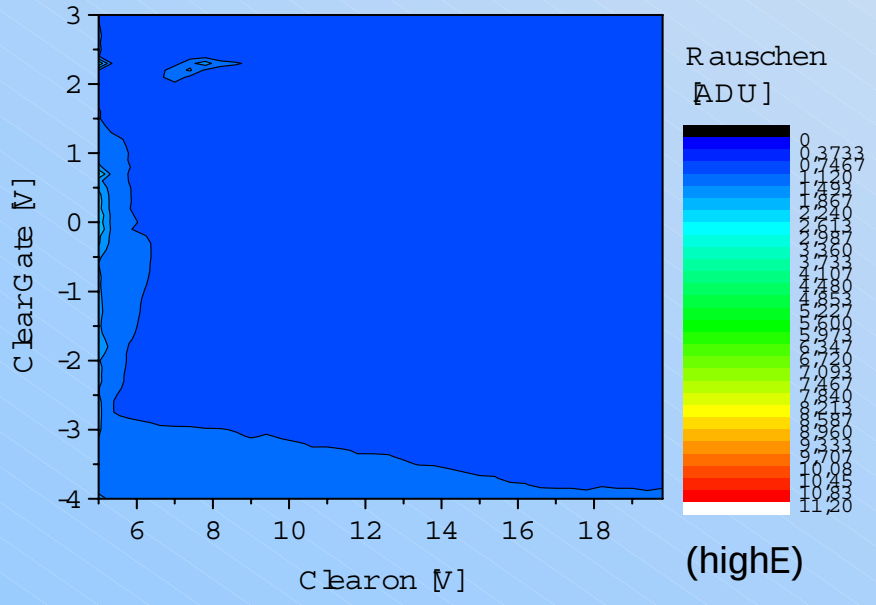
- **highE / non-hE**
- **clear – gate length, overlap**

Complete clear with non-clocking clear gate !

Cl-gate length=7.2µm

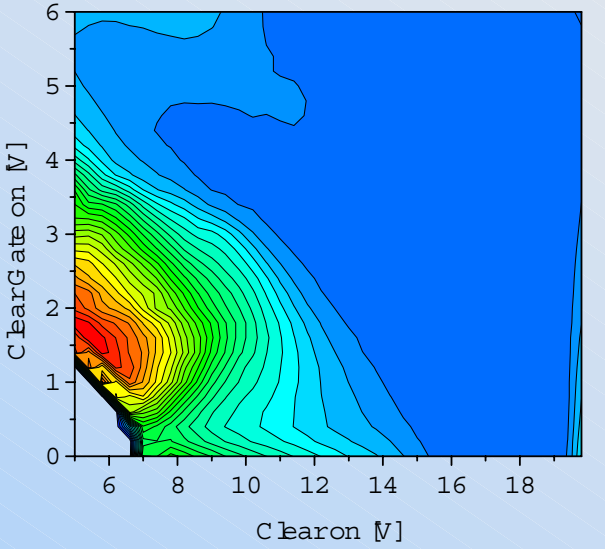


(non-hE)

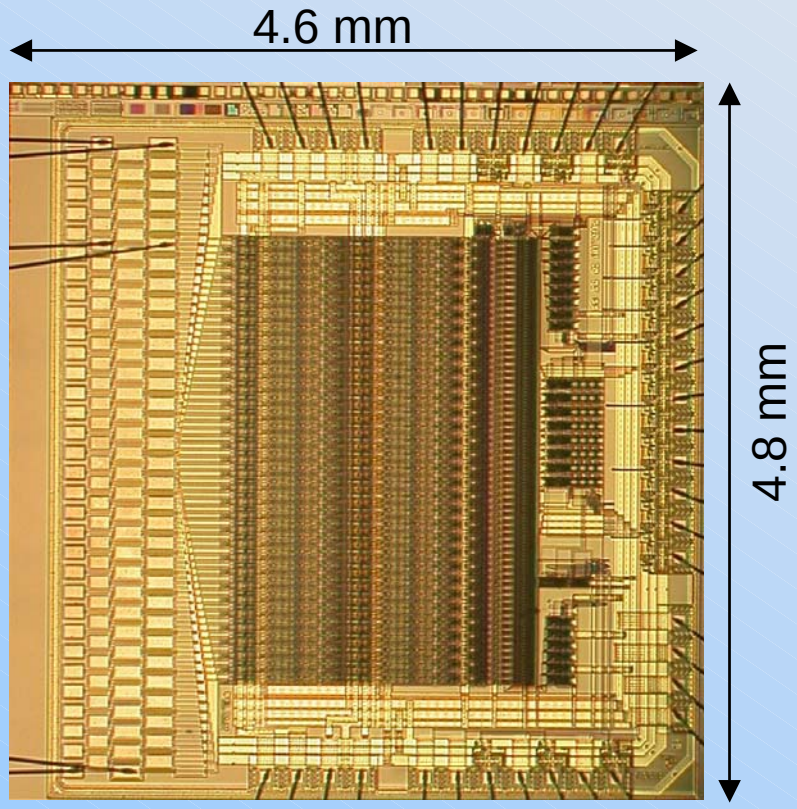


(highE)

Cl-gate length=4.2µm



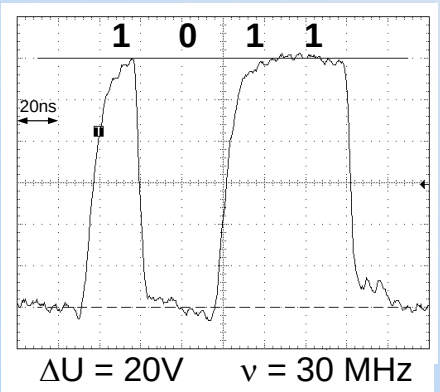
ASIC development (Switcher)



Features:

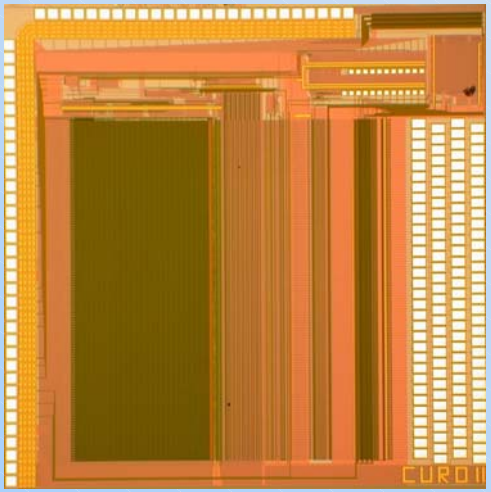
- **produced 1/2003**
- **2 x 64 channels**
- switches between 0 and 20 Volts (adjustable)
- **ground levels arbitrary**
- internal sequencer **(flexible pattern)**
- **daisy chaining of several chips for modules possible**
- **0.8 µm HV - technology**

„analog“ performance:

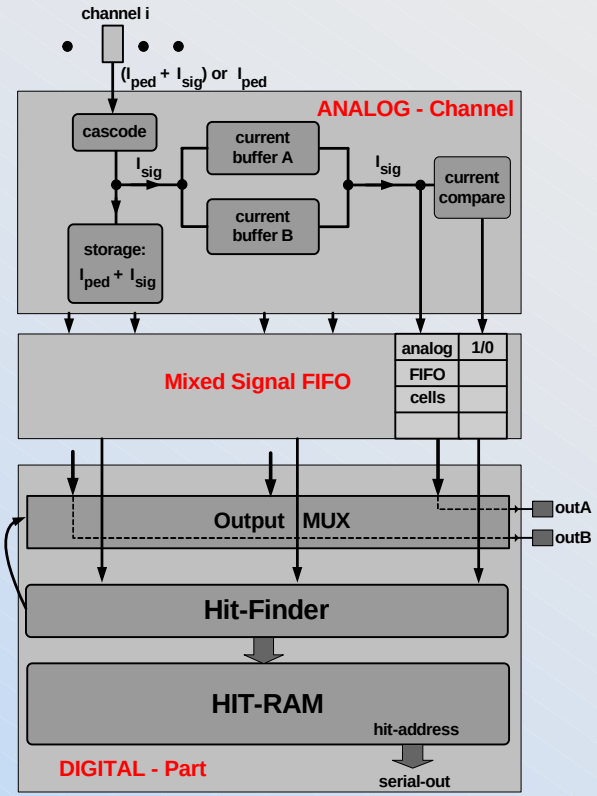


- functionality proven ✓
- **RAM & sequencer (digital) tested up to 80 MHz**
- Power consumption ~ 1mW / channel @ 30Mhz

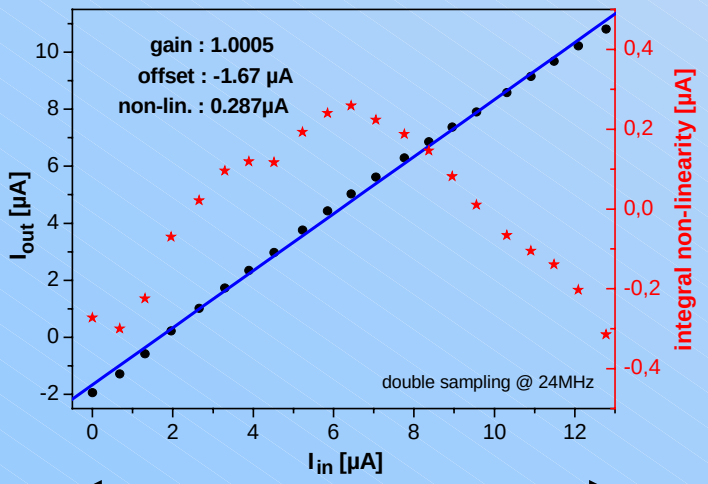
ASIC development (CURO)



- Noise contribution: ~50 e-
- 0-suppression > 100MHz
- analog sampling tested up ~50MHz

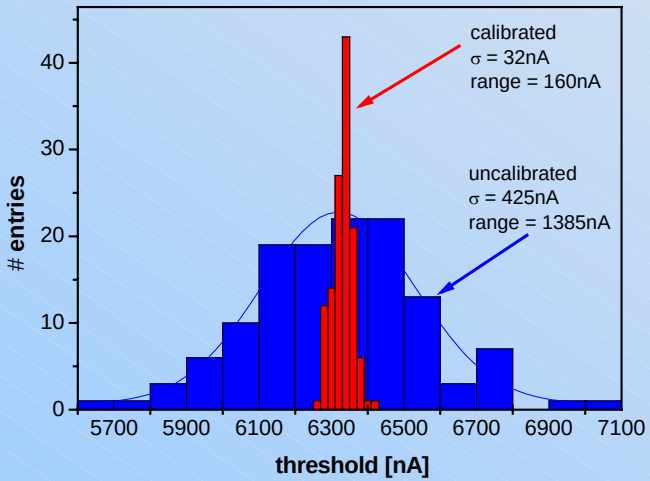


Linearity:



> 5mips

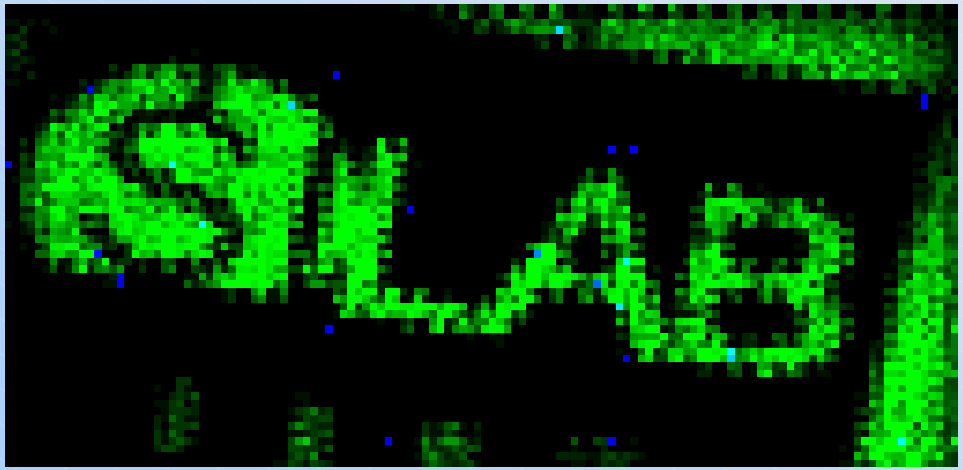
Calibration:

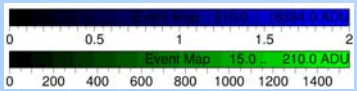


- current mode based
- fast correlated double sampling
- on chip 0-suppression

DEPFET-System in the lab

^{55}Fe (6keV γ) radiogram





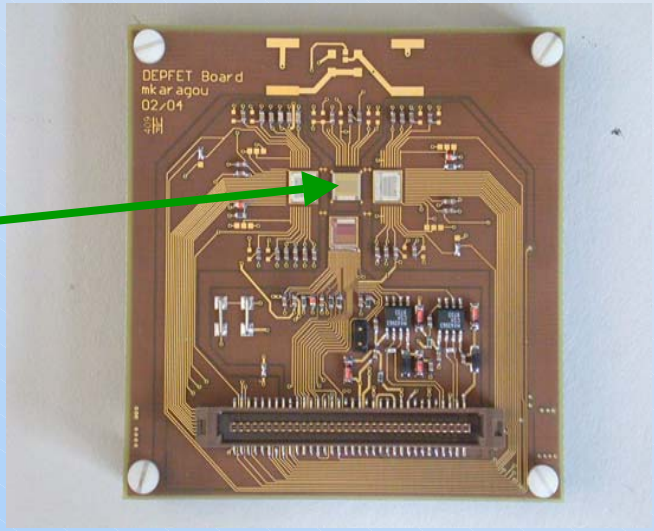
Current system performance:

- line rate: ~1MHz
- noise: 230e$^-$ (due to pick-up)

Tungsten-Logo:

2.7 mm

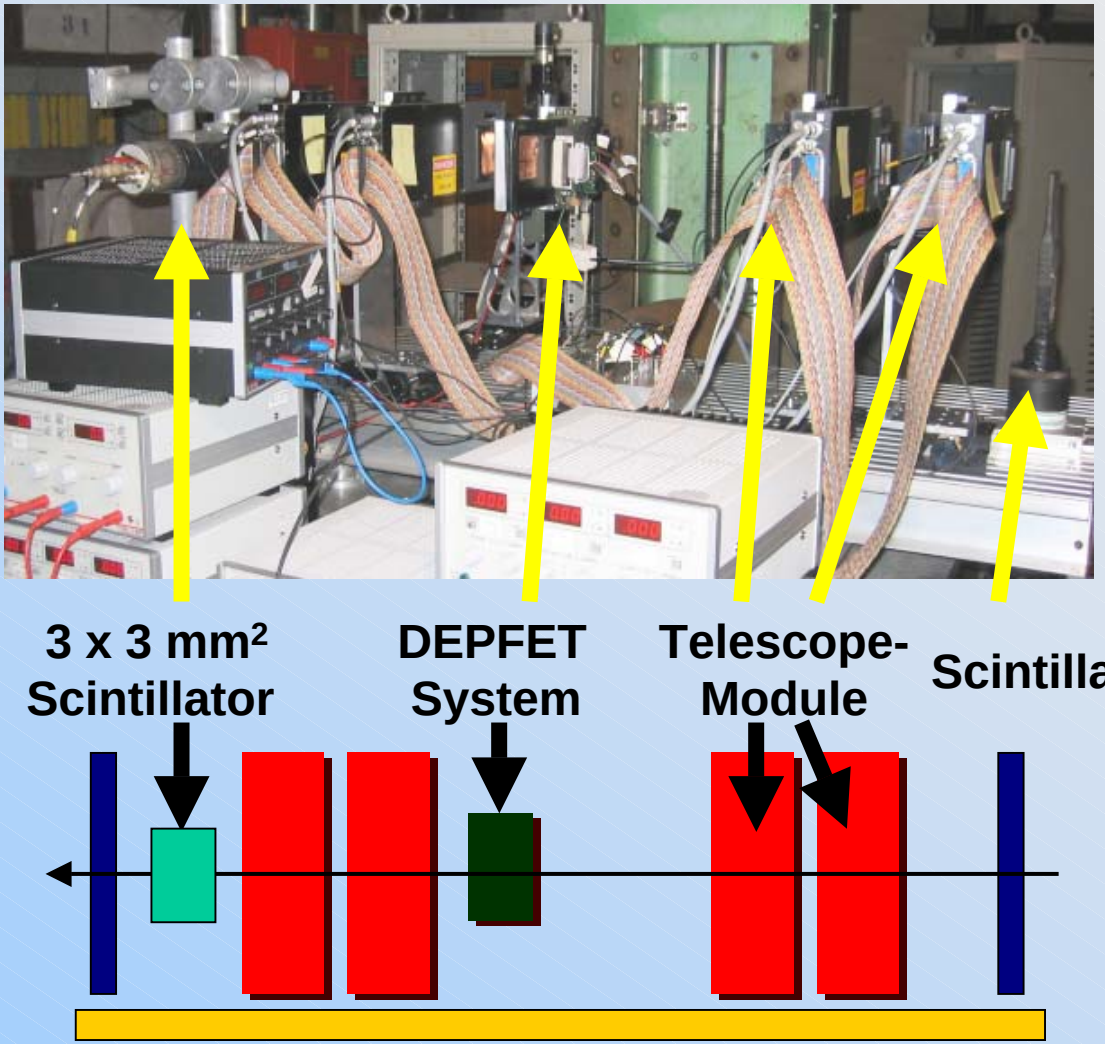
3.4 mm



Testbeam: Setup

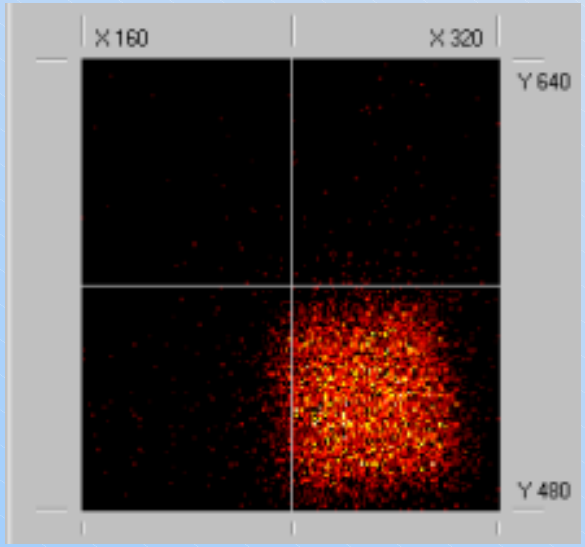
Testbeam 24 @ DESY

Jan + Feb 2005

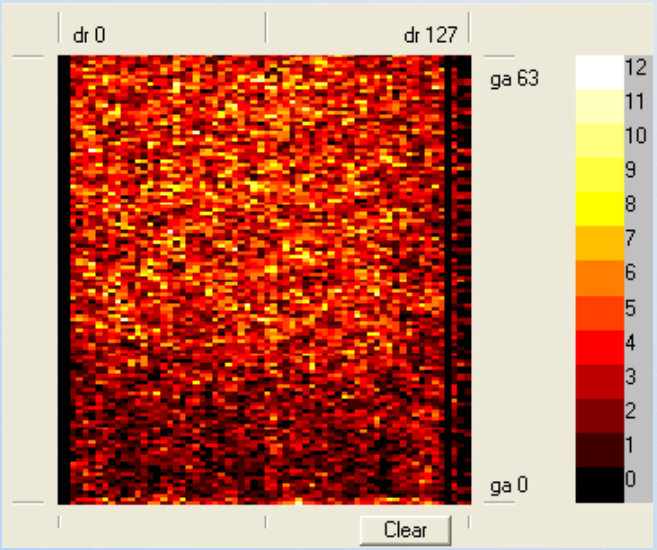


first „results“

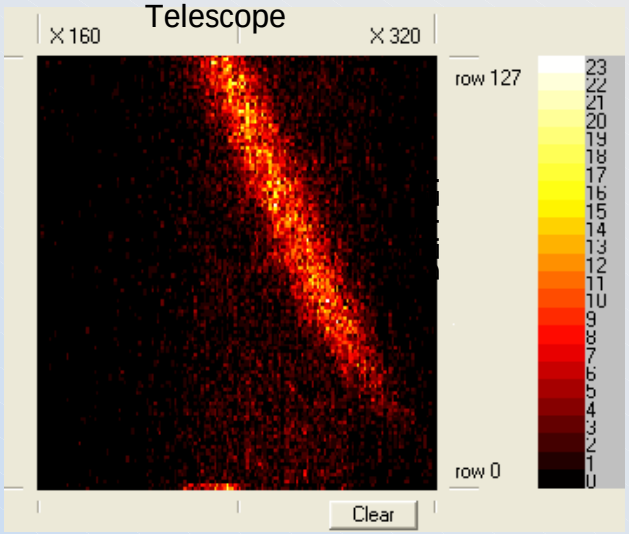
Telescope:



DEPFET:



Correlation:

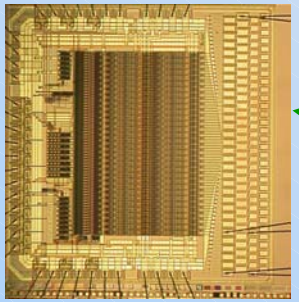


- **Event rate: 10Hz**
- **collected data: 10 million events**
- **two DEPFET - designs (highE / non-hE) in beam**

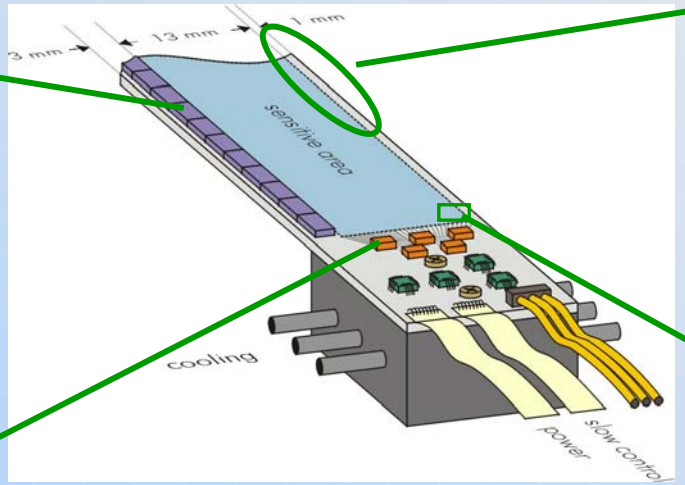
data anlysis ongoing

Summary / Outlook

Switcher (steering)



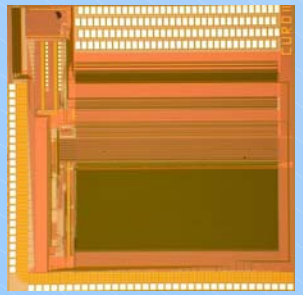
- driving voltages up to 20V
- line-rate: ~30MHz



thinning

PiN-diodes thinned to 50µm
(wafer bonding, anisotropic etching)

CURO (readout)

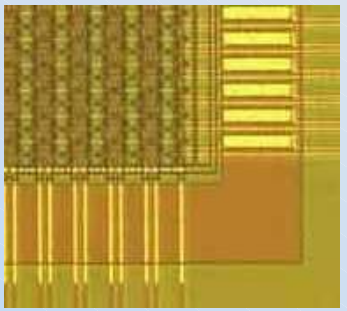


- fast current based readout concept
- on chip 0-suppression > 100MHz
- line rate: ~25MHz

outlook:

- increase system speed (currently 1MHz)
- radiation tolerance of steering chip ?
- larger matrices (512x256 pixels)
- stay tuned for testbeam results !

Sensor



- complete clear proven

→ no reset noise

END

Charge collection

Voltages during charge collection

- Clear off [V]
- Clear Gate off [V]

L-Gate	6 µm	$U_{Clear\ on}$	18,0 V
L-CG	4,2 µm	$U_{CG\ on}$	4,0 V
overlap	1,5 µm	U_{Bulk}	5,0 V