Fine Pixel CCD Option for the ILC Vertex Detector

19 Mar. 2005

@LCWS2005

Y. Sugimoto

KEK

Vertex Detector Options

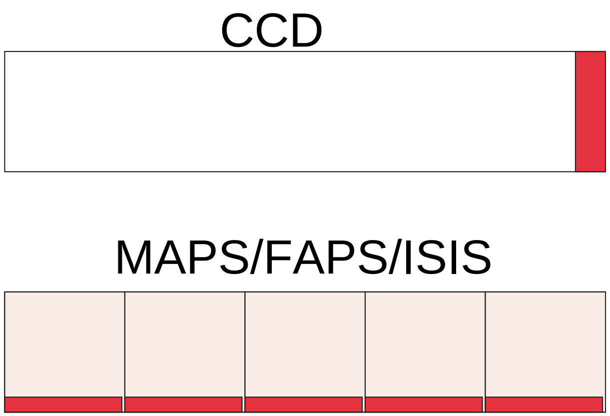
- If the hit signal is accumulated for one train of 2820 bunches, too many hits by beam b.g. → for 25 μm pixels, the pixel occupancy > 20%
- Solutions;
  - Fast readout : Column Parallel CCD @50MHz, 20 frames/train
    - Possible effect by RF noise by beam
  - Analog registers in each pixel (~20/pixel), and readout between trains
    - CMOS: Flexible Active Pixel Sensor (FAPS)
    - CCD: In-situ Storage Image Sensor (ISIS)
    - Complicated structure → Large area OK?
  - Make pixel density x20→**Fine Pixel CCD (FPCCD)**

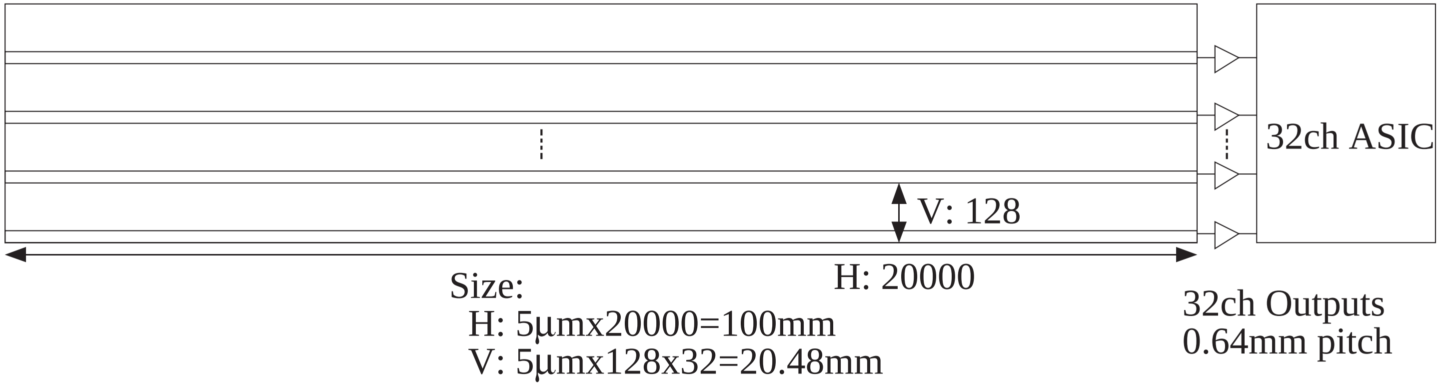
Vertex Detector Options

- FPCCD
  - Accumulate hit signals for one train and read out between trains
  - Keep low pixel occupancy by increasing number of pixels by x20 with respect to “standard” pixel detector
  - As a result, pixel size should be as small as ~5x5μm^2
  - Epitaxial layer has to be fully depleted to minimize charge spread by diffusion
  - Operation at low temperature to keep dark current negligible (r.o. cycle=200ms)

Advantages of FPCCD

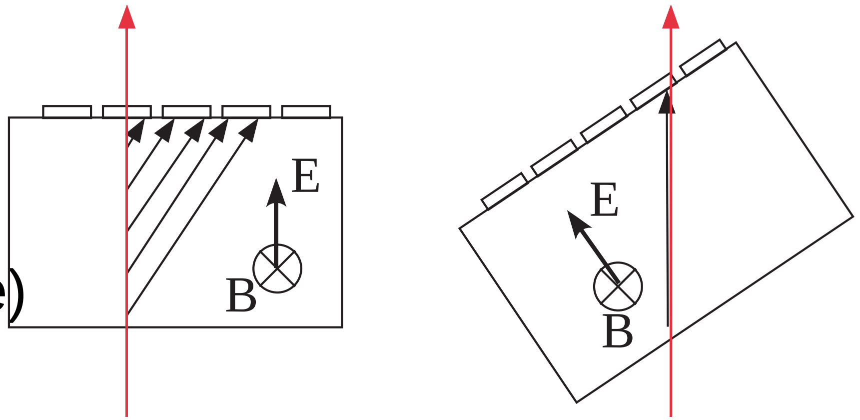
- Free from beam-induced RF noise
- σ_x~1.4μm even with digital readout
- Simple structure : advantageous for large size
- Active circuit on one edge : easy to control temperature
- Readout speed: 15MHz is enough (128(V)x20000(H)/200ms=12.8MHz) (CPCCD:>50MHz)





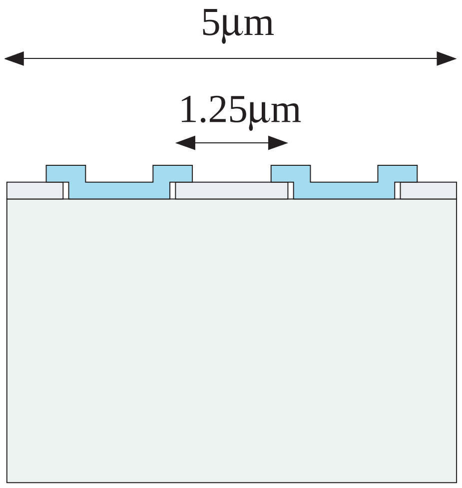
Challenges of FPCCD

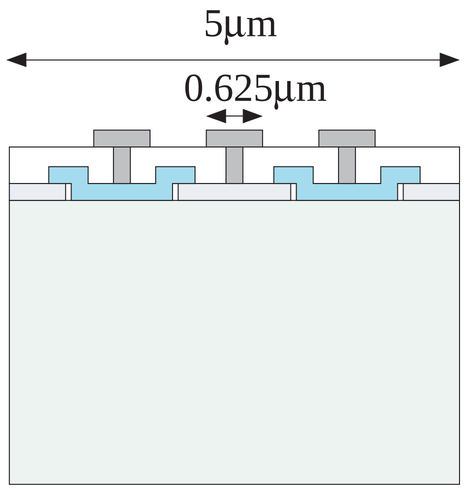
- Pixel size
- Horizontal register in image area
- Tracking efficiency
- Thin wafer and support structure
  - 50μm thick, 20x100mm^2
- Lorentz angle
  - Low B is preferable
- Readout electronics
  - Signal level is small (~500 e)
- Radiation hardness
  - Relaxed by low temp. operation



Pixel Size

- 5μm pixel of fully depleted CCD has full-well capacity of only few k electrons
- CCD process
  - 5μm pixel with poly-Si gate is easy (1.6μm pixel CCD for cameras on mobile phone already exists)
  - Large size and fast readout require Al layer
  - Large size CCD with 5μm pixel with poly-Si gate and metal layer is not easy



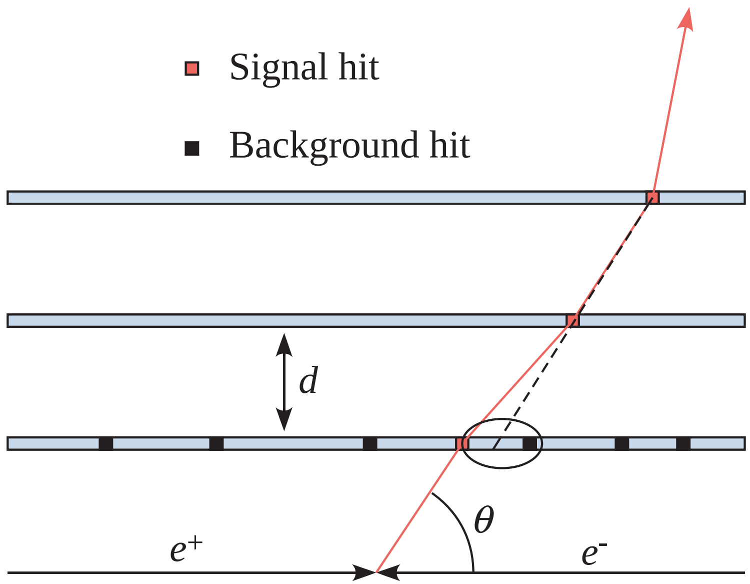


Tracking Efficiency

- In FPCCD, pixel occupancy would be low (~1%) but hit density mainly due to the pair-background is as high as ~40/mm^2 (B=3T, R=20mm, L=3.4x10^{34})
- So, it is not trivial whether we can get good tracking efficiency
- Extrapolation of tracks from Si intermediate tracker (SIT) with bunch ID capability will be necessary
- The study of tracking efficiency under high background rate is the most important and urgent issue
- Simulation framework to overlap background hits with physics events has to be constructed

Tracking Efficiency

- Large number of background hits may cause tracking inefficiency: mis-identification of signal hit with background hit



For a normal incident track, the probability of mis-identification of hit is given by;

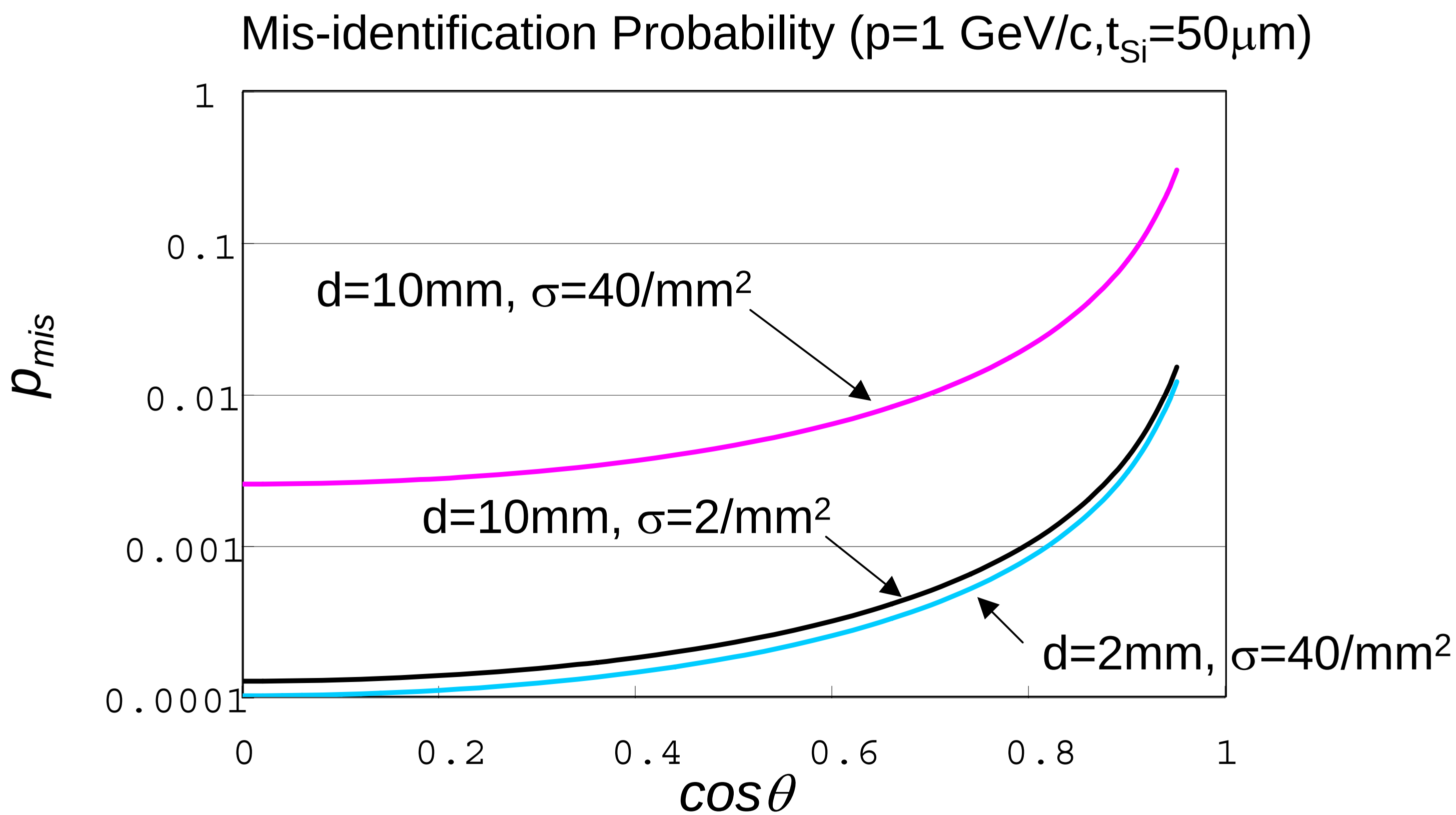
$$p_{mis} = 2\pi\sigma R_0{}^2, R_0 = d\theta_0$$

σ : Background hit density
θ_0 : Multiple scattering angle

Angular and momentum dependence;

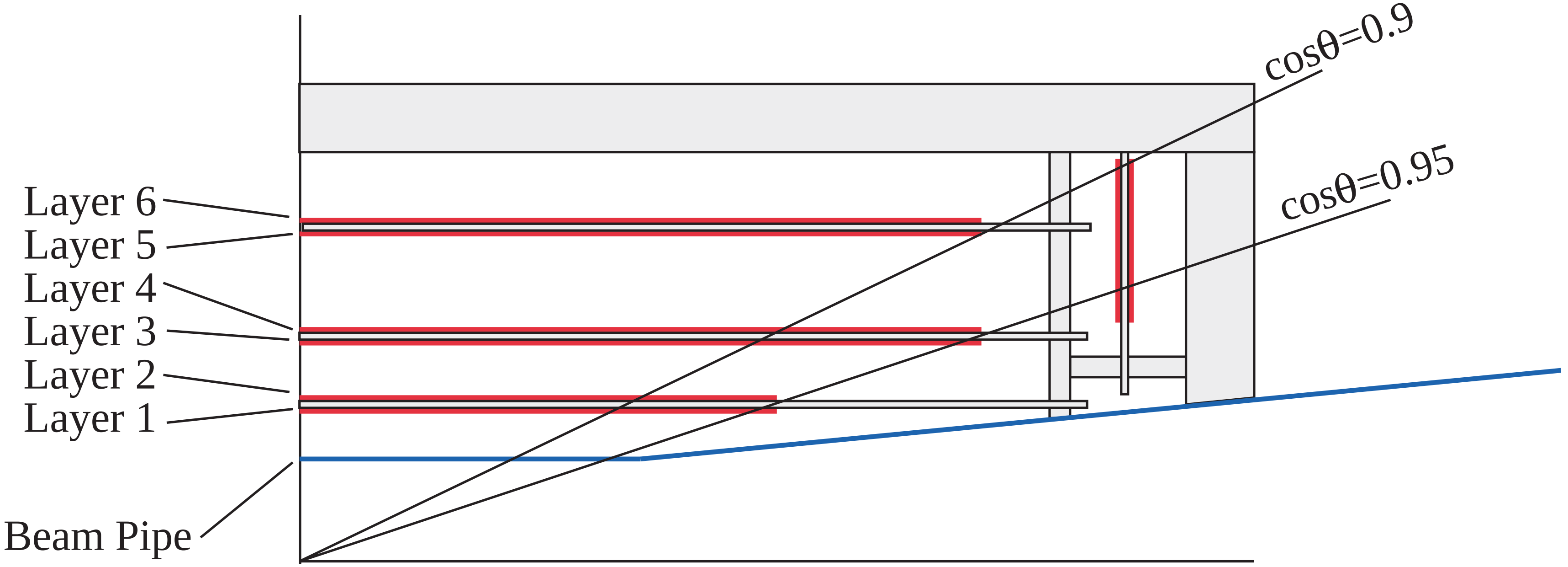
$$p_{mis} \propto p^{-2} \sin^{-4}\theta$$

Tracking efficiency



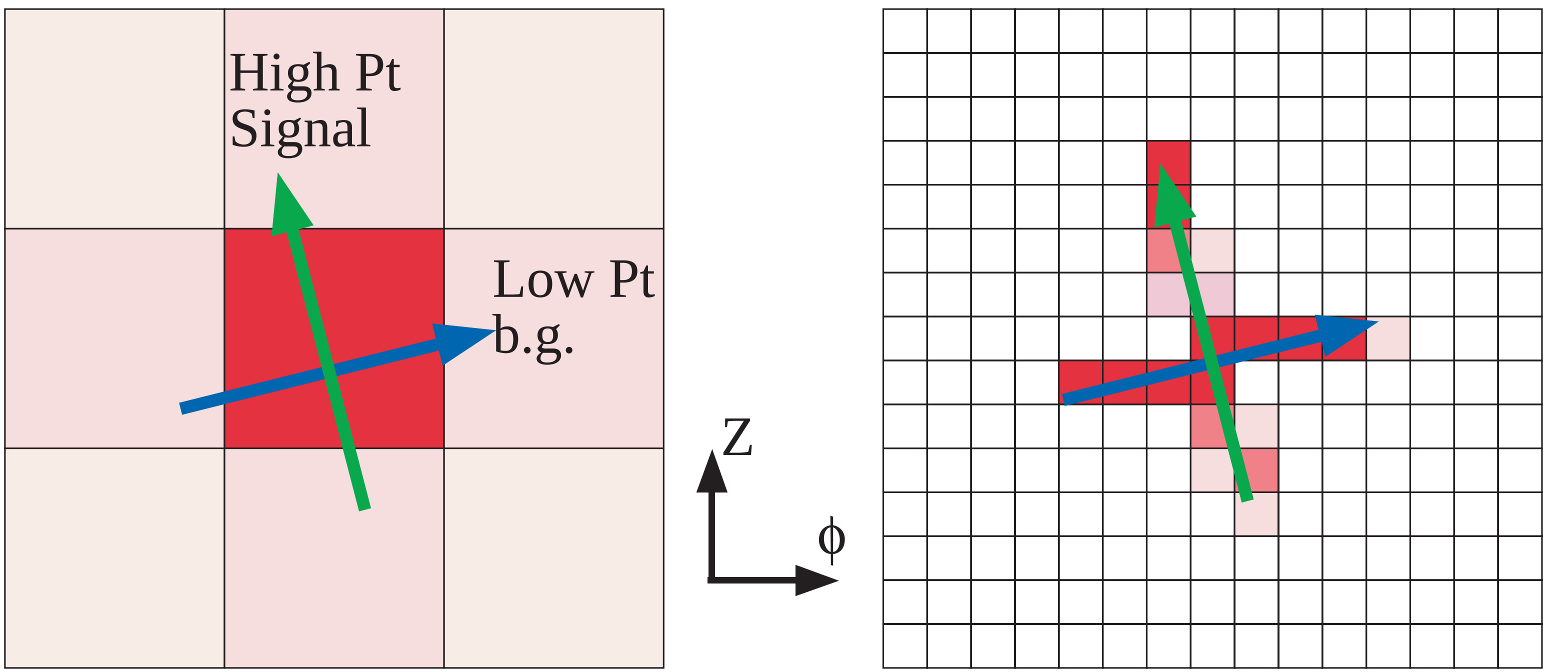
Tracking Efficiency

- Some ideas for b.g. rejection (1)
  - CCD doublet in proximity to reduce effect of M.S.



Tracking Efficiency

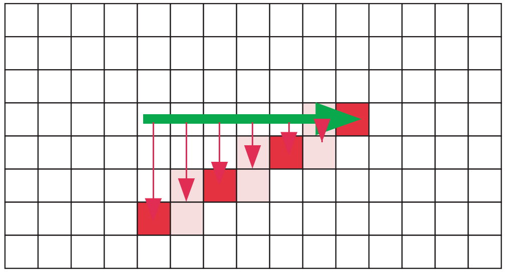
- Some ideas for b.g. rejection (2)
  - Hit cluster shape



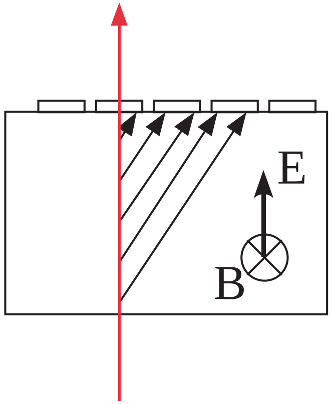
(tracking capability with single layer!)

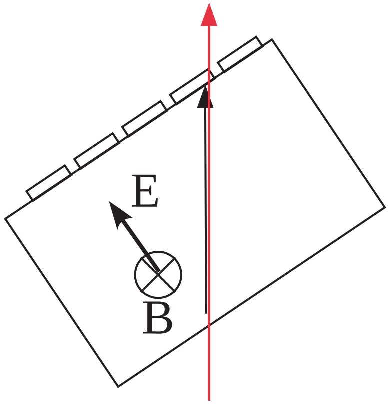
Lorentz Angle

- Lorentz angle in depleted-layer
  - $\tan\theta=\mu_n B$
    μ_n: electron mobility
  - Carrier velocity saturates at high E field:
    - μ_n =0.07 m^2/Vs
      @T=300K, E=1x10^4V/cm
    - μ_n =0.045 m^2/Vs
      @T=300K, E=2x10^4V/cm
  - Small angle can be cancelled by tilting the wafer
- May not be a serious problem
  - Number of hit pixels does not increase so much



	B=3T	B=5T
E=1x10^4V/cm	θ=12deg	θ=19deg
E=2x10^4V/cm	θ=7.7deg	θ=13deg





Study Issues of FPCCD

- Short term goal (by the “Detector outline document”)
  - Simulation study
    - Tracking efficiency
    - Physics implication (Flavor tagging)
  - Hardware study (depends on funding)
    - Charge spread in fully depleted CCDs
    - Lorentz angle in B field → Optimization of wafer tilt angle
    - Radiation hardness (difference in fully depleted CCD?)
  - Show that FPCCD works as a vertex detector “in principle”
- Mid term goal (by “CDR”)
  - Fabrication of prototype ladders
  - Test the prototypes and demonstrate the performance
- Long term goal (by “LOI”)
  - Engineering design of FPCCD Vertex Detector

Summary

- We propose FPCCD option for the ILC Vertex Detector
  - Fully depleted CCD with 5μm-square fine pixel size
  - Accumulate 2820 BX and readout between trains
  - Two layers make a doublet (super layer) to pick up signal hits out of background hits
- FPCCD seems the most feasible (least challenging) technology among the proposed options
- Tracking efficiency under beam background is the most critical issue for FPCCD. Simulation study is urgent.