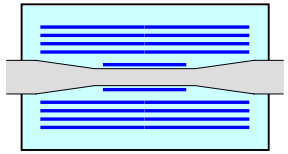


Detector R&D at the LCFI Collaboration

(Bristol U, Oxford U, Lancaster U, Liverpool U, RAL)

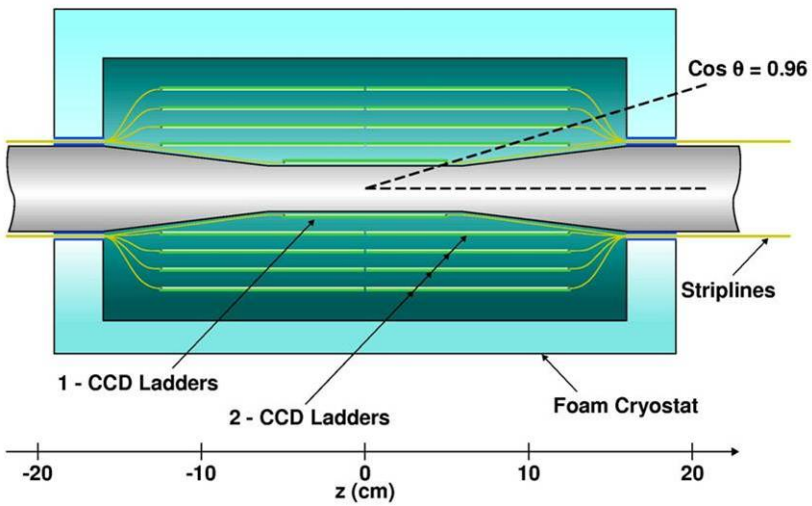
Konstantin Stefanov on behalf of the LCFI collaboration

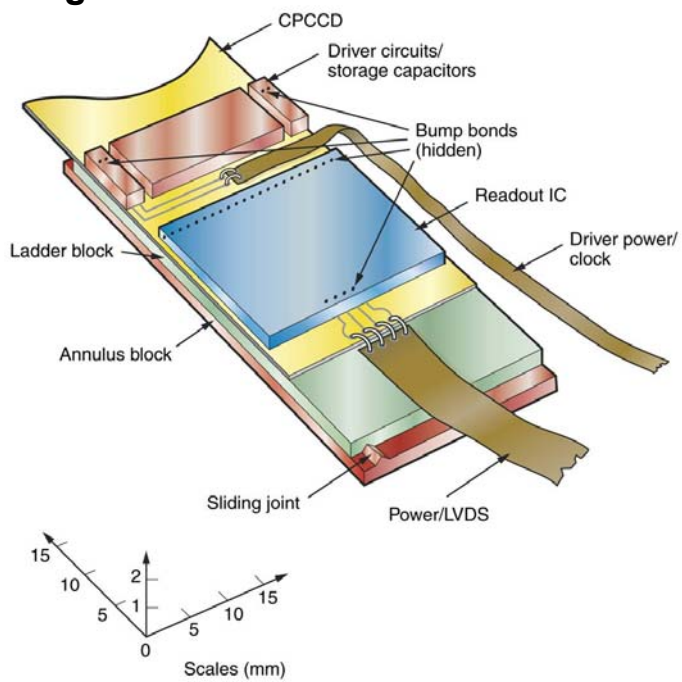
LCWS2005, Stanford, 18-22 March 2005

- Introduction
- Recent results
  - CPCCD work
  - ISIS work
- Future directions and summary

The Vertex Detector for ILC

- Excellent point resolution (3.5 μm), close to IP, good angular coverage
- Low material budget (<0.1% X_0 per layer), low power dissipation
- Readout:
  - Inner layer effectively read out at 50 μs intervals during the 1 ms pulse train (20 readouts) – information may leave the sensor or be stored in pixel
  - Outer layers read out at 250 μs intervals
- Moderate radiation hardness (≈20 krad/year)
- Tolerates Electro-Magnetic Interference (EMI) from RF leakage

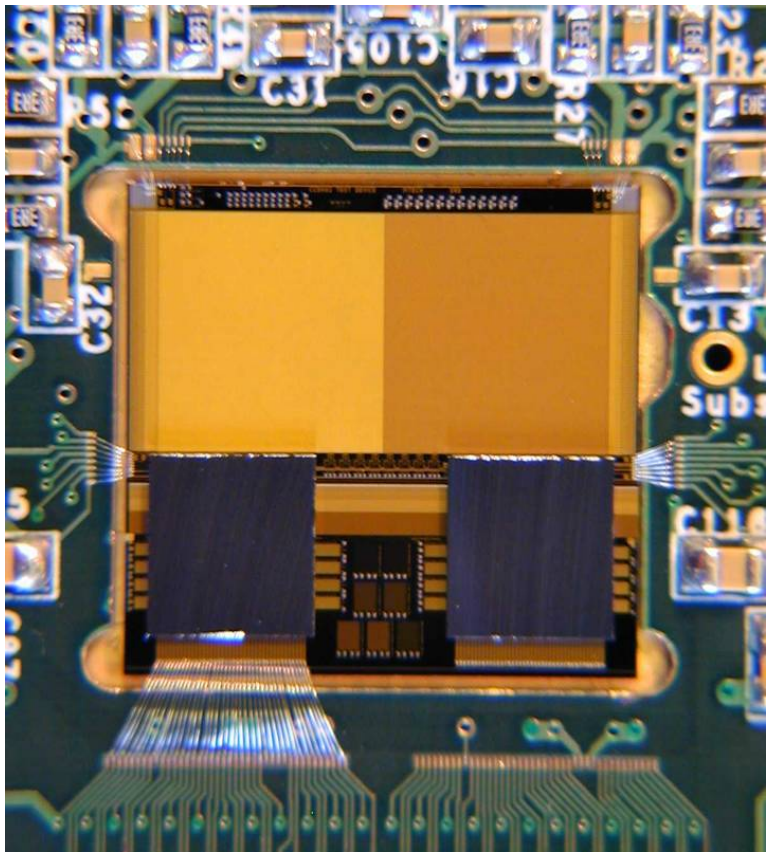




The Column-Parallel CCD

Main detector R&D at LCFI:

Hybrid assembly with Column-Parallel CCD (CPCCD) and CMOS ASIC

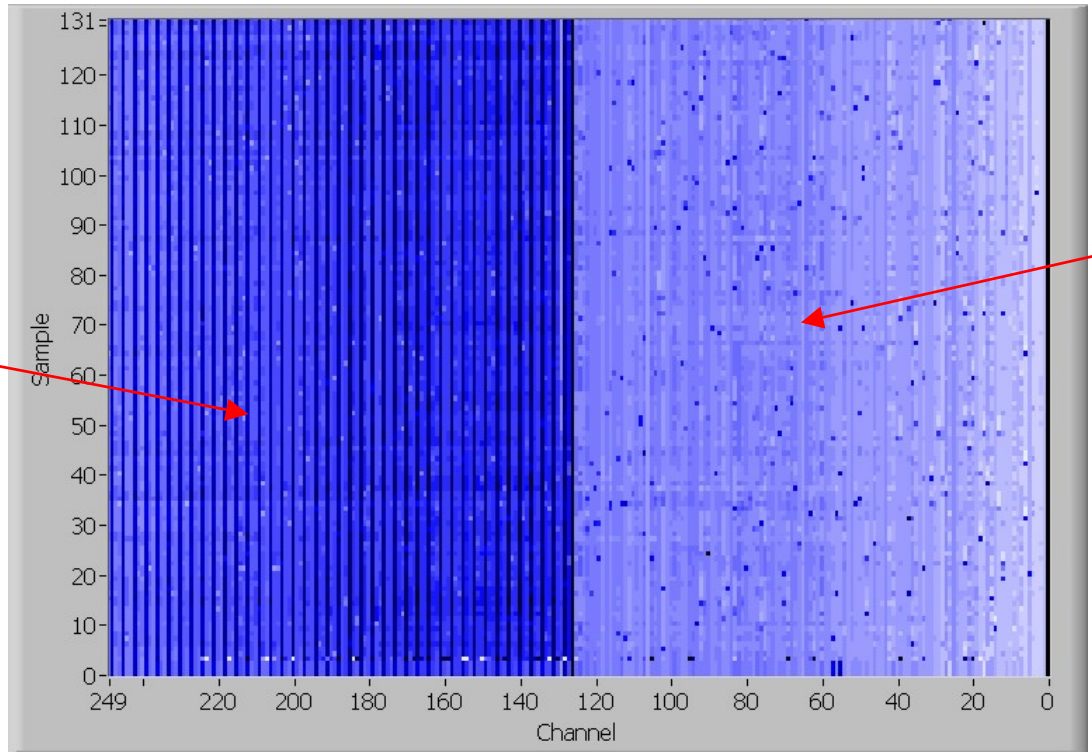


Bump-bonded CPC1/CPR1 in a test PCB

- First CPCCD (CPC1) manufactured by E2V:
  - 20 μm square pixels
  - 3 different outputs
- CMOS readout chip (CPR1) designed at RAL
- Bump-bonded by VTT (Finland)
- CPC1 clocked to 25 MHz stand-alone, metal-strapped gates for efficient clock propagation
- CPC1 optimised for low clock amplitude and low drive power – works with 1.9 Vpp clocks
- Readout chip has amplifiers, 5-bit ADCs and FIFO per column

Signals from CPC1+CPR1

5.9 keV X-ray hits, 1 MHz column-parallel readout



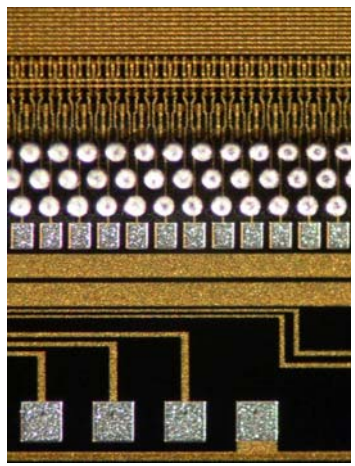
Charge outputs, inverting (positive signals)

Noise ≈100 e-

Voltage outputs, non-inverting (negative signals)

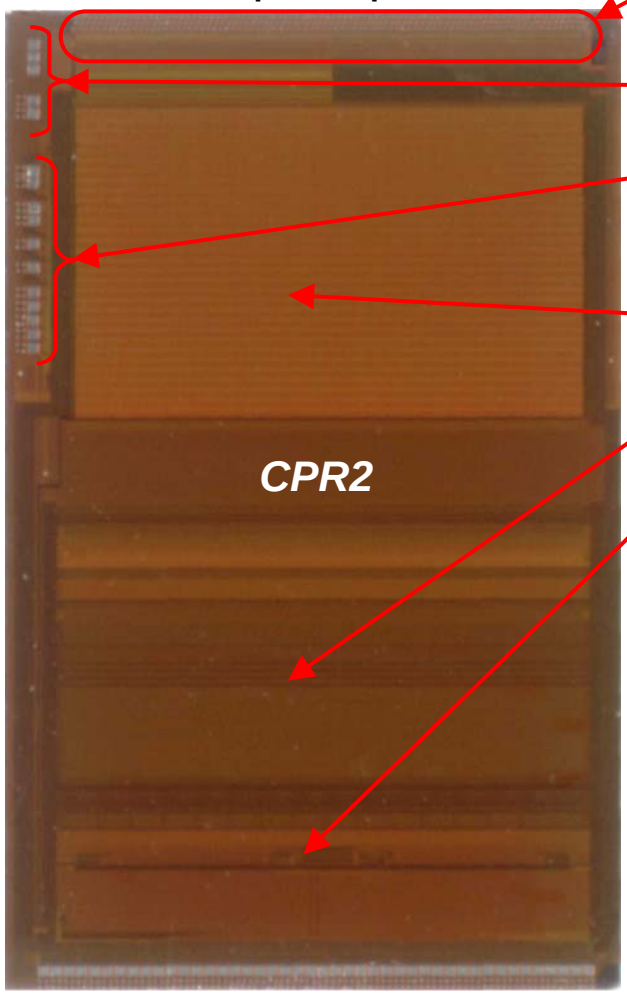
Noise ≈60 e-

- **First time E2V CCDs have been bump-bonded**
- **High quality bumps, but assembly yield only 30% - reason still unclear**
- **Differential non-linearity in ADCs (100 mV full scale) – addressed in CPR2**



Bump bonds on CPC1 under microscope

Readout Chips CPR1 and CPR2



Voltage and charge amplifiers, 125 channels each

Analogue test I/O

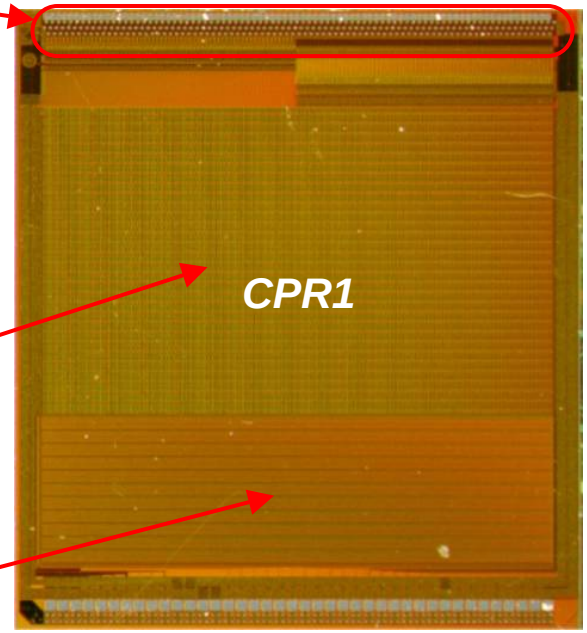
Digital test I/O

5-bit flash ADCs on 20 μm pitch

Cluster finding logic (2×2 kernel)

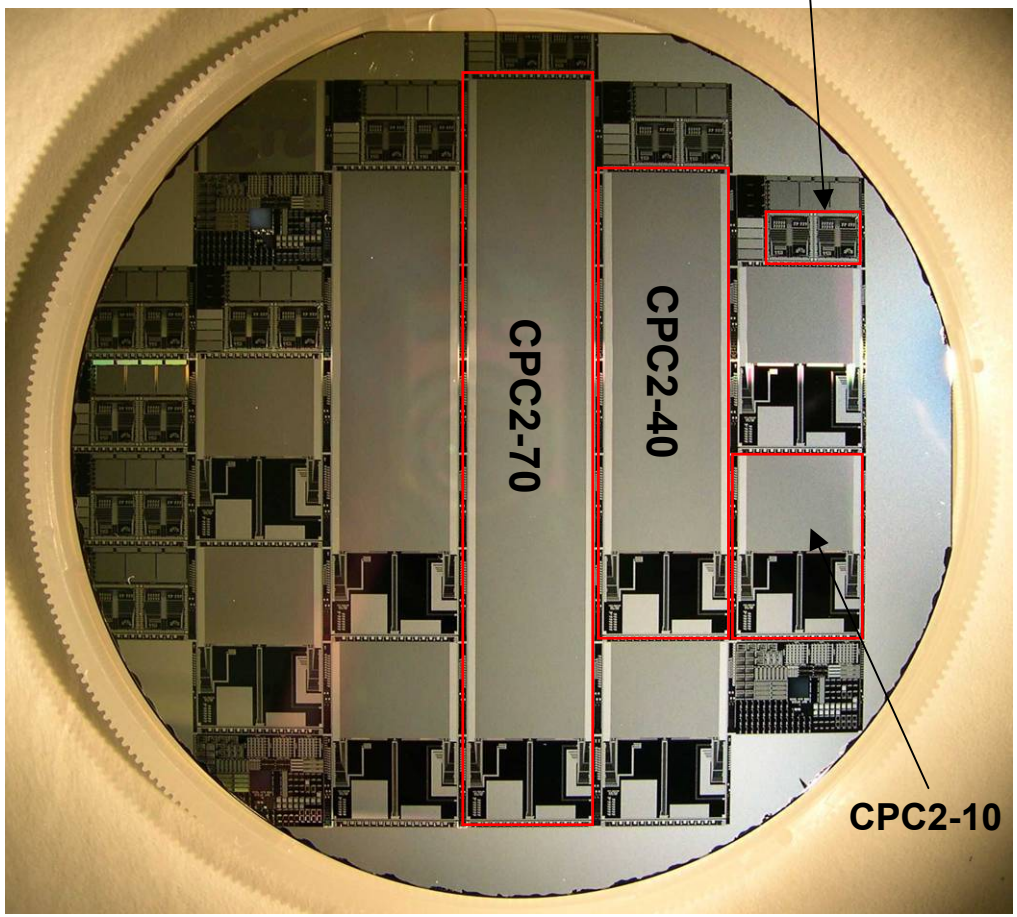
Sparse readout circuitry

FIFO



- CPR2 designed for CPC2
- Step forward from CPR1, lots of improvements
- Designed by the Microelectronics Group at RAL
- Size : 6 mm × 9.5 mm
- 0.25 μm CMOS process (IBM)
- Manufactured and delivered, fun is imminent

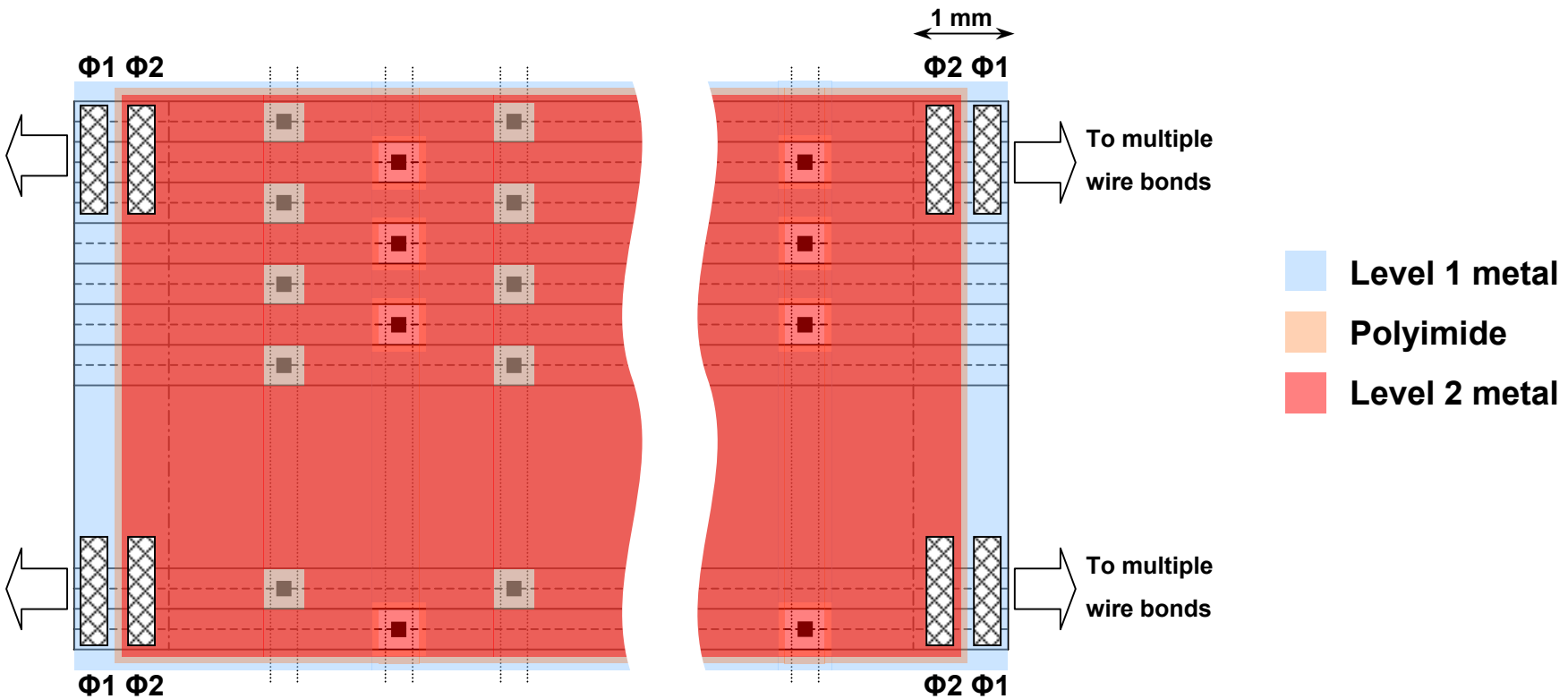
CPC2 / ISIS1 Wafer



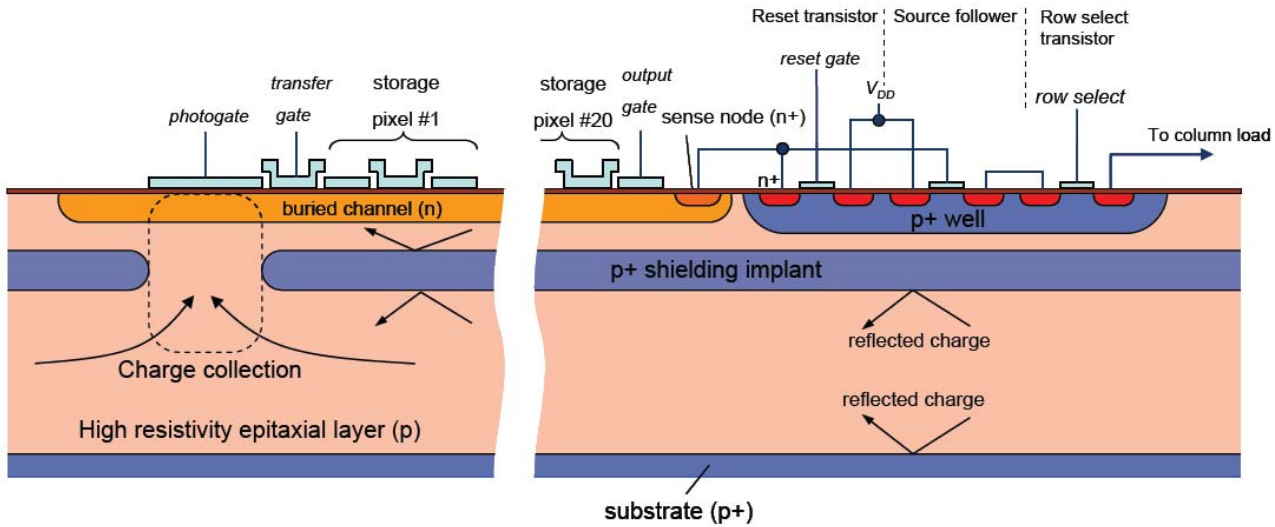
- Sufficient experience gained with CPC1 to move to CPC2
- CPC2 in manufacture, delivery by June 2005
- Three different chip sizes with common design:
  - CPC2-70 : 92 mm × 15 mm image area
  - CPC2-40 : 53 mm long
  - CPC2-10 : 13 mm long
- Compatible with CPR1 and CPR2
- Two charge transport sections
- Choice of epitaxial layers for different depletion depth: 100 Ω.cm (25 µm thick) and 1 kΩ.cm (50 µm thick)
- Baseline design allows few MHz operation for the largest size CPC2

CPC2 Drive

- CPC1 did not have optimal drive conditions due to single level metal
- Novel idea from LCFI for high-speed clock propagation: “busline-free” CCD:
  - The whole image area serves as a distributed busline
  - 50 MHz achievable with suitable driver in CPC2-10 and CPC2-40 (L1 device)
  - Transformer drive for CPC2, will evolve into dedicated driver chip



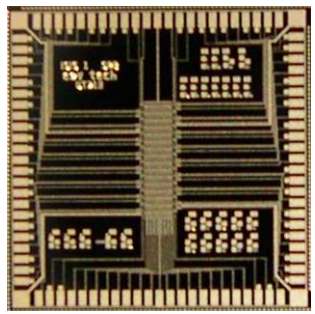
ISIS R&D



- RF pickup is a concern for all sensors converting charge into voltage during the bunch train;
- The In-situ Storage Image Sensor (ISIS) eliminates this source of EMI:
  - ❖ Charge collected under a photogate;
  - ❖ Charge is transferred to 20-pixel storage CCD in situ, 20 times during the 1 ms-long train;
  - ❖ Conversion to voltage and readout in the 200 ms-long quiet period after the train, RF pickup is avoided;
  - ❖ 1 MHz column-parallel readout is sufficient;

ISIS R&D

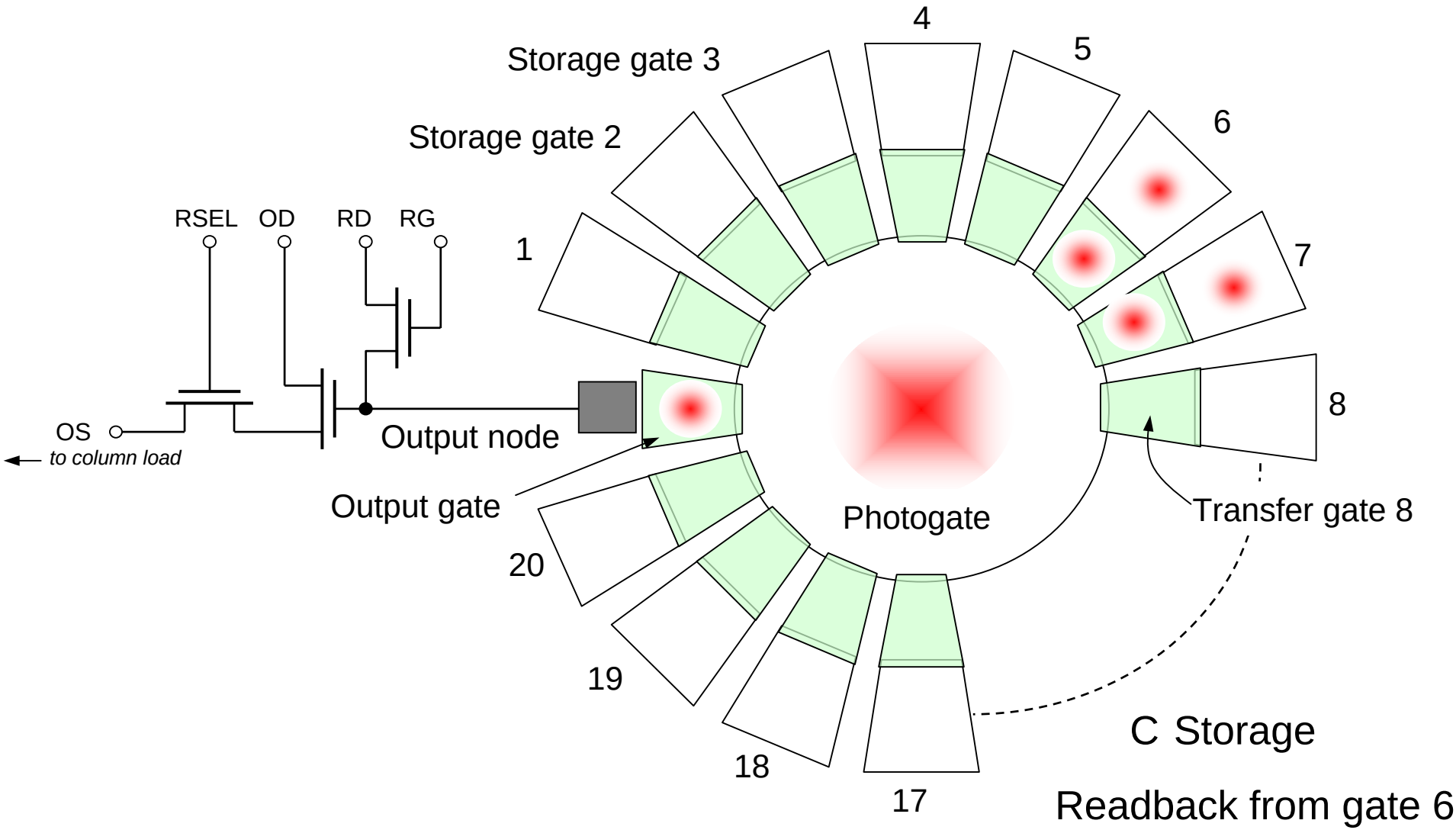
- Additional ISIS advantages:
  - ~100 times more radiation hard than normal CCDs – less charge transfers
  - Easier to drive because of the low clock frequency
- ISIS combines CCDs, active pixel transistors and edge electronics in one device: specialised process
- Development and design of ISIS is more ambitious goal than CPCCD



Edge logic for row selection and clock gating not shown

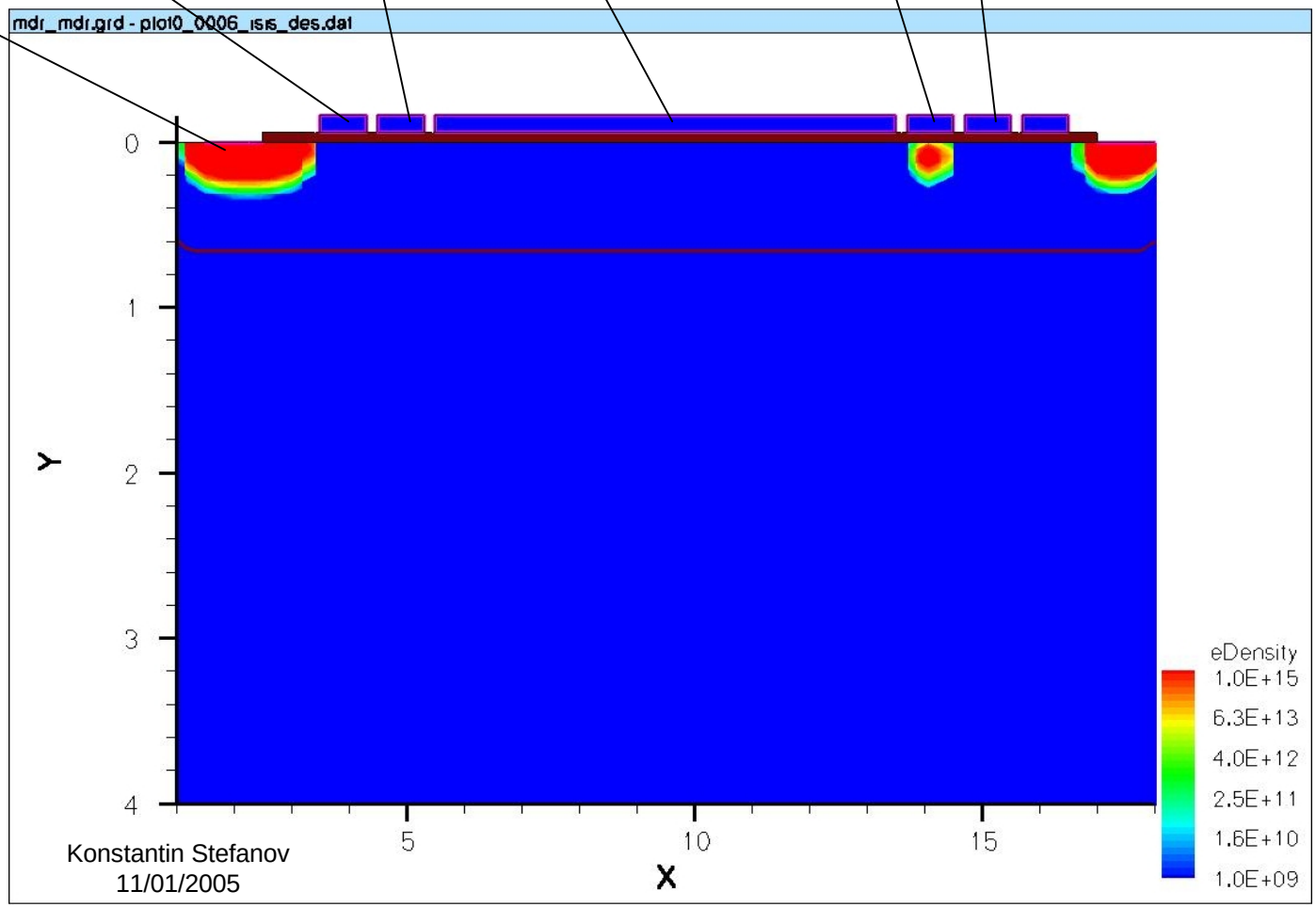
- "Proof of principle" device (ISIS1) designed by E2V:
- 16×16 array of ISIS cells with 5-pixel buried channel CCD storage register each;
- Cell pitch 40 μm × 160 μm, no edge logic (CCD process)

Revolver ISIS



Idea by D. Burt and R. Bell (E2V)

Revolver ISIS – Charge Transport



Time:

0 ns

25 ns

50 ns

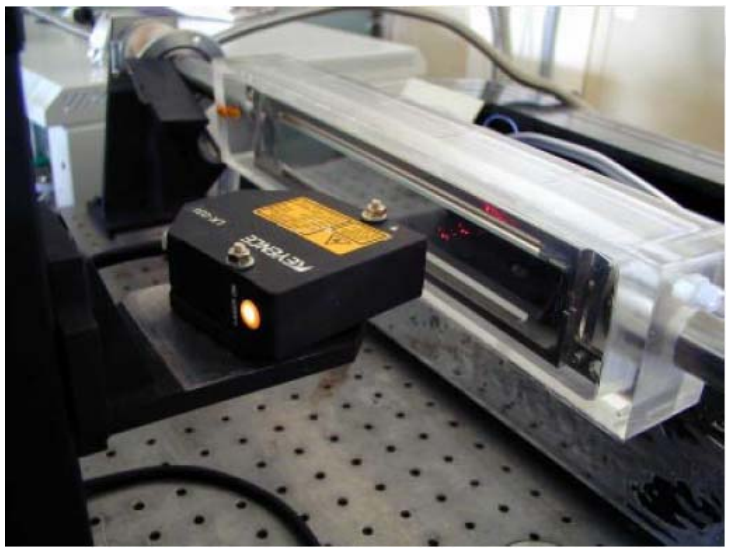
75 ns

100 ns

150 ns

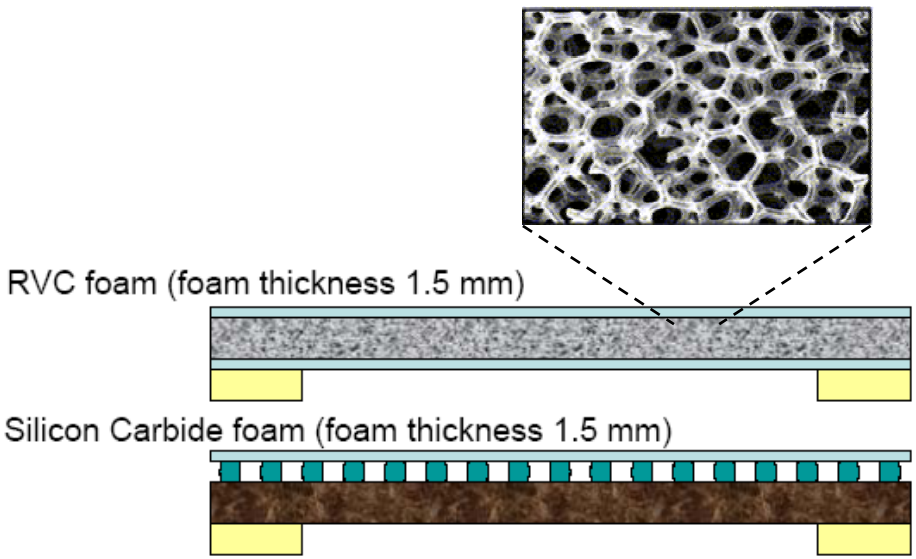
Thin Ladders: New Materials

30 μm unprocessed Si on 100 μm woven CF:

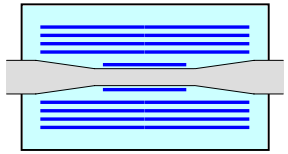


- **Reticulated Vitreous Carbon (RVC), 3% relative density : 3.1 mm = 0.05% X_0**
- **Silicon carbide foam, 8% relative density: 540 μm = 0.05% X_0**

(47 μm Si = 0.05% X_0)



Summary and Future Directions



- CPCCD program well advanced:
  - Hybrid assembly with CPCCD and CMOS chips works
  - Look into improvements to CPCCD – lower clock voltages and capacitance
  - Detector-like chips coming up soon
  - Mainstream work at LCFI
- ISIS work will be ramped up in the next 5-year proposal
  - First ISIS prototypes on CCD technology designed
  - Small pixel CMOS-based ISIS very promising and will be pursued

Immediate plans:

- Evaluate CPC2, CPR2 and ISIS1 till end of 2005
  - High speed external drive to CPC2-40 as demonstrator for the L1 vertex detector
  - LCFI already in a good position to contribute to the vertex detector at ILC and participate in its rich physics programme

Visit us at http://hepwww.rl.ac.uk/lcfi/