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Silicon Data Acquisition and Front-End Electronics

M. Dhellot, J-F. Genat, H. Lebbolo, T-H. Pham, and A. Savoy Navarro
LPNHE Paris, T33 RC 4, Place Jussieu, 75252 Paris, France

A highly integrated Front-End readout and Data Acquisition scheme for Silicon trackers is presented. In this context,a 16-channel readout chip for Silicon strips detector has been designed in 180nm CMOS technology, having in view a highly multiplexed and sparsified readout global strategy. First results are presented.

1. INTRODUCTION

A Front-end readout system for tracking Silicon detectors has to manage millions of channels. Actually, a Silicon strips envelope around the central tracker in the case of the LDC design would cover a few 100 square meters for a few millions channels to be read. This would also be true in the case of the SiD that in the present baseline design covers of the order of 100 square meters and a total of 6 millions channels. Therefore, the multiplexing of tasks such as analog to digital conversion and data sparsification are mandatory, and power cycling taking advantage of the ILC machine timing will be essential. The full context of this work is described in the document available from the Website: [1]

2. FRONT-END PROCESSING AND READOUT SCHEME

After the collisions stage, where analog data are stored in analog pipe-line buffers, digitization with zero suppression takes place, filling an on-chip buffer. In order to save power and buffer space at the front-end level, it is intended to store data only if a charge cluster exceeds a given threshold.

2.1. Front-end processing

The foreseen front-end processing is sketched in Figure 1. Silicon strips detectors of a capacitance between 10 and 100 pF with a maximum foreseen presently of 75 pF (60cm ladder). It is intended to get both the the amplitude on a strip and the hit coordinate along the strip by timing between the two ends of the detector, the performance of this timing process being presently under investigations.

During the collisions, the Front-end chips amplify, filter, buffer in analog pipe-lines and digitize the input charge. Actually, the occupancy of the detector dictating the analog buffers depth is foreseen of the order of a few per cent, mostly in the forward regions. In order to sparsify data at the readout stage, only charges collected on three adjacent strips, whose sum exceeds a given threshold, are stored and digitized. Digital processing for charge, time, cluster, and fast track algorithms is under study while designing the front-end electronics.

After amplification and pulse shaping, two analog samplers, one fast, one slow, with 10ns and 100ns scale clockings respectively, generate samples of the analog shaper output stored in two circular analog buffers of depth 16 running continuously. In order to store charge signals in the detector above a given threshold, an analog sum of three

[1] http://www.linearcollider.ca/lcws05/h/Savoy.pdf

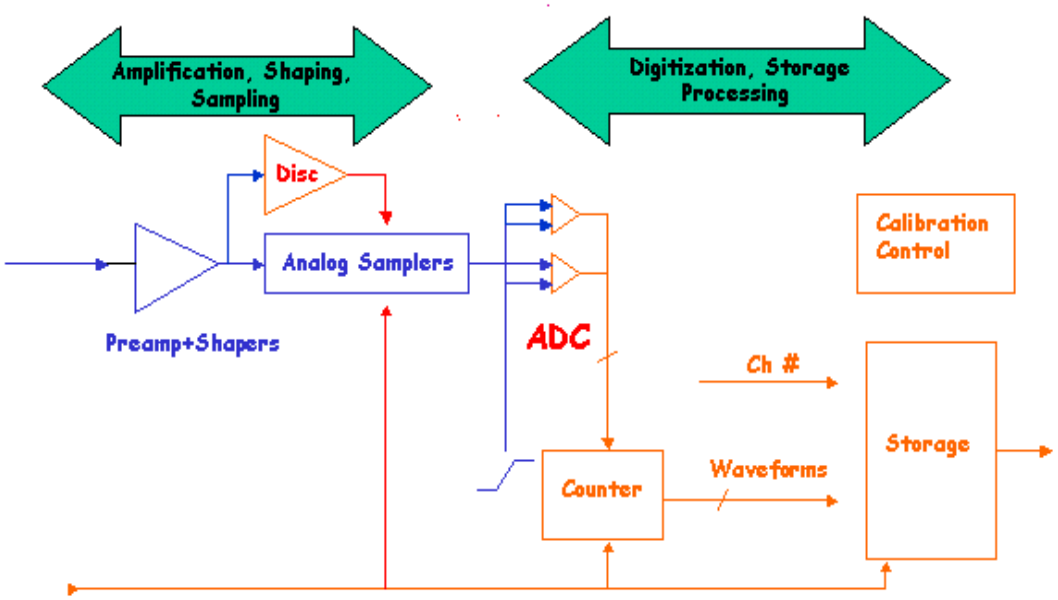

Figure 1: Front-End Processing

neighbouring channels is compared to a voltage level, taken at the output of the slow shapers, for each channel. A trigger decision at this level freezes the analog buffers, and selects an available set of two buffers for the next pulse to come. The total number of buffers for a given channel depends on the Silicon strips occupancy which is foreseen to be of the order of a few per cents. Therefore, a depth of 16 should cope with even worse detector output rate conditions.

This process runs for the total duration of an ILC train, of the order of one millisecond. At the end of the train, digitization takes place. In order to minimize the power, a single ramp ADC is foreseen, allowing to digitize in parallel as many channels as possible. The cost in power per channel is due to one comparator stage only. After digitization, data is pushed to an on-chip buffer structured as shown Figure 2.

3. TEST CHIP

A test chip has been designed in a 180 nm CMOS technology by United Microelectronics Corporation (Taiwan) available at multiproject cost through Europractice. It includes 16 channels comprising a low-noise preamplifier, a pulse shaper, a sample and hold, a voltage buffer and a comparator.

3.1. Low-noise analog section

The low-noise preamplifier is a folded cascode stage with a PMOS input transistor biased in moderate-weak inversion, the simulated noise from this stage being 85 + 16.5 e-/pF. The pulse shaper is an active CR-RC network using the same folded cascode structure as above, buffered with a source follower in order to drive the 600fF sample and hold capacitor. Two analog controls allow to tune the peaking time between one and five microseconds.

3.2. Sampling and comparator

The sample and hold is switched with a single NMOS transistor sized to trade off between rise-time, possible leaks, and the injected charge resulting in a voltage offset. A voltage buffer drives the comparator for which a trade-off

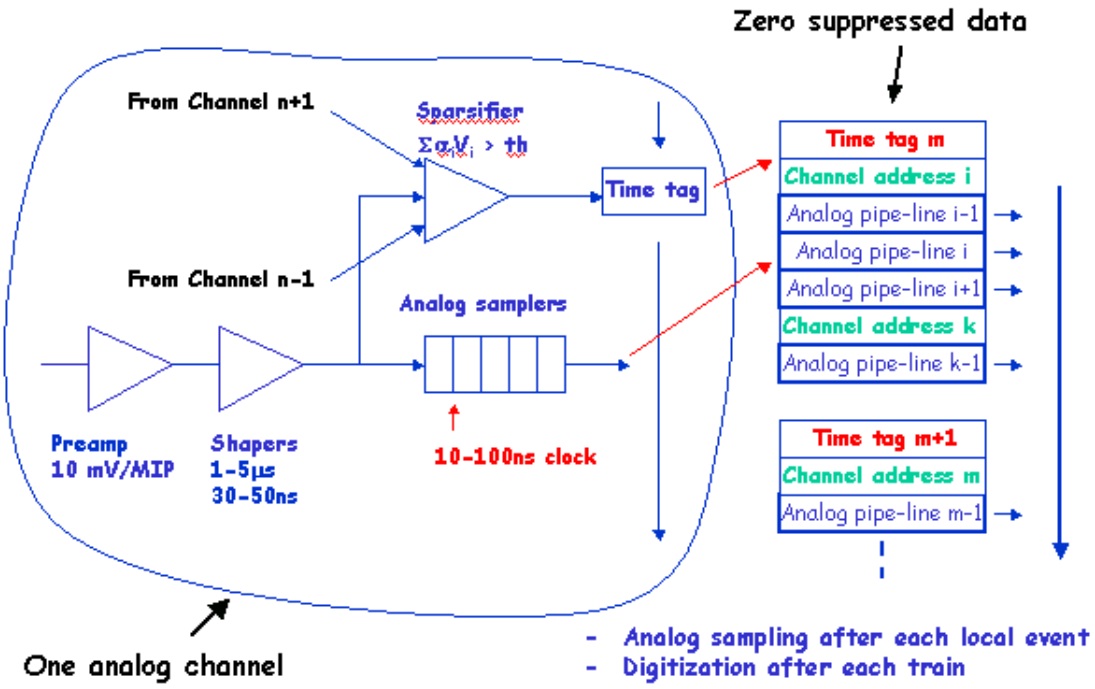

Figure 2: Data taking and data structure

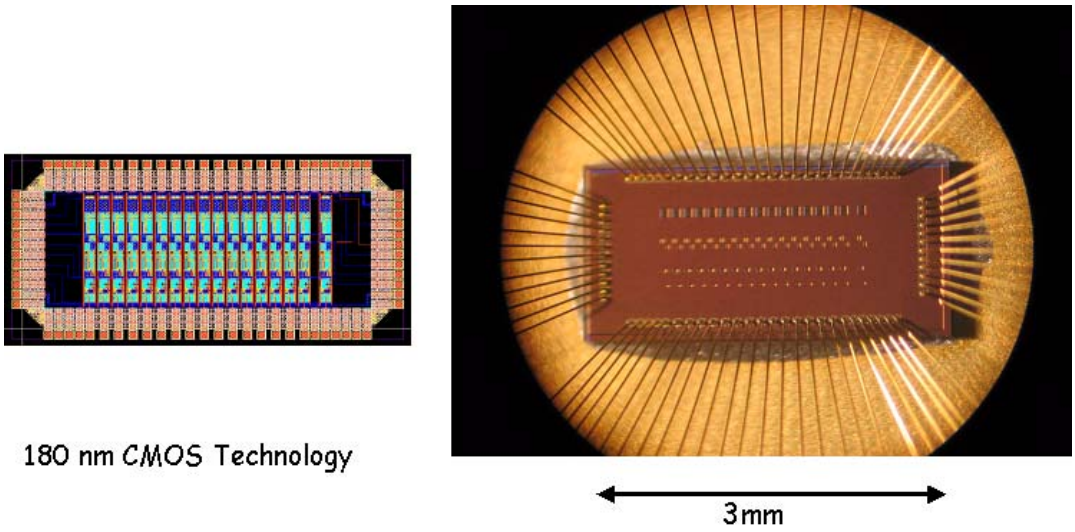

Figure 3: 180 nm CMOS Chip layout and picture

between power and accuracy has been set at 30μW per channel, regarding the foreseen 10-bit ADC precision.

4. TEST CHIP RESULTS

The layout and chip are shown Figure 3.

4.1. Noise

At 60μW input stage power, 50pF detector capacitance, 3μs shaping time, the various contributions to the detector and front-end electronics noise are summarized in Table 1.

Table I: Foreseen noise contributions at 50pF detector capacitance and 3μs shaping time

Noise source	**Value**	**Noise**
Input FET	g_m = 0.69mA/V	910e-
Detector leak	10nA	588e-
Bias resistor	10MΩ	423e-
Total		1163e-

The measured noise slope is 205 + 16.5 e-/pF. The discrepancy between the simulated noise floor at zero capacitance and the experimental result is under investigations.

4.2. Power

In order to take advantage of the ILC machine timing, all front-end stages running during the collisions only could be switched off for the readout stage. Therefore, a factor 100-200 can be saved at this level. This process has been simulated to be effective with the present front-end electronics provided the integration capacitor is reset before power-off and after power-on.

5. CONCLUSION

The integration of a front-end electronics for Silicon detectors in Deep Sub-Micron CMOS technology allows to implement a highly integrated front-end for the Silicon trackers that should not degrade the intrinsic detector resolution within an affordable power budget.

A future 128-channels version that will include fast and slow shapers, the sparsifier stage, analog samplers and a full ADC, digital section including possibly digital filtering and lossless data compression, power switching, is under design.