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Design Considerations for the Scintillator-strip ECAL Electronics

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We describe a local electronics system near detector proposed for Linear Collider Detector, especially for a calorimeter with scintillator as active material. The system works to read analog signal from photon sensors, digitizes, does zero suppression and transfers those data to the upper DAQ system.

1. INTRODUCTION

An electronics system will be discussed here supposing an Electro-magnetic calorimeter of scintillator strips as a detector. This detector would be called GLD-detector which is specified as to be largest among the detectors for the ILC discussed. In order to achieve Particle Flow to identify jets coming from source partons, the detector has to have a capability of recognition to separate neighboring showers or tracks in the calorimeter. The size being talked is about 1cm x 1cm in every layers. And each layer has to be read out independently. Scintillator strip layer of X direction, absorber, Y-strips, absorber, tile layer and absorber will be a set of stacks which is shown in figure 1. There are 13 stacks (or super layer) in the EM-CAL. In each strip or tile, a wave length shifting fiber is embedded where scintillation lights made by passing charged tracks are absorbed and reemitted lights. At the end of each WLS fiber, one can read out number of photons from scintillation lights, where we put a photon sensor. The photon sensor is supposed to be made of silicon photon detector of multi-pixles, such as Sicon Photomultiplier (SiPM) or MPC (Multi pixel Photon Counter). One of the test results is shown in figure 2, which shows a pulse height distribution by an LED light at very small amount of light. The most left peak is a pedestal, the next one at right side is a peak corresponding to a pixel hitting by a photon and so on. We can count up to about 5 or 6 pixels which corresponds 5-6 photons in a sensor.

This indicates several million channels of analog read out and digitization. Here we discuss at a very basic point to construct such system.

2. REQUIREMENTS

Fist of all requirements from accelerator is the beam collision timings. We have 2820 bunches every 377ns in 1 micro-sec, so that we will have 200ms of data transfer time when we have no bunches. We supposer 1 Gbps of data transfer capability as a normal ethernet speed. In a train which happens every 200ms, we can transfer data of 20 MB.

We assume 4 bytes length in a hit including address and analog-to-digital converted data and 1000 channels have hits in a event which happens in a bunch. This means 4 byte x 1000 ch x 2820 bunch = 11.2 MB/s . This value is twice or more bigger than the data transfer rate we supposed at this moment. The requirement is fulfilled.

Since the photon sensor is made up with pixels of many small Geiger mode devices, random hits dominate in the background data. Suppose the rate of random hits is 1 MHz, this is a reasonable number from our experience, contribution in background is negligible, since the number of random coincidence is controled to be small enough when the signal window of the event timing is narrow.

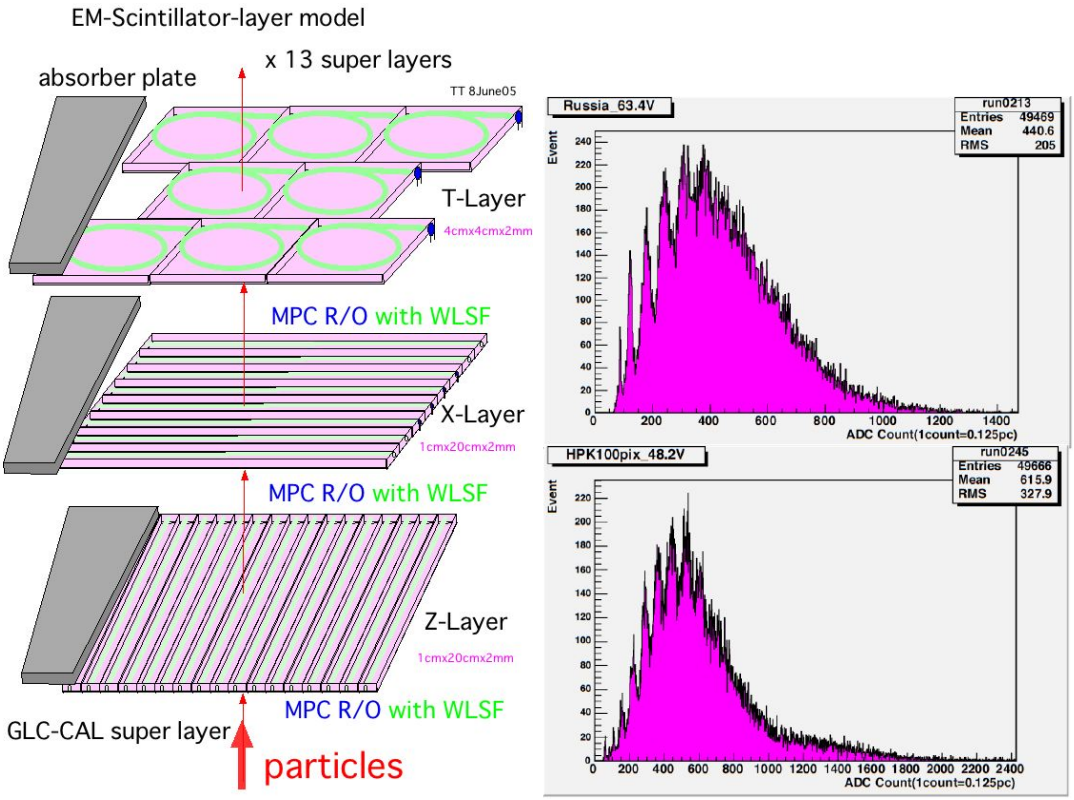

Figure 1: Left : A super layer of scintillator strip EM-CAL for GLD, Right : Pulse height distribution of a SiPM which can count number of photons as peaks.

There is another requirement of the power consumption, since the electronics sits very close to the detector and the photon sensors. The power loss in the power cable must be kept to be small.

The channel density in the detector is about 1mm / channel. Since the photon sensors are aligned every 1cm, however, summing up to 10 rows makes this density. This value is almost equivalent to the wiring to any chips.

The dynamic range required in the photon sensor is about 100, taking into account about 10 ADC count for a MIP (Minimum Interacting Particle) causes about 1000. This is achieved with 10 bit ADC. We need at least 10 bit ADC's.

We have to take into account the capability of gain controlling system in the electronics, which may need to adjusting bias voltage of photon sensor around 0.1V.

3. OVERVIEW OF THE ELECTRONICS

We propose here a read out electronics which transfer data during the bunch train gap, so that this satisfy the requirement. Analog to digital conversion consists of synchronous current integration for Q to V conversion type (SQV) circuit. This set the timing width minimum so that the random noise effect make minimum. The chip contains SQV and zero suppression mechanism. Thus the read out data size will be suppressed to fit the requirement. The data transfer will be carried out though an optical links. This makes the grounding problem minimum. The ethernet type data transferring will be employed to use commercial technology available. This makes the construction easier and cheaper.

A block diagram in figure 3 shows an realization of above scheme. The electronics circuit is compacted in the FE board in figure 3.

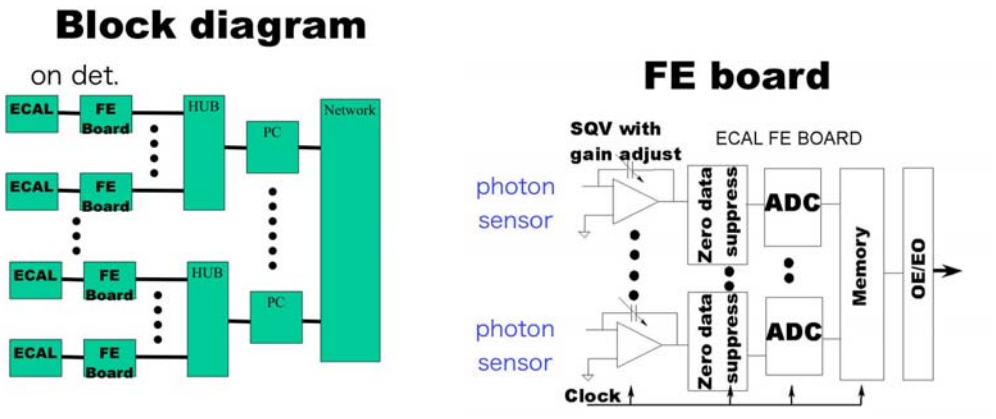

Figure 2: Left : over all read out schme with a block diagram , Right : FrontEnd electronics part in detail.

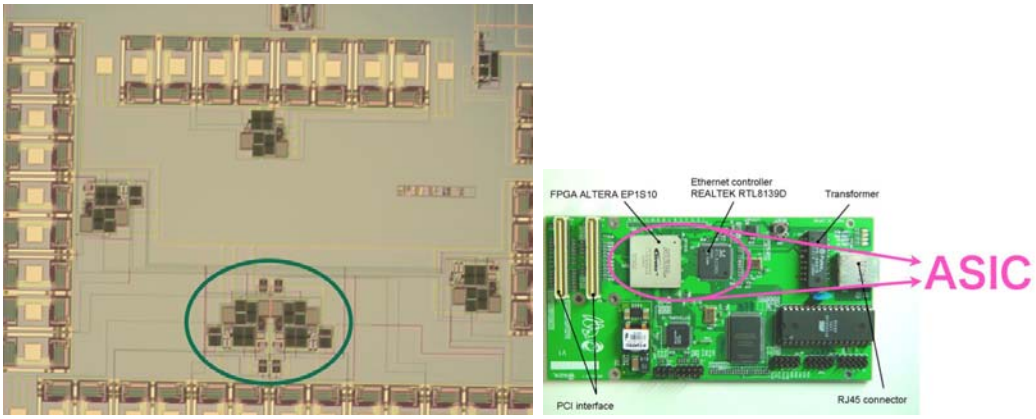

Figure 3: Left : a picture of a sample ADC-ASIC, Right : Ethernet type read out board which will be packed into an ASIC.

Look into the FE board, SVQ, zero suppression circuit, ADC, buffer memory and interface are aligned in figure 4.

4. R/D OF ELECTRONICS

In figure 5, one of the under developing SVQ is shown. There SVQ is in a circle and other buffer circuit are shown as well. One can find enough space in this TEG, where we can install zero suppression circuit and others.

In figure 6, a prototype ethernet data transfer board is shown. We will produce a ASIC chip as a net chip. This ASIC will be combined into our read out scheme.

5. SUMMARY

We have shown an read out electronics example for the Linear Collider detector, especially for the EM-Calorimeter. The electronics will meet the requirements where timing and data aquisition rate are taken into account. We are developing those circuits and ASICS. They will be realized as chips and boards.