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Front-end Electronic for the Calice ECAL Physics Prototype

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A 18-channel low-noise front-end chip has been designed and produced to read out the 1cm² silicon PIN diodes of the CALICE W-Si physics prototype calorimeter. Each channel includes a multi-gain low noise charge preamplifier followed by a bi-gain shaper and a track and hold device. A single output allows reading out every channel at 5 MHz through a multiplexer. Voltage swing is 2.5V with a 5‰ non-linearity. The measured dynamic range on a fixed gain is larger than 13 bits. The gain of the preamplifier can be tuned from 0.3V/pC to 5V/pC with 4 bits. The shaping is done by two fixed-gain shapers (gain 1 and gain 10). Output measured noise is 3000 e- with a detector capacitance of 100pF and a MIP around 42000 e-. Crosstalk is around 1‰. 1000 chips have been produced to equip the physics prototype.

Several version of PCB have been designed, taking into account the thickness constraint. A first version with the front-end chip outside the detector has been produced and has been running since January 2005 at DESY, exhibiting an overall MIP/noise ratio of 9. A new thinner version embedding the chip inside the calorimeter has been prototyped and is ready to go in test beam.

1. INTRODUCTION

The future linear collider will need a very high granularity electromagnetic calorimeter to achieve particle flow reconstruction[1]. That calorimeter will then have a huge number of channels – around 32 million - with typical calorimeter accuracy – around 15 bit. These specifications make the front-end electronic expectations outreach many actual specifications such as consumption or integration.

An interesting calorimeter design is a Tungsten-silicon sampling calorimeter. Active layers are 1 by 1 centimeter silicon PIN diodes. That architecture ensures a very high granularity as a pad is smaller than the moliere radius. A physics prototype has been designed to validate the concept and sharpen physics modeling. Dimensions of that prototype are 30 cm by 30 cm over 30 layers with 10,000 channels[2].

Figure 1 – Picture of the physics prototype in DESY (©Marc Anduze)

[1] J-C. Brient, These proceedings
[2] J-C. Vanel, these proceedings

A front-end chip has been designed to read out the 36-PIN-diode wafers which compose the detector. An 18-channel-chip solution has been retained thus 2 chips are needed to read out one wafer.

This paper will describe that chip called FLC_PHY3 which stands for FLC PHYsic prototype version 3. Measurements will be shown and the general architecture of the chip will be explained.

In parallel of the physics prototype construction has begun a technological R&D program to achieve the final detector expectations.

2. PHYSICS CONTEXT

That chip has been designed by the LAL microelectronic group for the CALICE collaboration which has chosen to split the R&D of the Si-W calorimeter in two directions:

- A physics prototype in a very short term to validate the concept of the detector. That prototype does not need to achieve all expectations of the TESLA TDR but as to be as close as possible of what might be the final detector.

- A technological prototype in a middle term to validate the technology chosen to achieve the performance of the final detector.

FLC_PHY3 has been designed in a very tight schedule for the physics prototype test beams beginning in December 2004 in DESY and going on in higher energy beam in 2005-2006.

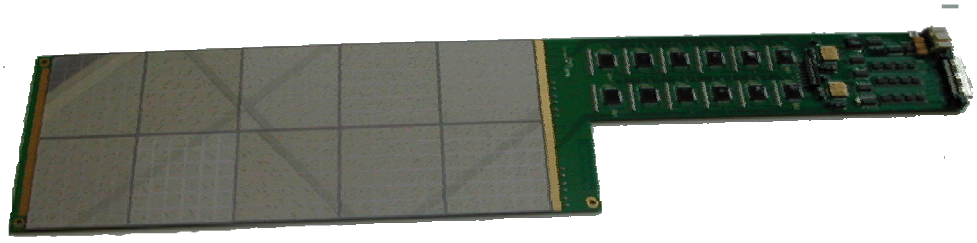

Figure 2 - Picture of the front-end board embedding FLC_PHY3 chips and silicon wafer matrices

3. CHIP DESCRIPTION

3.1. General description

The FLC_PHY3 Front-end chip is an 18-channel charge input front end circuit. It provides a shaped signal proportional to the input charge. Each channel is made of a variable-gain charge preamplifier followed by two parallel shaping filter of different gain (1 and 10) using a CRRC structure. Each of these shaper are followed by a track & hold device driving a single multiplexed output. The bias of each stage is common for every channel.

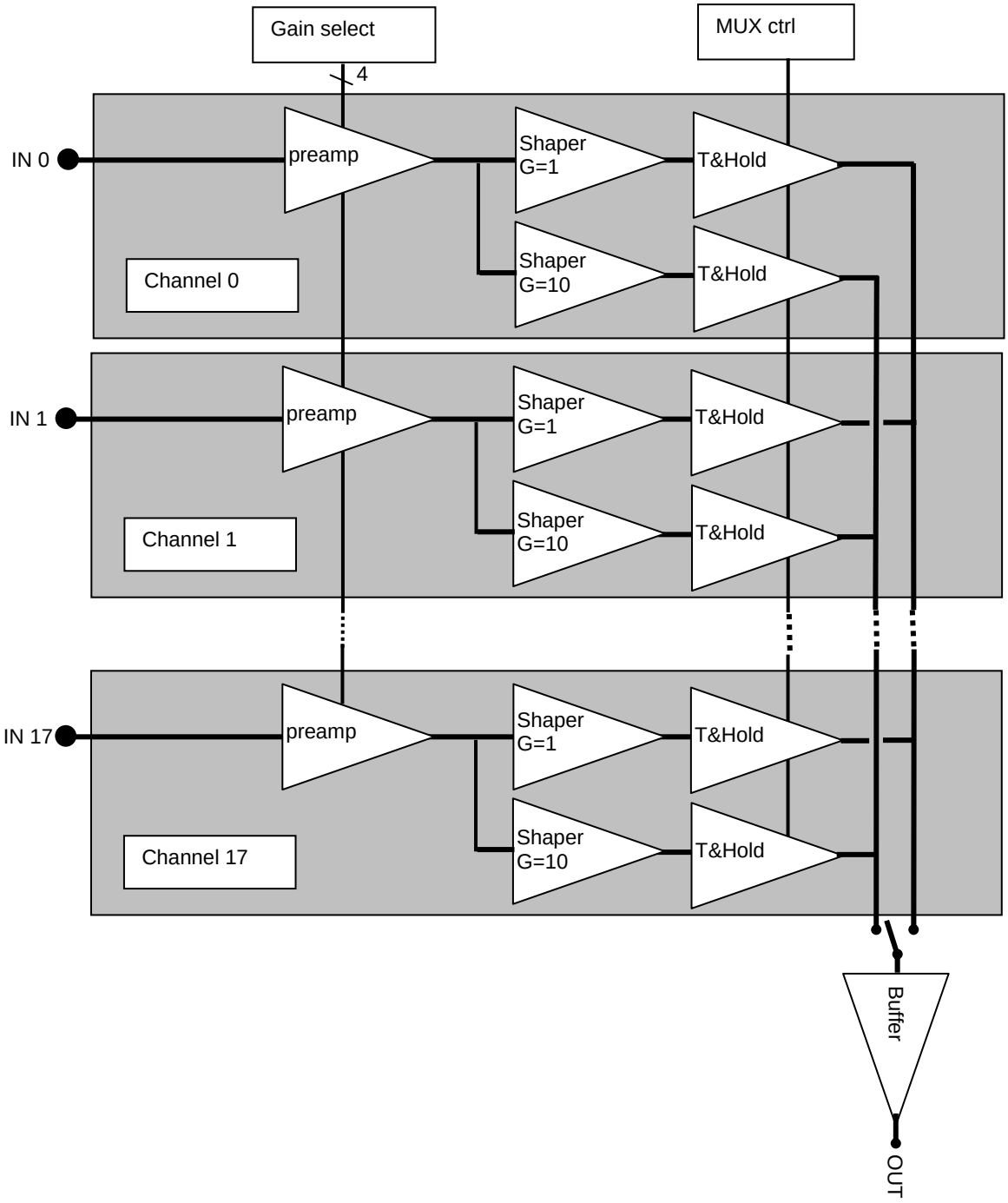

Figure 3 - General block scheme of FLC_PHY3

3.2. One channel description

The chip architecture is built around a low noise variable gain charge preamplifier followed by a by-gain CRRC shaper, a Track and Hold and an output multiplexer. The chip houses 18 channels, matched to a half detector wafer and is realized in 0.8 µm AMS BiCMOS technology. 1000 circuits have been produced at the end of 2003 and are packaged in TQFP64.

The charge preamplifier is a classical folded cascode architecture with a 3000/0.8 input PMOS which exhibits a transconductance of 8mA/V and a noise spectral density of 1.6 nV/√Hz at ID=0.9 mA drain current. The DC feedback is realized with a 36 kΩ resistor multiplied by 625 by a set of current mirrors, achieving an effective feedback resistance of 22 MΩ, while keeping good linearity. The "gain" (feedback capacitance) can be varied from 0.2 pF to 3 pF in 4 bits, the rise time can also be tuned by changing the dominant pole capacitance by a similar ratio.

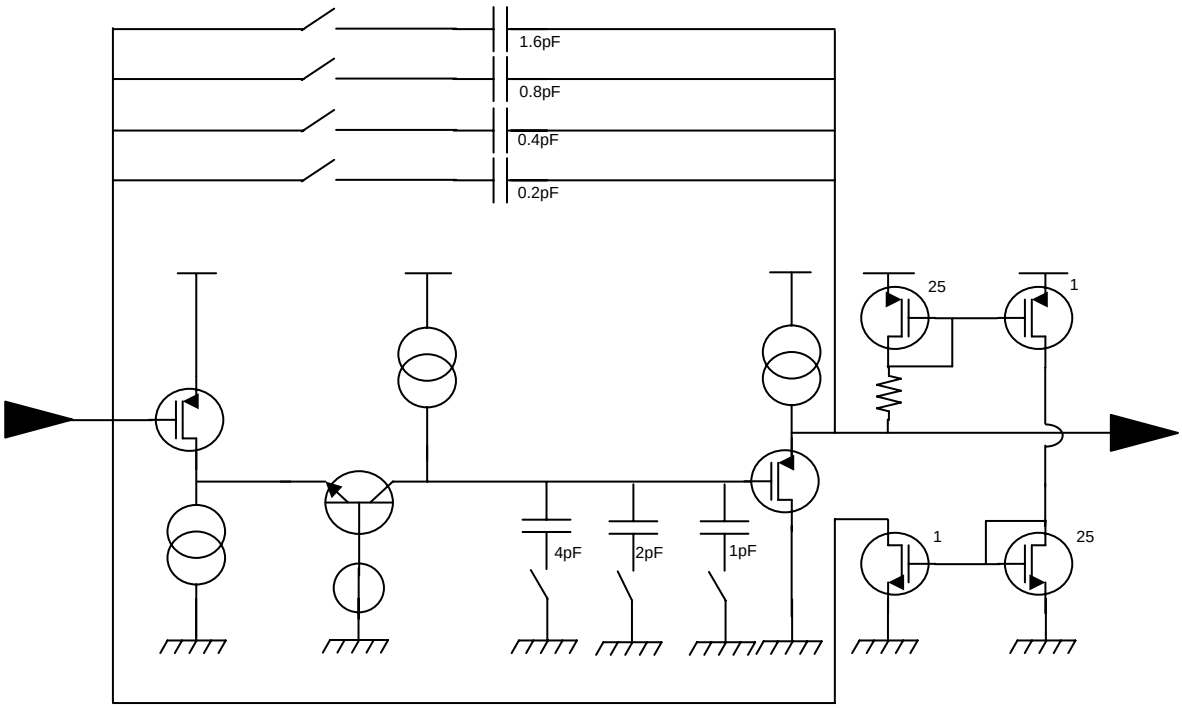

Figure 4 - Charge preamp scheme

The following stages are taken from a previous ASIC (OPERA_ROC) developed for the multi-anode PMT of the OPERA experiment3. The shaper uses a differential configuration in order to reduce the pedestal dispersion at the output and is built around a CRRC architecture with a peaking time of 200 ns. The track and hold is a simple 1 pF capacitor and a CMOS switch followed by a Widlar differential buffer for low offset, it is read-out sequentially by an OTA in follower configuration.

3 A. Lucotte et al *Nucl. Instr & Meth*. A521 378-392 (2004)

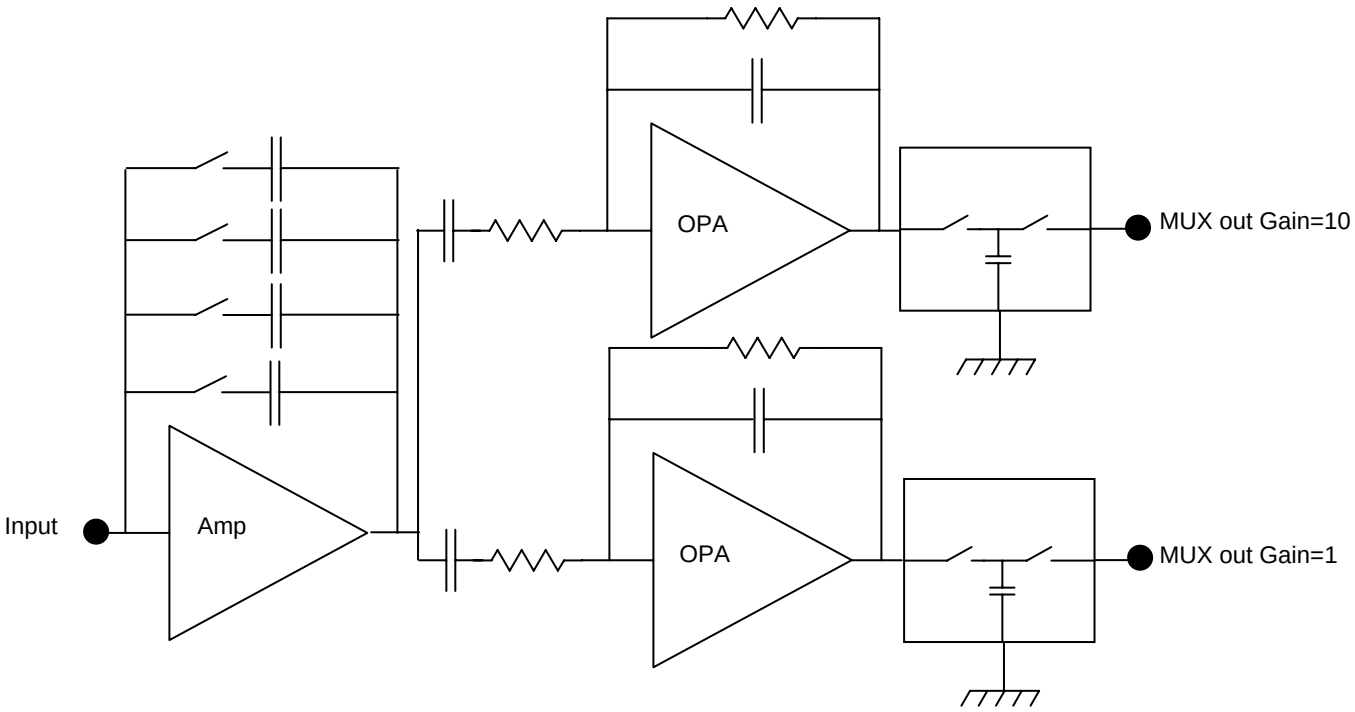

Figure 5 - Block scheme of one channel

4. MEASURED PERFORMANCE

4.1. Preamplifier

The output waveforms for the various gain settings are shown in Figure 6. The gain can be varied with 4 bits on a range of 16 while keeping the signal shape very constant. The linearity of the gain adjustment is better than 1%, with a “slope” of 1.65 V/pC and an “offset” of 25 fF.

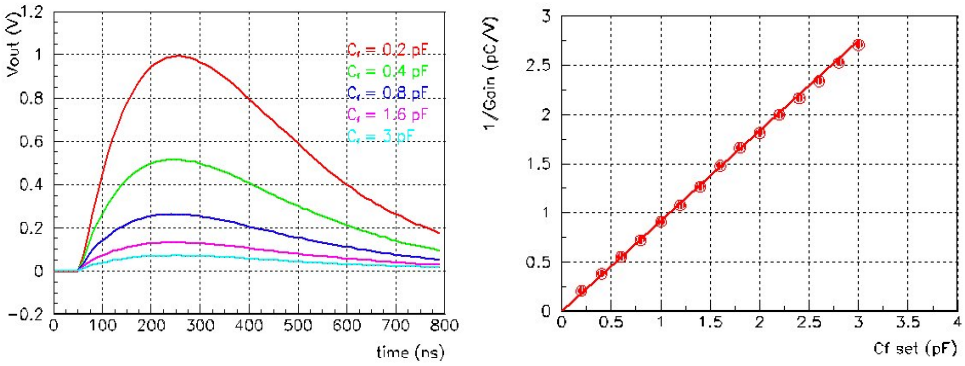

Figure 6 - Ouptut shape vs Cf set & 1/gain vs Cf set

The noise of the preamplifier alone has been measured via a dedicated "test output" followed by a variable CRRC2 shaper4. It follows nicely the fitted curve with series noise and 1/f noise. By varying the detector capacitance, the noise spectral density and the input capacitance can be extracted, yielding en=1.6 nV/√Hz and Ca=25 pF from which the test board accounts for 2/3. At tp=150 ns, the equivalent noise charge is measured as ENC = 1000 + 30 e-/pF. Thus with a detector capacitance of 70 pF (25 pF for the Si diode and 50 pF for the PCB line) the total noise is expected to be around 3500e- < 1/10 MIP. The preamplifier maximum output voltage is 3 V, corresponding to 600 MIPS with a feedback capacitance of 1.6 pF. All further plots below are shown with Cf=1.6 pF.

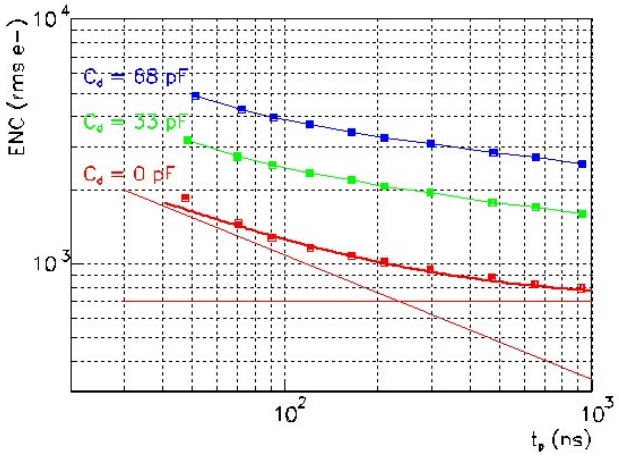

Figure 7 – Equivalent noise charge vs shaper peaking time

4.2. Shaper

The shaper is splitted in two gains 1 and 10, although mostly the gain 1 will be read out. The gain 10 is provided to possibly enhance the dynamic range and accommodate other detectors. Gains are given for a preamp feedback of 1.6 pF.

The gain 1 gives a signal of 696 mV/pC (5 mV/MIP) with a uniformity of 3% rms, the peaking time is 189 ns with a rms of 2 ns. The pedestals exhibit a dispersion of 4.8 mV rms with an excellent stability thanks to the differential architecture.

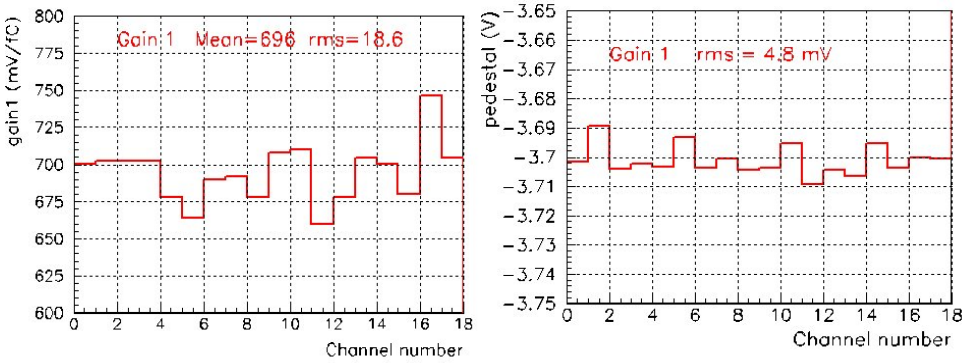

Figure 8- Gain uniformity (left) and pedestal uniformity (right) vs channel number (gain 1)

[4] C. de La Taille *Nucl. Phys B.* **B32**, 449 (1993)

The gain 10 gives a signal of 6294 mV/pC (45mV/MIP) with a uniformity of 3% rms, the peaking time is 174 ns with a rms of 2 ns. The pedestals exhibit a dispersion of 8.3 mV rms. In both gains, the crosstalk is smaller than 0.2%.

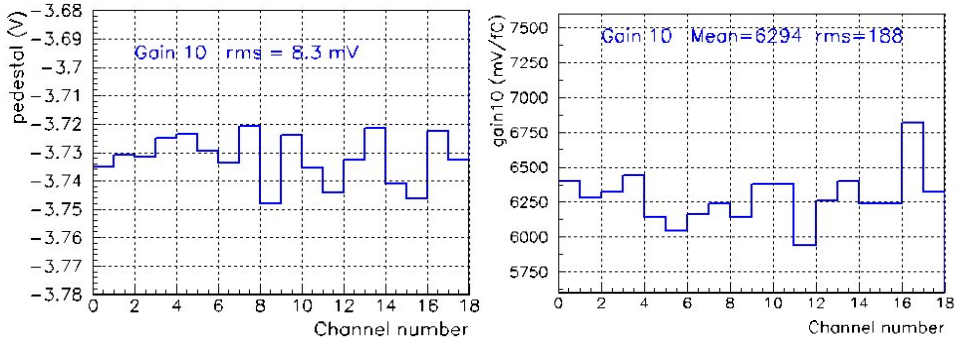

Figure 9 - Gain uniformity (left) and pedestal uniformity (right) vs channel number (gain 10)

4.3. Overall performance

The overall linearity has been measured for the various gain settings and is well within ± 0.2% up to an output voltage of 2.5 V. Residuals for a linear fit are shown below for the nominal configuration of Cf=1.6 pF and unity gain.

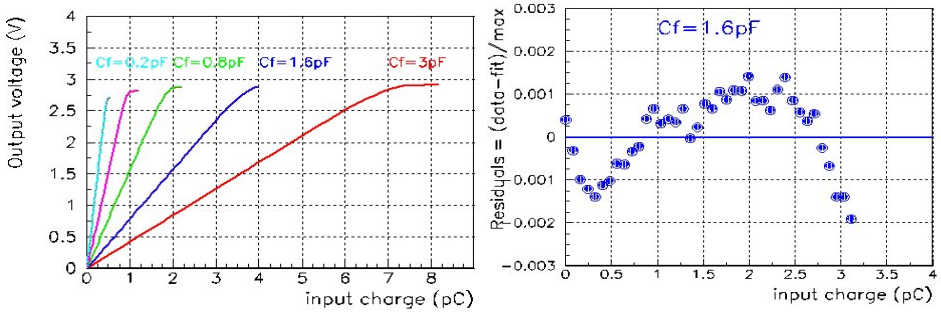

Figure 10- Overall linearity (left) and residuals to a linear fit (right) of the complete readout

The noise in this nominal configuration, with a total detector capacitance of Cd=68 pF (including PCB contribution of 47pF) is 400 µV in G1 and 200 µV without detector capacitance.. The dynamic range is thus around 6500 (12.5bits) with the detector and 13000 without (13.5 bits). Using the bi-gain readout with the gain of 10, the dynamic range can be extended to 14-16bits.

4.4. Test beam in DESY

A test beam has been performed in January 2005 in DESY to achieve the calorimeter debugging and to perform the first physics measurement. Gigabytes of data have been acquired and are currently analyzed[5]. A picture of an electromagnetic shower is shown in Figure 11.

[5] G. Mavromanolakis, these proceedings

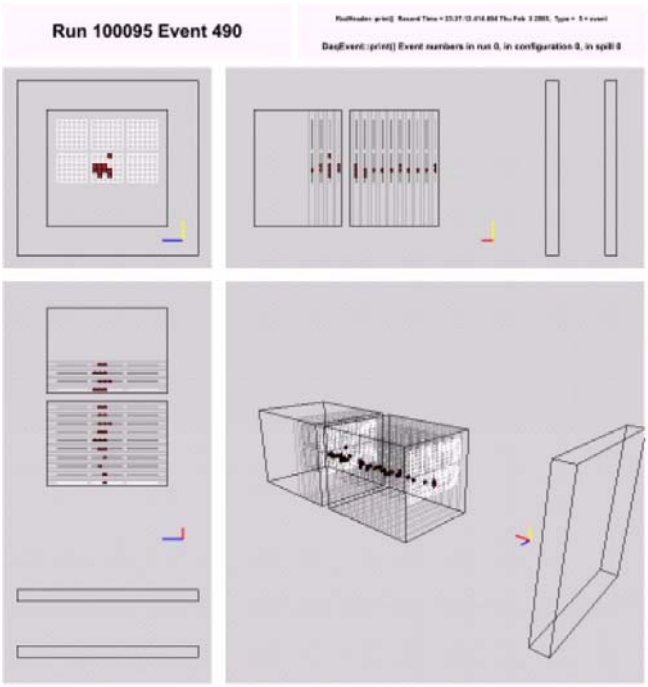

Figure 11 – 3 GeV electromagnetic shower in the ECAL(© G Mavromanolakis)

5. R&D ON PCB

5.1. Context

It has been decided by the Calice collaboration to embed the front-end chip in the detector instead of having it at the edge of the front-end PCB as planned in the TESLA TDR. That decision has been argued by the fact that long lines between detector cells and preamplifier input were generating much noise. A second argument was that industry was not easily able to built long PCB to equip a full detector slab. It is necessary then to build up the slab with several small PCBs. The last measurements made by the LAL about preamp consumption6 allow a passive cooling if the front-end chip is embedded.

5.2. The new FLC_FEV3 PCB

A new PCB called FLC_FEV3 has been designed to validate how low the industry is able to go in PCB thickness. Thanks to the reduction of wires length, the PCB has only 6 layers and is only 640µm thick. The main feature of that new FLC_FEV3 PCB is the full compatibility with the physics prototype DAQ to ensure an easy test bench setup. The FLC_PHY3 front end chips are not mounted on the back of the PCB, just behind the wafer spot. The wafer footprint is compatible with either wafers used in the physics prototype or new wafers currently in R&D embedding high voltage resistor and decoupling capacitance. These wafers should be available for the collaboration in 2005.

That PCB will be used to:

[6] C de La Taille, these proceedings

- Validate the concept of embedded chips (Front-end in an electromagnetic shower)
- Validate the epitaxial capacitance and resistor deposited on the wafers
- Validate the gluing of such new wafers

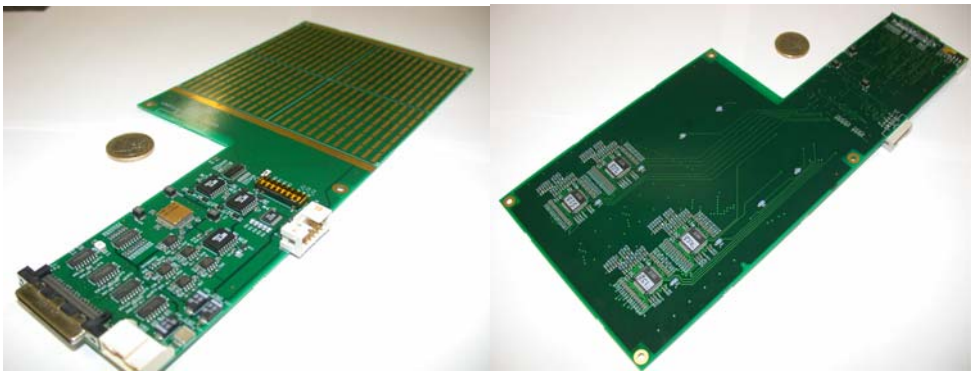

Figure 12 - Picture of the FLC_FEV3 front end board

6. CONCLUSION AND NEXT STEP

The production of electronic for the physics prototype is now finished and the R&D for a module 0 within 3 years has begun.

The front-end electronic developed fulfils W-Si test beam prototype. Using that starting point, new designs are in test yielding the final detector expectations in term of thickness, low power and features integrations.

A new PCB version is planned for the end of 2005 integrating the power switching, the A/D conversion, the ultra low thickness and much other functionality.