2005 International Linear Collider Workshop – Stanford, U.S.A.

Monolithic CMOS Pixel Detectors for ILC Vertex Detection

C. Baltay, W. Emmet, H. Neal, D. Rabinowitz
Yale University
J. Brau, O. Igonkina, N. Sinev, D. Strom
University of Oregon

1. INTRODUCTION

Studies carried out in the U.S., Europe, and Asia, have demonstrated the power of a pixel vertex detector in physics investigations at a future high energy linear collider. Until recently silicon CCD's (Charged Coupled Devices) [1] seemed like the detector elements of choice for vertex detectors for future Linear e^+ e^- Colliders. However, with the recent technology decision choosing a cold TESLA-like superconducting technology for the future International Linear Collider (ILC), the usefulness of CCD's for vertex detection has become problematical. The time structure of this cold technology is such that it necessitates an extremely fast readout of the vertex detector elements and thus CCD's as we know them will not be useful. New CCD architectures are under development [2] but have yet to achieve the required performance. For these reasons there is an increased importance on the development of Monolithic CMOS pixel detectors that allow extremely fast non sequential readout of only those pixels that have hits in them. This feature significantly decreases the readout time required. Last year, recognizing the potential of a Monolithic CMOS detector, we initiated an R&D effort to develop such devices. Another important feature of our present conceptual design for these CMOS detectors is the possibility of putting a time stamp on each hit with sufficient precision to assign each hit to a particular bunch crossing. This significantly reduces the effective backgrounds in that in the reconstruction of any particular event of interest we only need to consider those hits in the vertex detectors that come from the same bunch crossing.

2. STRAW MAN VERTEX DETECTOR DESIGN

The overall vertex detector design we are working towards is shown in Fig. 1, and the numbers and sizes of the 120 detector elements (chips) are summarized in Table 1.

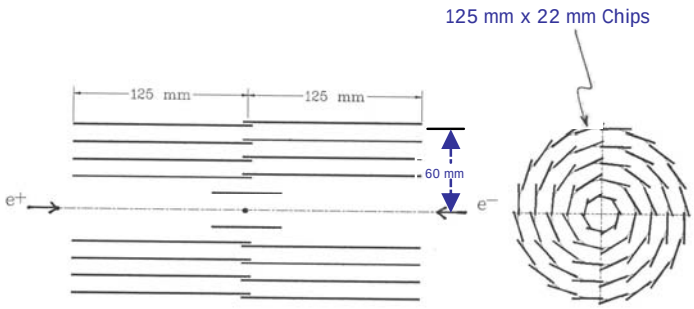

Figure 1: Vertex Detector Design, with Monolithic CMOS Pixel Detectors

Table 1

Layer	Radius	Total Length	No of Chips	Chip Size
	Cm	Cm		Cm
1	1.2	5.0	8x1	5.0x1.2
2	2.4	25.0	8x2	12.5x2.2
3	3.6	25.0	12x2	12.5x2.2
4	4.8	25.0	16x2	12.5x2.2
5	6.0	25.0	20x2	12.5x2.2

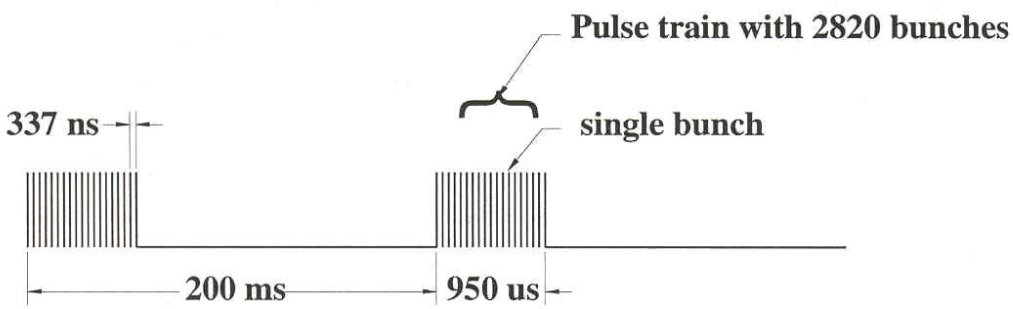

Figure 2: Time Structure for the TESLA Design

The detailed time structure of the ILC is still to be settled on in the future. For the purposes of our present design we are using the time structure of the TESLA design, shown in Fig. 2. We assume that the ILC design will have the same basic features. This design has 2820 bunches in a bunch train, with 5 bunch trains per second. The separation between bunches in 337 nanosec, which makes each bunch train about 1 millisec long, with about 200 millisec between bunch trains.

Extensive background calculations indicate that the maximum total hit rate in the vertex detector will be 0.03 hits/mm^2/bunch crossing.

3. PROGRESS ON MONOLITHIC CMOS PIXEL DETECTOR DESIGN

During the past year, in collaboration with SARNOFF, Inc. (RCA's silicon fabrication house) with whom we had an R&D contract, we developed a draft conceptual design for a device (chip) that we believe will work well for the ILC

Vertex Detector application and that SARNOFF believes they can make. We will discuss here a typical 22 mm x 125 mm chip to be fabricated by SARNOFF's CMOS process. Each chip would consist of two particle detection layers, which we call Big pixels (Macro Pixel Array) and Small pixels (Micro Pixel Array) (Big pixels ~ 50μ x 50μ, Small pixels ~ 5μ x 5μ) each layer covering the full area of the chip (i.e. ~ 100 Small pixels under each Big pixel), as sketched in Figure 3. The Big pixels will detect a hit and get the time of the hit (to a precision of better than 1/3 microsec or one bunch crossing time). There will be enough logic circuitry in each pixel that using the location of the Big pixel hit we look for hits in the Small pixels to determine the precise x and y location of the hit and get a 3 bit grey scale of the charge accumulated in each Small pixel. Even a single particle crossing will deposit charge in several Small pixels due to charge spreading beyond a pixel. The 3 bit grey scale is to allow the determination (later in the analysis) of the coordinates of the centroid of the particle to better than a pixel size. The time information for each hit in the Big pixels is stored under the area of the Big pixels with room for up to 4 hits. At 12 bits + 1 parity bit this requires 52 bits under each Big pixel which is quite manageable. The Big pixels are reset after the time is stored to get ready for the next beam crossing. The Small pixel array stores the analog signal charges locally for the ~ 1 millisec duration of the entire bunch train.

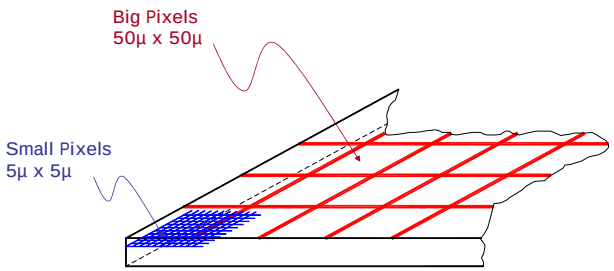

Figure 3

Due to concerns about excessive Electromagnetic Interference during the bunch train, we do not plan to read out the device until after the bunch train when we have a leisurely 200 millisec to read out not all pixels as in a CCD but only the pixels that were hit.

To get some estimates of hit rates and occupancies, we use the maximum rate of 0.03 hits/mm^2/bunch. We then expect an occupancy of ~ 10^{-6} per Small pixel and ~ 10^{-4} per Big pixel per bunch crossing. Integrating over 2820 bunches in a train we expect about 3×10^{-3} hits per Small pixel and ~ 0.3 hits per Big pixel in a bunch train. Thus we expect to only rarely exceed the storage capacity of 4 hits in each Big pixel (if need be the 4 hit limit can be increased). The total number of hits per 22 mm x 125 mm device (chip) (with 1.1×10^8 Small pixels) is expected to be ~ 3×10^5 hits/chip/bunch train. At a read out rate of 25 MHz these hits can easily be read out in well under the 200 millisec gap between bunch trains. The occupancy in the Small pixels, integrating over a bunch train, is expected to be of the order of one percent. This appears much too high to allow efficient pattern recognition. The crucial element of our design is

the availability of the time information (i.e., bunch crossing number) with each hit. If we trigger on an event that we are interested in from another part of the detector (tracker or calorimeter) with a time, i.e., the bunch crossing number known, we need to look only at those vertex detector hits which are consistent in time with the event of interest and the occupancy drops to below 10^{-5} per Small pixel (SLD worked well with an occupancy of ~ 10^{-3} per pixel in the Vertex Detector).

A first design of the architecture of the Big (Macro) and Small (Micro) Pixel Arrays by SARNOFF has now been completed.

4. PLANS FOR FUTURE STUDIES

As described above, we believe that we have a conceptual design for these detectors that will work for the Vertex Detector for a superconducting ILC, with even a considerable margin of safety. The next step we believe is to start detailed design of these devices via a contract with SARNOFF that will lead to the fabrication of some small prototypes.

There are many issues and uncertainties that will have to be addressed in the detailed design. Some of these issues apparent at this time are:

- SARNOFF feel they can build devices with pixels as small as 5μ x 5μ, have large area chips, 25 MHz read rate, and sufficient logic under each pixel to do what it needs to do in this conceptual design. Can they achieve all of these features simultaneously on one chip?
- How thin can these devices be thinned below the standard 500μ thickness?
- Radiation hardness
- Power consumption
- Will the Electromagnetic Interference during a bunch train affect adversely the functioning of the device at the pixel level?

We believe that the funding that will be available this coming year will not be sufficient to carry out both the detailed design by SARNOFF and the fabrication of the first prototypes. We foresee two options. The first is to find Japanese or European collaborators to put in some funds to allow SARNOFF to proceed with prototypes this coming year. The second option is to delay the fabrication of the first prototypes until the following year.

References

[1] K. Abe, et. Al., "Design and Performance of the SLD Vertex Detector, a 307 Mpixel Tracking System," Nucl. Instrum. Meth. A400, 287 (1997)

[2] C. S. J. Damerell, LCWS 2004, Paris, April, 2004, http://hepww.rl.ac.uk/lcfi/public/lcws-damerell.ppt; Y. Sugimoto, 7th ACFA Linear Collider Workshop, Taipei, Nov. 10, 2004, http://hep1.phys.ntu.edu.tw/ACFA7/slides/B-4 Sugimoto.ppt